CO224 Group – 11

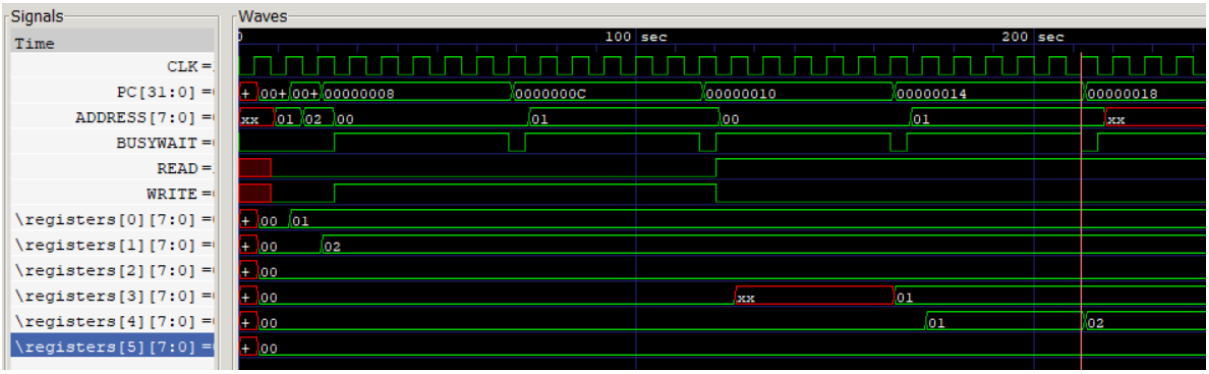
Computer Architecture E/10/129, E/10/408

Building a Memory Hierarchy

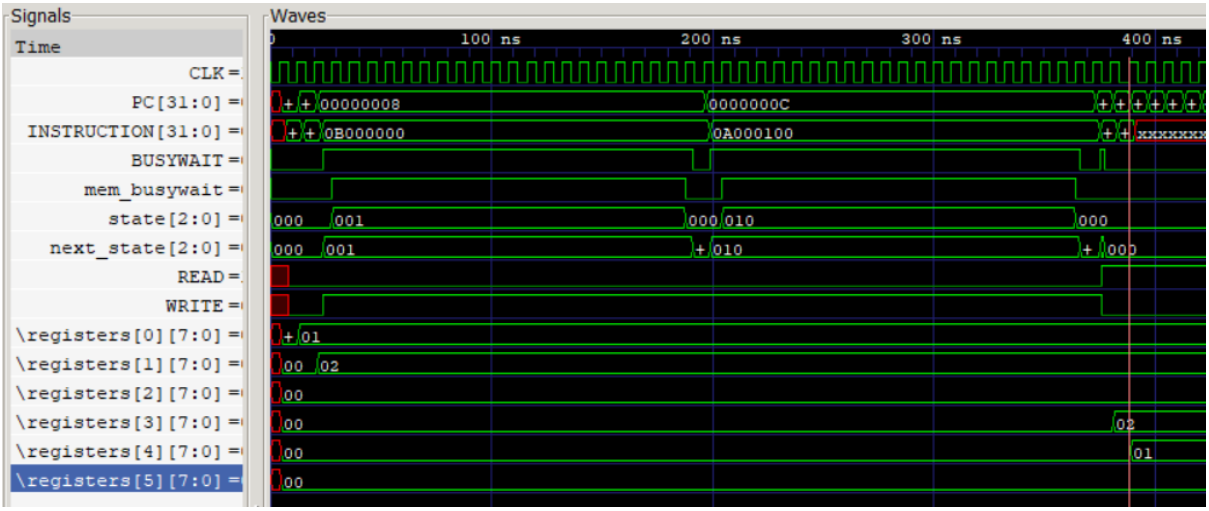
Test Code1:

```
loadi 0 0x01
loadi 1 0x02
swi 0 0x00
swd 1 0
lwi 3 0x00
lwd 4 0
```

The waveform of part 1 program (without cache):



The waveform of part 2 program (with cache):



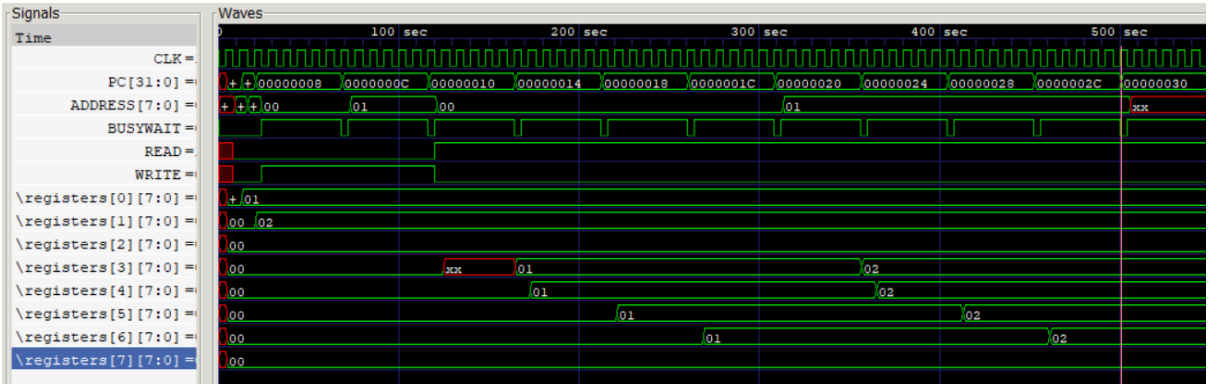
For the given program, part 1 implementation executes in 213s but in part2 implementation its execution time is 389s.

When reading for the first time, the system with the cache needs to load data blocks from the data memory to the cache. Since reading data blocks consumes more time than reading a single word in data memory (as in the system without a cache), the system with the cache takes more time to execute the program.

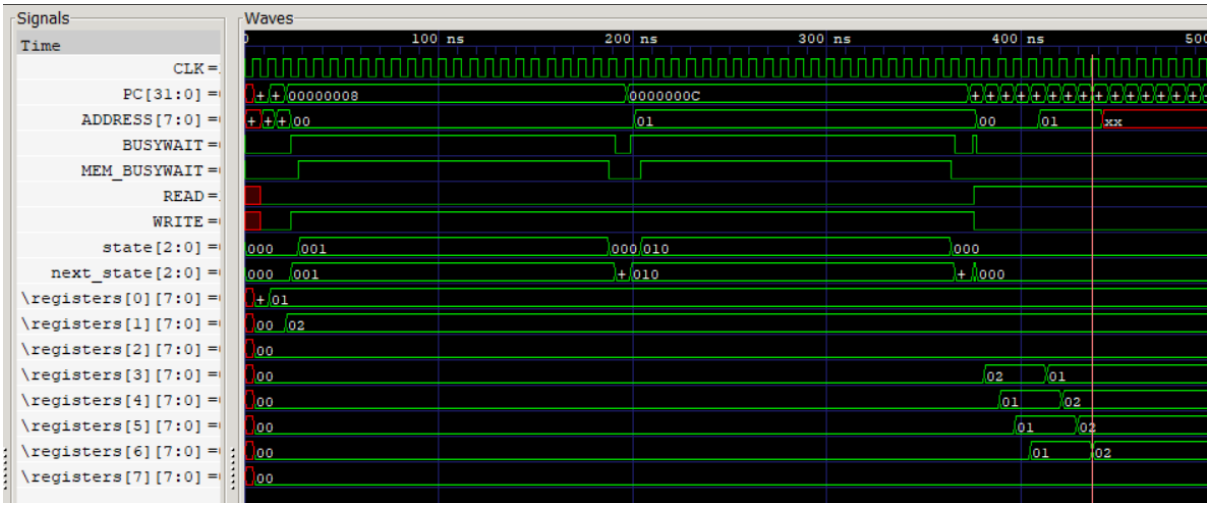
TestCode2:

```
loadi 0 0x01
loadi 1 0x02
swi 0 0x00
swd 1 0
lwi 3 0x00
lwi 4 0x00
lwi 5 0x00
lwi 6 0x00
lwd 3 0
lwd 4 0
lwd 5 0
lwd 6 0
```

The waveform of part 1 program:



The waveform of part 2 program:

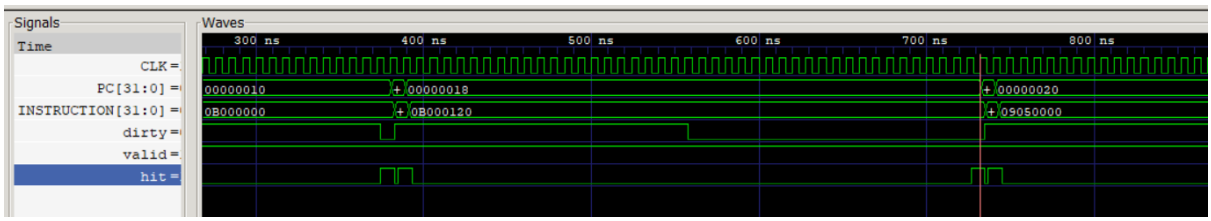


For the given program, part1 implementation executes in 501s but in part2 implementation its execution time is 437s.

After loading the cache for the first time, the system with the cache works more efficiently. That is because, if reading or writing is a hit the data can be fetched within one clock cycle. In the system without cache, it takes 40 clock cycles for each data to be fetched from the data memory.

However, if there is a read miss or write miss with a dirty bit = 1, the system should write back the current data block to the memory and load the new data block from the memory. It consumes a lot of time than directly reading a word from data memory.

```
loadi 0 0x01
loadi 1 0x08
swd 1 0
lwd 2 0
swi 0 0x00
lwi 3 0x00
swi 1 0x20
lwi 4 0x20
lwi 5 0x00
lwi 6 0x20
```



Even if the dirty bit=0 for the read or write miss, the time it takes to load the data block from the memory consumes more time.

Thus, according to the above results, it can be observed that when there is a high hit count, the system with cache works more efficiently whereas if the count of misses is high, the system without cache is more efficient.