

Kanishka Gunawardana

Department of Computer Engineering, University of Peradeniya, Sri Lanka

+94 76-2152049 | kanishkagunawartha@gmail.com | [Portfolio](#) | [LinkedIn](#) | [GitHub](#) | [Google Scholar](#)

Profile

Top-ranked Computer Engineering graduate with strong interests in Computer Architecture, Embedded Systems, and Neuromorphic Computing, complemented by experience in Intelligent Systems. Dedicated to leveraging hardware-software co-design to solve real-world challenges, with demonstrated leadership, research excellence, and a collaborative mindset.

Education

University Of Peradeniya

Undergraduate in B.Sc. Engineering(Hons.) Computer Engineering

Nov. 2021 – Aug. 2025

GPA: 4.0/4.0, Rank: 1/486

Dharmaraja College Kandy

G.C.E. Advanced Level Examination

Nov. 2006 – Aug. 2019

Z-score: 2.5661

National Rank - **149/19508**, District Rank - **11/1189**

Experience

Temporary Instructor

Department of Computer Engineering, University of Peradeniya

Aug. 2025 – Present

Instructing courses in computer architecture, digital design and embedded systems, including labs and evaluations. Conducting neuromorphic accelerator research with the [PeraMorphIQ Neuromorphic Research Group](#) and mentoring project teams at the [ESCAL Lab](#) on on-chip learning, memory power optimizations, and system architecture.

Software Engineering Intern

WSO2 LLC, Colombo, Sri Lanka

Jul. 2024 – Dec. 2024

Developed Ballerina integrations, including the [OpenAI Finetunes Connector](#). Worked on [ISO20022-to-SwiftMT](#) message conversion using Ballerina for financial message interoperability, along with SaaS-based app design and development.

Publications

Optimized Multi-Processor System-on-Chip (MPSoC) Design for Low-Resource JPEG Encoding

K.H. Gunawardana et al. | ICAC 2024 (Colombo) | DOI:10.1109/ICAC64487.2024.10851123

- Implemented an FPGA MPSoC JPEG encoder on Cyclone IV using Nios II/e cores; introduced lightweight custom hardware instructions and custom FIFO queues to offload compute-critical stages and reduce processor stalls.
- Achieved 2.8× throughput improvement; superscalar options were evaluated but deprioritised.

Undergraduate Research Thesis

SNAP-V: A RISC-V SoC with Configurable Neuromorphic Acceleration for Small-Scale Spiking Neural Networks (Final Year Thesis) |

Nov. 2024 – Jul. 2025






- Designed and developed a dual-core RISC-V System-on-Chip integrating a configurable neuromorphic accelerator with over 1k LIF neurons organized into parallel clusters interconnected through a hierarchical Network-on-Chip (H-NoC), enabling efficient spike-based computation for small-scale SNNs in low-power edge applications.
- Validated the SoC on MNIST using Synopsys (VCS/PrimePower) and Xilinx Vivado, achieving 96.69% accuracy (within an average 2.62% of baseline) and state-of-the-art energy efficiency of 1.39 pJ/synaptic operation.
- Technology: **RISC-V, Chisel, Chipyard, Verilog-HDL, Synopsys VCS/PrimePower, Vivado**

Selected Projects

RV32IM 5-stage Pipeline Processor | *Group* |

Dec. 2024 – Jul. 2025

- Implemented a 5-stage pipelined RISC-V RV32IM processor with in-order hazard handling, explored AXI-based memory integration for SoC compatibility, performed RTL power and static timing analysis (0.197 mW, 142 MHz), automated the analysis via a GitHub Actions CI/CD workflow, and prototyped the design on a Virtex-7 FPGA.
- Technology: **Verilog HDL, Synopsys DC, VCS, RTLA, PrimePower, GTKWave, GitHub**

- Impact Tracking System for Athletes (3YP)** | *Group* |   Nov. 2023 – Mar. 2024
- Developed a real-time head impact monitoring system for contact sports using wearable devices and desktop dashboards, facilitating prompt concussion identification, post-session data transmission, and comprehensive analytics for player safety and informed decision-making.
 - Contributions: Led hardware and firmware design and development of wearable devices, developed the centralized hub and WIFI local communication, contributed to backend API, and deployed the system on AWS EC2.
 - Technologies: **C++, ESP32, Raspberry Pi, MQTT, Python, Express.js, MongoDB, AWS**
- Field-Based Approach for Quantifying Plant Leaf Color** | *Group* |   Aug. 2023 – Nov. 2023
- Developed a mobile application with a backend that utilizes Image Processing and Computer Vision to objectively quantify plant leaf colour by analyzing information extracted from captured leaf images.
 - Contributions: Developed the backend API for image analysis using FastAPI and contributed to image preprocessing, including image segmentation with a Mask R-CNN model fine-tuned for leaf segmentation.
 - Technology: **Python, OpenCV, Pytorch, FastAPI**
- 8-bit Single-cycle Processor** |  Mar. 2023 – Jun 2023
- Designed and implemented an 8-bit single-cycle processor architecture in Verilog HDL with instruction and data caches, featuring a memory unit and a MIPS-inspired ISA supporting arithmetic, logic, and control operations.
 - Developed a comprehensive testbench for verification and waveform analysis using GTKWave tool.
 - Technology: **Verilog-HDL, GTKWave**

Achievements

- SLIoT Challenge 2023** | *Sri Lankan Biggest IOT Competition* | *Team: IMPAX* Mar. 2024
- 1st runners-up (Out of 100+ Teams) | *Organized by UOM in collaboration with SLT-MOBITEL and IESL*
- MoraXtream 8.0** | *12 hour algorithmic programming competition* | *Team: Five4Five* Nov. 2023
- National Rank - 4 (Out of 400+ Teams) | *Organized by the IEEE Student Branch of the University of Moratuwa*
- IEEE Xtreme 17.0** | *24 hour algorithmic programming competition* | *Team: Five4Five* Nov. 2023
- Global Rank - 374 (Out of 16500+ participants), National Rank - 24 (Out of 330 Teams)
- ACES Coders v10.0** | *12 hour algorithmic programming competition* | *Team: Five4Five* Oct. 2023
- National Rank - 12 (Out of 350+ participants) | *Organized by the ACES*

Selected Certificates

- Machine Learning Specialization - Stanford University & DeepLearning.AI (Coursera) Sep. 2023
- Supervised Machine Learning: Regression and Classification
 - Unsupervised Learning, Recommenders, Reinforcement Learning
 - Advanced Learning Algorithms

Technical Skills

Languages: Python, C/C++, Java, JavaScript, TypeScript, SQL, Verilog HDL, ARM assembly, Ballerina.
Frameworks: Arduino, Express.js, Spring Boot, FastAPI, Node.js, React.js.
Libraries: OpenCV, NumPy, Pandas, Matplotlib, PyTorch, TensorFlow.
Developer Tools: Linux, Git, Docker, AWS, Quartus II, Nios II, GTKWave, Vivado.
EDA & Verification: Synopsys Design Compiler, VCS, PrimeTime, PrimePower.

Extra-Curricular Activities

- Volunteering Project Nenathambara - University of Peradeniya Sep. 2023 - Jul. 2024
- Head of Web Development - Robotics Society, University of Peradeniya Sep. 2023 - Aug. 2024
- Executive Committee Member - Robotics Society, University of Peradeniya Dec. 2022 - Sep. 2023
- Member of Rotaract Club of University of Peradeniya Dec. 2021 - Dec. 2023

References

- Dr. Isuru Nawinne | isurunawinne@eng.pdn.ac.lk
 Senior Lecturer, Department of Computer Engineering, Faculty of Engineering, University of Peradeniya, Sri Lanka.
- Prof. Roshan G. Ragel | roshanr@eng.pdn.ac.lk
 Professor, Department of Computer Engineering, Faculty of Engineering, University of Peradeniya, Sri Lanka.