SCHOOL OF ELECTRONICS ENGINEERING

Fall Semester 2024-2025

BECE102P – Digital Systems Design LAB

Task -5

Voting machine

by

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Summary

Summary of the Project

This project focuses on designing and implementing an FPGA-based voting machine for two candidates using the Cyclone IV E FPGA device and the DE2-115 development board. The system utilizes Verilog HDL to create a simple yet effective digital voting system capable of counting votes, displaying results, and determining the winner.

Key Features and Functionalities

Vote Counting:

Two push buttons allow users to cast votes for Candidate 1 and Candidate 2.
Votes are stored in registers and displayed on 7-segment displays in real-time.

Result Display:

A switch triggers the result evaluation, comparing vote counts to determine the winner.
The winner is displayed using a 2-bit signal:
01 for Candidate 1
10 for Candidate 2
00 for a tie.

Reset Mechanism:

A reset switch clears all vote counts and results, preparing the system for a new voting session.

Design Approach

The project was implemented using Verilog HDL, synthesized and simulated in Quartus II and **ModelSim.**
Pin mappings were assigned to utilize the DE2-115 board components effectively:
Onboard clock for synchronization.
Push buttons for vote casting.
Switches for reset and result display.
7-segment displays for real-time vote count visualization.

System Model

Inputs include the clock signal, reset button, voting buttons, and result display trigger.
Outputs include 7-segment displays showing vote counts and a signal indicating the winner.
The logic consists of counters for vote storage, comparators for result evaluation, and reset

functionality.

Practical Impact

Social Benefits:

Demonstrates a transparent and error-free electronic voting process suitable for small-scale applications like schools, organizations, and mock elections.

Environmental Benefits:

Reduces the use of paper ballots, promoting environmental sustainability.

Challenges and Achievements

Designing the logic for real-time vote counting and ensuring synchronization using the FPGA clock were key challenges.

Successfully synthesized and tested the design with no timing violations or functional errors, achieving accurate and reliable operation.

Conclusion

The FPGA-based voting machine is a cost-effective, eco-friendly, and reliable system for small-scale voting applications. It highlights the power of FPGA technology in creating efficient digital systems. With further enhancements, such as adding authentication or encrypted data storage, this design could serve as the foundation for more advanced voting systems.

This project underscores the practical application of digital design principles and the versatility of FPGA devices in solving real-world problems.

AIM:

To design and implement a voting machine on the Cyclone IV E FPGA device (DE2-115 board) using Verilog HDL. The system allows electronic voting for two candidates, displays the vote counts on 7-segment displays, and determines the winner based on the highest votes.

WORKING PRINCIPLE:

Vote Casting:

Each candidate is assigned a dedicated button (KEY[0] for Candidate 1 and KEY[1] for Candidate 2).
Pressing a button increments the corresponding candidate's vote count by 1, which is stored in a 4-bit register.
The updated vote count is displayed on the corresponding 7-segment display (HEX0 for Candidate 1, HEX1 for Candidate 2).
Result Display:

When the show_result switch (SW[1]) is activated, the FPGA compares the vote counts.
The candidate with the higher vote count is declared the winner, and the result is displayed using a 2-bit binary output:
01: Candidate 1 Wins
10: Candidate 2 Wins
00: No clear winner (tie or no votes).
Reset Functionality:

Activating the reset switch (SW[0]) clears all vote counts and resets the result output to 00, preparing the system for a new voting session.

SYSTEM MODEL/ALGORITHM:

SYSTEM MODEL:

The FPGA-based voting machine for two candidates is modeled as a digital system composed of the following key components:

Inputs:

clk (Clock): Synchronizes the operation of the system.
reset: Resets the system, clearing all vote counts and the result.
vote_1 and vote_2: Buttons used to cast votes for Candidate 1 and Candidate 2, respectively.
show_result: A switch to trigger the result display.
Outputs:

candidate_1_votes and candidate_2_votes: Registers that store and display the number of votes received by Candidate 1 and Candidate 2 on 7-segment displays.
winner: A 2-bit signal indicating the winner (01 for Candidate 1, 10 for Candidate 2, and 00 for a tie).
Registers and Logic Blocks:

Vote Registers: Store the vote counts for the candidates.
Comparator Logic: Determines the winner based on the vote counts.
Reset Logic: Clears all vote counts and the result when the reset signal is triggered.

ALGORITHM:

The operation of the system can be summarized in the following steps:

Initialization:

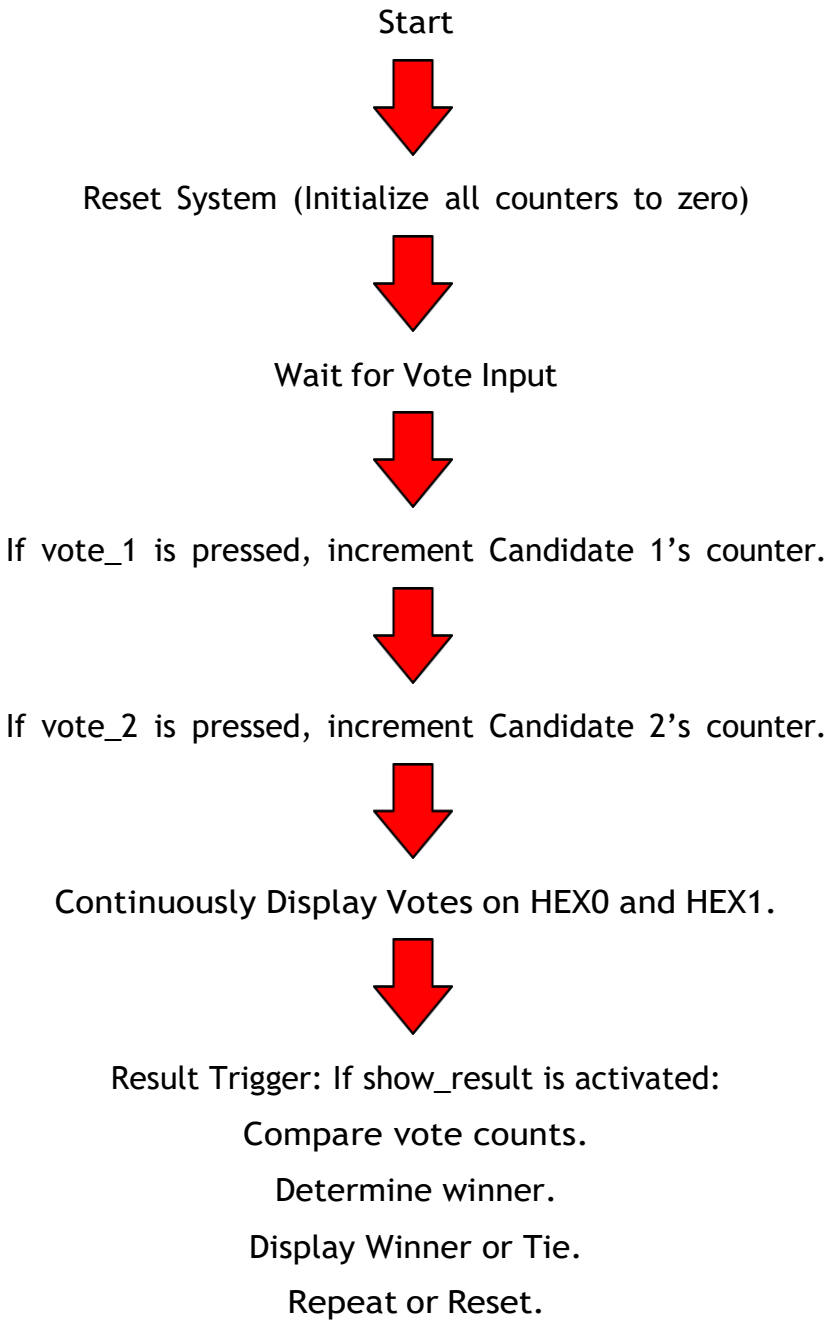
When the reset signal is activated, set all vote counters (candidate_1_votes, candidate_2_votes) to zero. Set the winner signal to 00 (no result).
Vote Casting:

When vote_1 is pressed, increment the value of candidate_1_votes by 1.
When vote_2 is pressed, increment the value of candidate_2_votes by 1.
Continuously display the updated vote counts on the 7-segment displays (HEX0 for Candidate 1, HEX1 for Candidate 2).
Result Evaluation:

When show_result is activated, compare the vote counts:
If candidate_1_votes > candidate_2_votes, set winner = 01 (Candidate 1 wins).
If candidate_2_votes > candidate_1_votes, set winner = 10 (Candidate 2 wins).

If candidate_1_votes == candidate_2_votes, set winner = 00 (tie).

FLOWCHART FOR SYSTEM OPERATION:



(Software and Hardware Details)

SOFTWARE TOOLS:

Quartus II: Used for designing, compiling, and synthesizing the Verilog code.

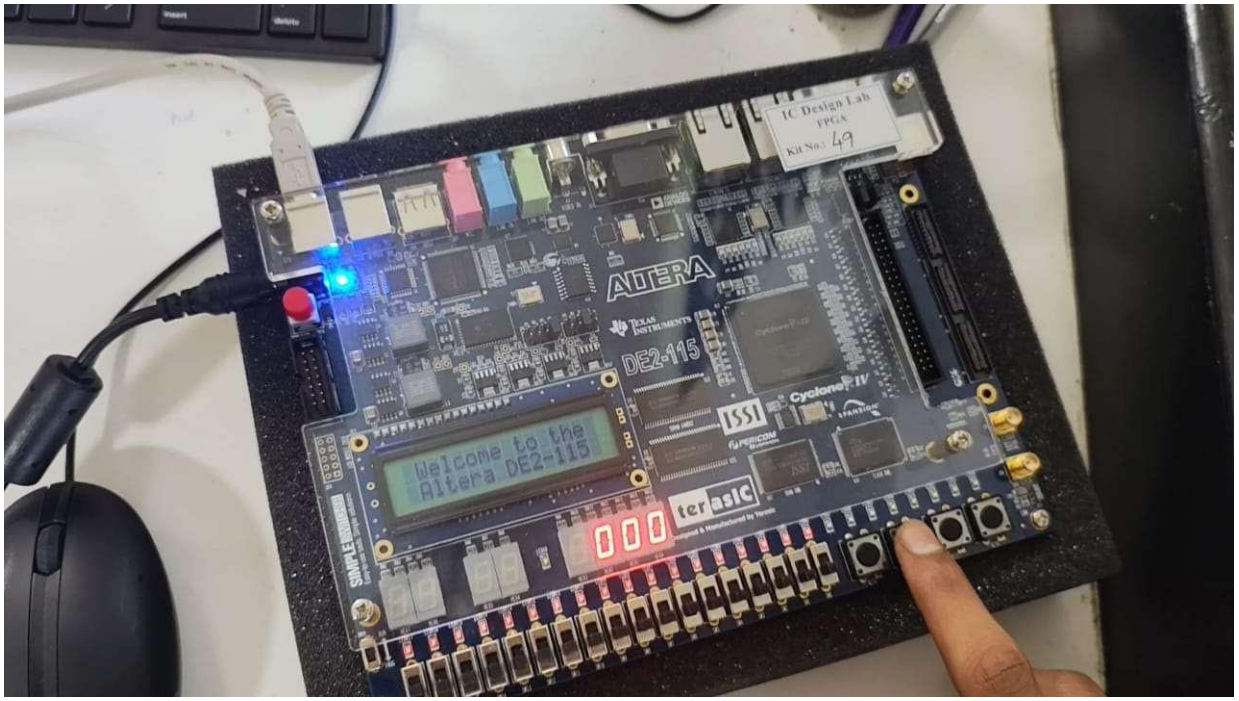
ModelSim: For functional simulation of the design.

Waveform Analysis Tools: For verifying the working of the design.

HARDWARE COMPONENTS:

Cyclone IV E FPGA (EP4CE115F29C7): The FPGA chip used for implementing the voting machine.
DE2-115 Development Board: Provides the platform for testing and demonstrating the project.
Push Buttons: Mapped to cast votes for candidates.
Switches: Mapped for system reset and result release functionality.
7-Segment Displays: Display the vote count for each candidate.
Onboard Clock: Provides a 50 MHz clock signal for synchronization.

PROJECT DEMO SETUP:



OUTPUT/RESULTS:

The FPGA-based voting machine for two candidates produces the following outputs based on user inputs:

Vote Counts
The number of votes for Candidate 1 is displayed on HEX0 (7-segment display).
The number of votes for Candidate 2 is displayed on HEX1 (7-segment display).
Each button press (vote_1 for Candidate 1 and vote_2 for Candidate 2) increments the respective vote count, which is updated in real-time.
Winner Display

When the show_result switch is activated:
If Candidate 1 has more votes than Candidate 2, Winner = 01 is displayed (using LEDs or on a digital interface).
If Candidate 2 has more votes than Candidate 1, Winner = 10 is displayed.
If both candidates have the same number of votes, Winner = 00 (indicating a tie).

SOCIAL / ENVIRONMENTAL IMPACT:

Social Impact:

Provides a simple and cost-effective solution for small-scale voting processes such as in schools, organizations, or mock elections.
Promotes transparency and eliminates human errors in vote counting.
Encourages the adoption of technology in democratic processes, fostering digital literacy.

Environmental Impact:

Reduces the dependency on paper-based ballots, contributing to environmental sustainability.
Minimizes physical resource requirements, lowering the carbon footprint associated with traditional voting systems.

CONCLUSION :

The FPGA-based voting machine designed in this project is a compact, reliable, and efficient solution for small-scale voting applications. Utilizing the Cyclone IV E FPGA device and DE2-115 development board, the system ensures real-time vote counting, result display, and winner determination with precision. Its transparent operation and error-free performance make it an excellent prototype for educational, organizational, and community-level elections, showcasing the practical potential of FPGA technology.

Additionally, this project promotes environmental sustainability by eliminating the need for paper-based voting systems, contributing to eco-friendly practices. By leveraging Verilog HDL for design and FPGA synthesis, the project enhances understanding of digital system principles and real-world hardware implementation.

With future enhancements, such as voter authentication and encrypted data handling, the design can evolve into a scalable and sophisticated voting system. This work demonstrates how technology can address practical challenges effectively.