Op-amp analysis, measurement, and design

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Contents

Aim: Learn how to analyse, measure, and design op-amps.

Variables definition:

V_E: Emitter voltage V_C: Collector voltage V_B: Base voltage

I_E: Emitter current I_C: Collector current I_B: Base current

P_D: Quiescent power dissipation

A_d: Voltage gain A_{tot}: Total voltage gain A_{CM}: Common-mode gain

R_{in}: Input impedance R_{out}: Output impedance

Section 1: Op-amp DC/AC Analysis

Circuit:

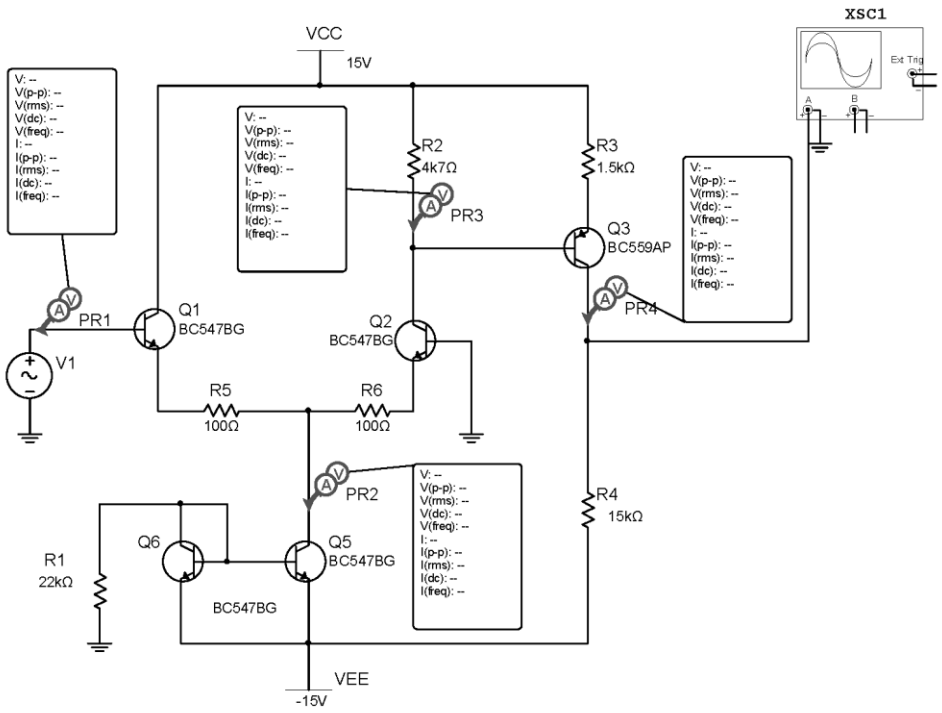


Figure 1 Op-amp circuit

1. DC Analysis:

DC collector currents and voltages in the circuit：

Calculation of **Q6**:

$$V_{E6} = V_{E5} = VEE = -15V$$

$$V_{BE6} = 0.7V$$

$$V_{C6} = V_{B6} = V_{E6} + V_{BE6} = -15 + 0.7 = -14.3V$$

$$I_{C6} = \frac{V_{C6}}{R_1} = -\frac{14.3}{22k} = -650\mu A$$

Calculation of **Q5**:

$$I_{C5} = I_{C6} = -650\mu A$$

Assume Q1 and Q2 match, so they share the same current:

$$I_{E1} = I_{E2} = I_{R5} = I_{R6} = \frac{I_{C5}}{2} = -\frac{650}{2} = -325\mu A$$

$$I_{C1} = -I_{E1} = 325\mu A$$

Voltage part:

Because base of Q1 and Q2 is grounded

$V_{BE1} = 0.7V = V_{B1} - V_{E1}$, and $V_{B1} = 0V$

$$V_{E1} = -0.7V$$

$$V_{R5} = I_{R5} * R_5 = -325\mu A * 100 = -0.0325V$$

$$V_{C5} = V_{E1} - V_{R5} = -0.7 + 0.0325 = -0.6675V$$

Calculation of **Q1**:

$$I_{C1} = -325\mu A$$

$$V_{C1} = VCC = 15V$$

Calculation of **Q2**:

Q2 shares the same emitter current and voltage with Q1, because the base of Q2 is also grounded.

Hence,

$$I_{C1} = I_{C2} = 325\mu A$$

Because $I_{B3} = 0A$, $I_{R2} = I_{C2}$

$$V_{R2} = I_{R2} * R_2 = 325\mu A * 4700\Omega = 1.5275V$$

$$V_{C2} = VCC - V_{R2} = 15 - 1.5275 = 13.4725V$$

Calculation of **Q3**:

$$V_{B3} = V_{C2} = 13.4725V$$

$$V_{BE3} = 0.7V = V_{B3} - V_{E3}$$

Hence, $V_{E3} = V_{B3} - V_{BE3} = 13.4725 - 0.7 = 12.7725V$

$$V_{R3} = VCC - V_{E3} = 15 - 12.7725 = 2.2275V$$

$$I_{R3} = \frac{V_{R3}}{R_3} = \frac{2.2275}{1500} = 1.485mA$$

And $I_{E3} = I_{R3} = 1.485mA$

$$I_{C3} = I_{R4} = -I_{E3} = -1.485mA$$

$$V_{R4} = I_{R4} * R_4 = -1.485mA * 15000\,\Omega = -22.275V$$

$$V_{C3} = VEE - V_{R4} = -15 + 22.275 = 7.275V$$

All DC collector currents and voltages are listed below.

Transistor	Collector Current	Collector Voltage
Q1	325μA	15V
Q2	325μA	13.4725V
Q3	-1.485mA	7.275V
Q5	-650μA	-0.6675V
Q6	-650μA	-14.3V

Quiescent power dissipation for each transistor and the voltage gains of each stage in the op-amp circuit

$$P_D = I_C * V_{CE}$$

$$P_{D1} = I_{C1} * V_{CE1} = 325\mu A * (VCC - V_{E1}) = 325\mu A * \big(15 - (-0.7)\big) = 5.1025mW$$

$$P_{D2} = I_{C2} * V_{CE2} = 325\mu A * (V_{C2} - V_{E2}) = 325\mu A * \big(13.4725 - (-0.7)\big) = 4.6mW$$

$$P_{D3} = I_{C3} * V_{CE3} = 1.485mA * (V_{C3} - V_{E3}) = 1.485mA * \big(7.275 - (12.7725)\big) = 8.16mW$$

$$P_{D5} = I_{C5} * V_{CE5} = 650\mu A * (V_{C5} - V_{E5}) = 650\mu A * \big(-0.6675 - (-15)\big) = 9.3mW$$

$$P_{D6} = I_{C6} * V_{CE6} = 650\mu A * (V_{C6} - V_{E6}) = 650\mu A * \big(-14.3 - (-15)\big) = 0.455mW$$

2. AC Analysis:

Calculation of the voltage gain of each stage

Gain stage

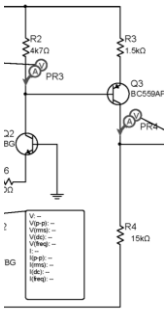


Figure 2 Gain stage

$$A_d = \frac{V_{od}}{V_{id}} = \frac{Total\ resistance\ in\ collector\ circuit}{Total\ resistance\ in\ emitter\ circuit} = \frac{\alpha R_C}{R_E}$$

$$\alpha = \frac{\beta}{\beta + 1} = \frac{400}{400 + 1} \cong 1$$

$$r_{e3} = \frac{25mV}{I_{C3}} = \frac{25mV}{1.485mA} = 16.8\Omega$$

$$A_{d1} = \frac{V_{od}}{V_{id}} = \frac{\alpha R_C}{R_E} = \frac{\alpha R_4}{R_3 + r_{e3}} = \frac{15k\Omega}{1.5k\Omega + 16.8} = 9.89 = 20\log(9.89) = 19.9dB$$

Hence, voltage gain of the gain stage $A_{d1} = 19.9dB$

Differential amplification stage

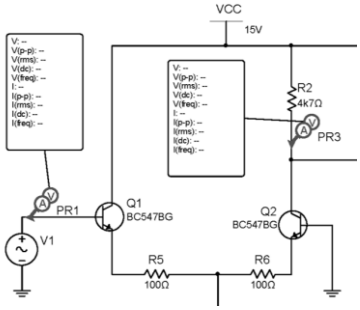


Figure 3 Differential amplification stage

$$A_d = \frac{V_{od}}{V_{id}} = \frac{Total\ resistance\ in\ collector\ circuit}{Total\ resistance\ in\ emitter\ circuit} = \frac{\alpha R_C}{R_E}$$

$$r_{e1} = r_{e2} = \frac{25mV}{I_{C2}} = \frac{25mV}{325\mu A} = 76.9\Omega$$

$$A_{d2} = \frac{V_{od}}{V_{id}} = \frac{\alpha R_C}{R_E} = \frac{\alpha R_2}{R_6 + r_{e2} + R_5 + r_{e1}} = \frac{4700}{100 + 76.9 + 76.9 + 100} = 13.3 = 20\log(13.3)$$
$$= 22.5dB$$

Hence, voltage gain of the differential amplification stage $A_{d2} = 22.5dB$

Total voltage gain:

$$A_{tot} = A_{d1} * A_{d2} = 13.3 * 9.89 = 131.5 = 20log131.5 = 42.4dB$$

Input/Output impedance

Assuming input voltage source V_1 =20mV @ 1kHz

$$I_{E1} = -325uA$$

$$I_{b1} = \frac{I_{E1}}{\beta + 1} = \frac{-325uA}{400 + 1} = 0.81uA$$

$$R_{in} = \frac{V_{in}}{I_{in}} = \frac{20mV}{0.81uA} = 24.7k\Omega$$

$$R_{out} = R4 = 15k\Omega$$

CMRR:

Ideally, the common-mode gain should be 0. Hence, $A_{cm} = 0$

$$CMRR(dB) = 20log\frac{|A_d|}{|A_{cm}|} = 20log\frac{131.5}{0} = \infty dB$$

Hence, the theoretical CMRR should be infinite.

Voltages swing:

$$V_{out} = A_{tot} * V_{in} = 131.5 * 20mV = 2.63V$$

Hence, the maximum output voltage swing is from -2.63V to 2.63V.

Ideally, an op-amp should have a very high input impedance (MΩ), low output impedance (10-100 Ω), very high voltage gain (> 100,000 = 100 dB), and a very high CMRR (> 100dB). Is this the case with this simple circuit?

$$R_{in} = 24.7k\Omega$$
$$R_{out} = 15k\Omega$$
$$A_{tot} = 42.4dB$$
$$CMRR(dB) = \infty dB$$

	Theoretical results	Ideal results	Comments
Input impedance	$24.7k\Omega$	$M\Omega$	Large difference
Output impedance	$15k\Omega$	$10-100\Omega$	Large difference
Total voltage gain	$42.4dB$	$>100dB$	Large difference
CMRR	∞dB	$>100dB$	Great result

Except for CMRR, other data cannot meet the ideal values.

Section 2: Simulation of op-amp circuit

NI MultiSim schematic of op-amp circuit

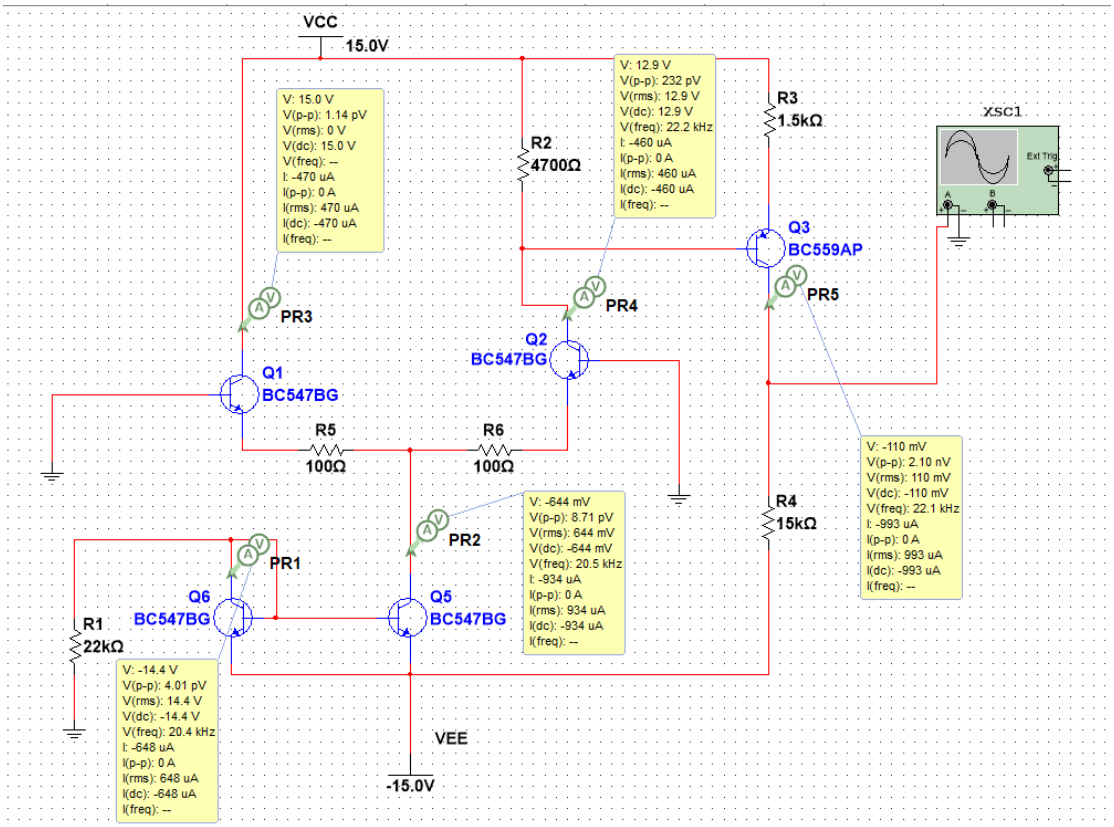


Figure 4 NI MultiSim schematic of op-amp circuit

1. DC analysis:

DC collector currents and voltages in the circuit

Transistor	Collector Current	Collector Voltage
Q1	-470μA	15V
Q2	-460μA	12.9V
Q3	-993μA	-110mV
Q5	-934μA	-644mV
Q6	-648μA	-14.4V

Quiescent power dissipation for each transistor

$$P_D = I_C * V_{CE}$$

$$P_{D1} = I_{C1} * V_{CE1} = 470\mu A * (VCC - V_{E1}) = 470\mu A * \big(15 - (-0.597)\big) = 7.33mW$$

$$P_{D2} = I_{C2} * V_{CE2} = 460\mu A * (V_{C2} - V_{E2}) = 460\mu A * \big(12.9 - (-0.598)\big) = 6.2mW$$

$$P_{D3} = I_{C3} * V_{CE3} = 993\mu A * (V_{C3} - V_{E3}) = 993\mu A * \big(0.11 - (13.5)\big) = 13.3mW$$

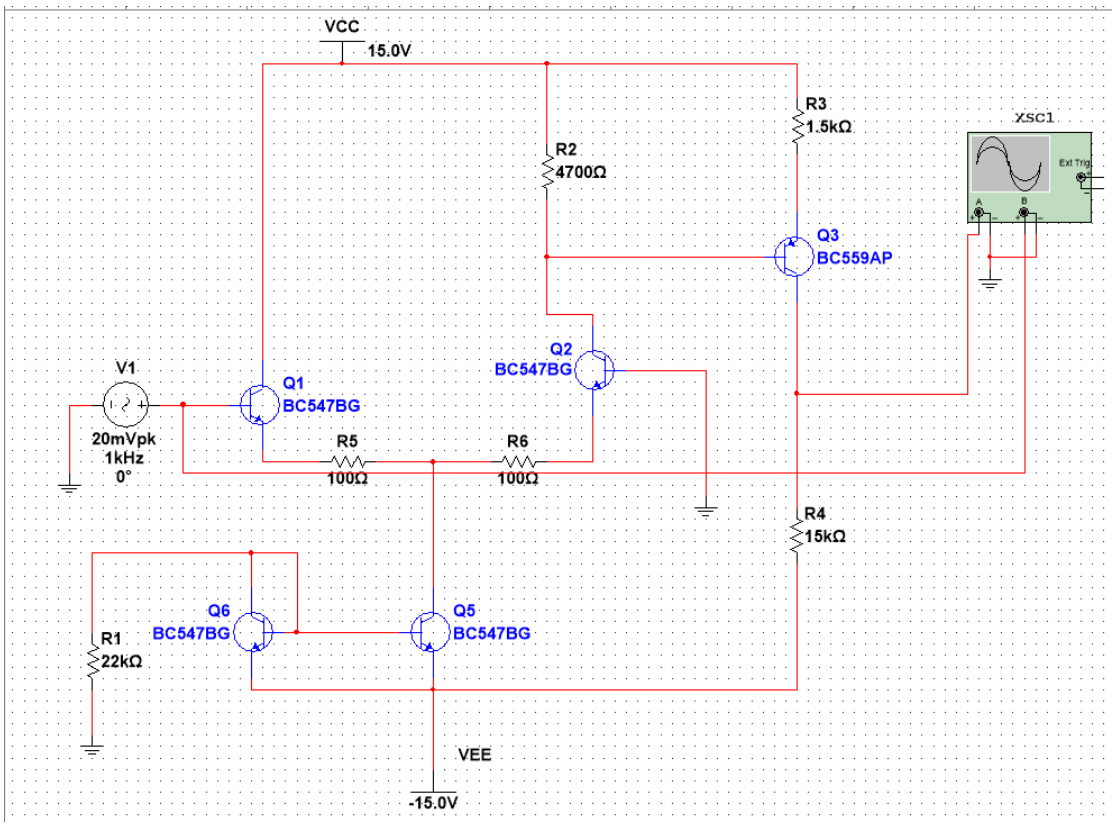
$$P_{D5} = I_{C5} * V_{CE5} = 934\mu A * (V_{C5} - V_{E5}) = 934\mu A * \big(-0.644 - (-15)\big) = 13.4mW$$

$$P_{D6} = I_{C6} * V_{CE6} = 648\mu A * (V_{C6} - V_{E6}) = 648\mu A * \big(-14.4 - (-15)\big) = 0.389mW$$

2. AC analysis:

Set the single input voltage source V_1 =20mV @ 1kHz

All current and voltage in the calculation are the peak values.



Calculation of voltage gain of each stage

Gain stage

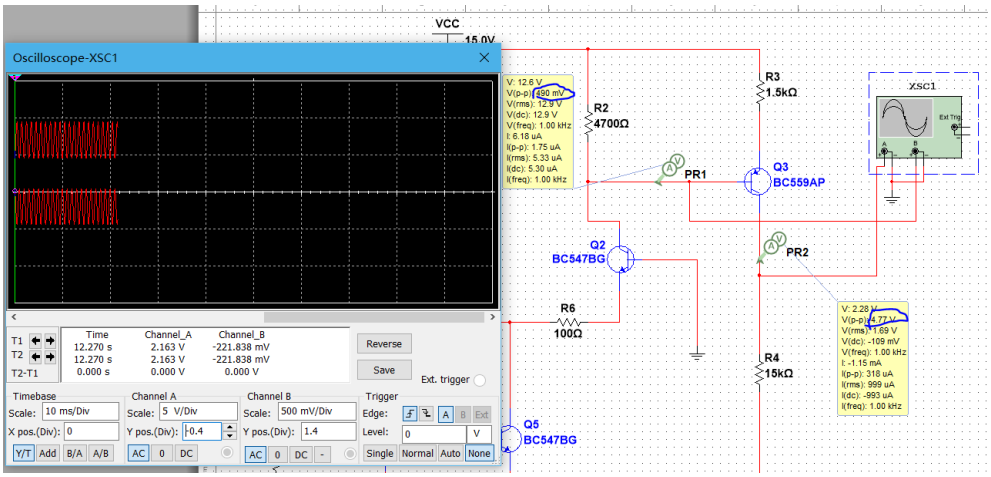


Figure 5 Gain stage (simulation)

The value I found in simulation is peak-to-peak value, so the peak value would be half of each p-p value.

$$V_{out} = 2.385V, \qquad V_{in} = 245mV$$

$$A_d = \frac{V_{out}}{V_{in}}$$

$$A_{d1} = \frac{V_{out}}{V_{in}} = \frac{2.385V}{245mV} = 9.73 = 20\log(9.73) = 19.7dB$$

Hence, the output voltage gain of the gain stage is 19.7dB.

Differential amplification stage

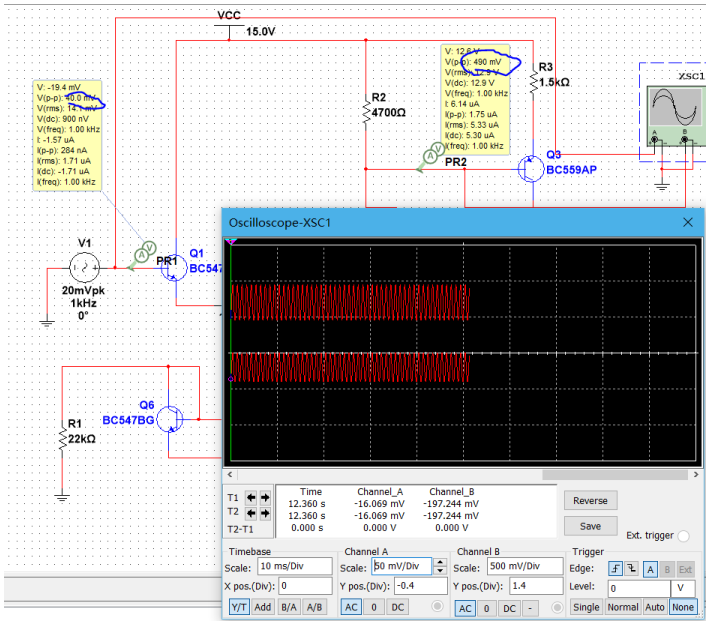


Figure 6 Differential amplification (simulation)

$$A_d = \frac{V_{od}}{V_{id}}$$

$$V_{od} = 245mV, \qquad V_{id} = 20mV$$

$$A_{d2} = \frac{V_{od}}{V_{id}} = \frac{245mV}{20mV} = 12.25 = 20\log(12.25) = 21.8dB$$

Hence, the output voltage gain of the differential amplification stage is 21.8dB.

Total voltage gain:

$$V_{out} = 2.385V, \qquad V_{in} = 20mV$$

$$A_{tot} = \frac{V_{out}}{V_{in}} = \frac{2.385V}{20mV} = 119.25 = 20log119.25 = 41.5dB$$

Hence, the total output voltage gain is 41.5 dB.

Input/Output impedance

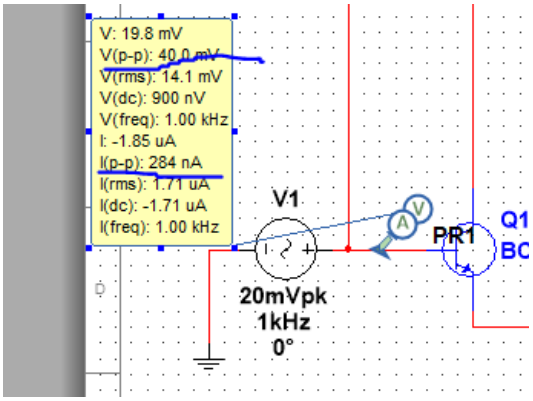


Figure 7 Input impedance

$$V_{in} = 20mV, \qquad I_{in} = 142nA$$

$$R_{in} = \frac{V_{in}}{I_{in}} = \frac{20mV}{142nA} = 0.14M\Omega$$

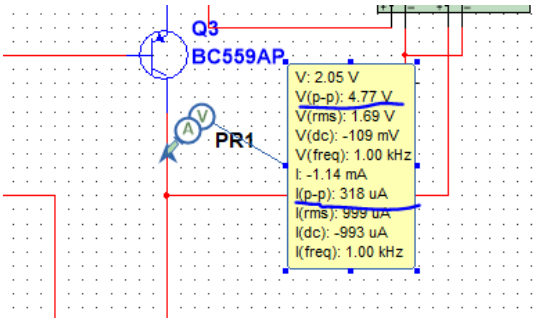


Figure 8 Output impedance

$$V_{in} = 2.385V, \qquad I_{in} = 159\mu A$$

$$R_{out} = \frac{V_{out}}{I_{out}} = \frac{2.385V}{159\mu\, A} = 15k\Omega$$

CMRR:

Common-mode gain: (when there are two voltage source connected.)

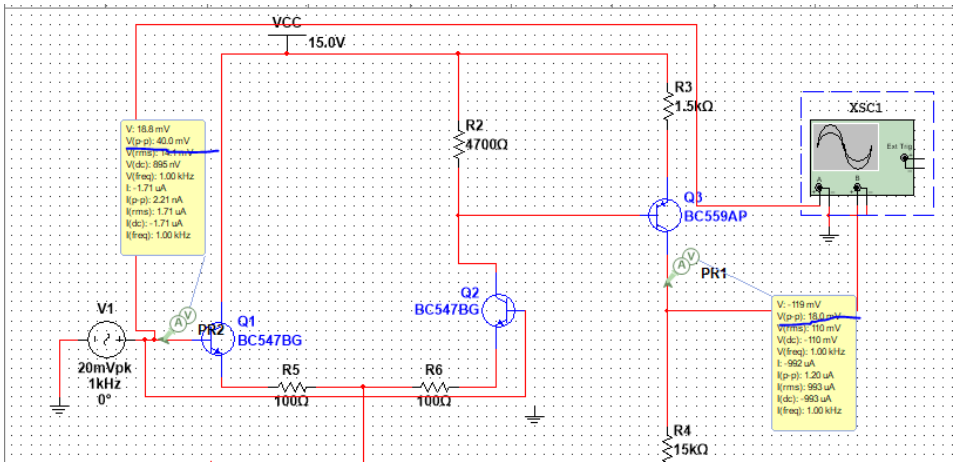


Figure 9 Common-mode gain (simulation)

In this case, $V_{in} = \frac{V_1}{2} = \frac{20mV}{2} = 10mV$

$$V_{in} = 10mV, \quad V_{out} = 9mV$$

$$A_{cm} = \frac{V_{out}}{V_{in}} = \frac{9mV}{10mV} = 0.9$$

Differential gain: (when there is only one voltage source connected.)

$$A_d = A_{tot} = A_{d1} * A_{d2} = 9.73 * 12.25 = 119.1925$$

CMRR:

$$CMRR(dB) = 20log\frac{|A_d|}{|A_{cm}|} = 20log\frac{119.1925}{0.9} = 42.44dB$$

Voltages swing:

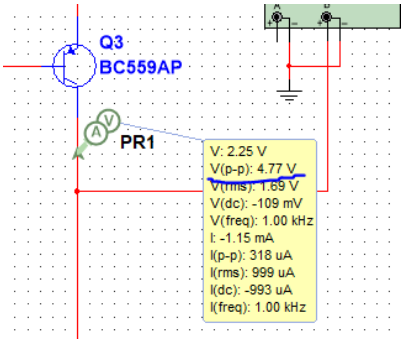


Figure 10 Voltage swing

As V_{p-p}=4.77V,

Hence, the maximum output voltage swing is from -2.385V to 2.385V.

3. Comparison:

Theoretical results

Transistor	Collector Current	Collector Voltage	Power Dissipation
Q1	325μA	15V	$5.10mW$

Q2	325μA	13.47V	$4.6mW$
Q3	-1.49mA	7.28V	$8.16mW$
Q5	-650μA	-0.67V	$9.3mW$
Q6	-650μA	-14.3V	$0.46mW$

Gain stage voltage gain	$19.9dB$
Differential amplification stage voltage gain	$22.5dB$
Total voltage gain	$42.4dB$
Input impedance	$24.7k\Omega$
Output impedance	$15k\Omega$
CMRR	∞dB
Voltages swing	-2.63V~ 2.63V

Simulation results

Transistor	Collector Current	Collector Voltage	Power Dissipation
Q1	-470μA	15V	$7.33mW$
Q2	-460μA	12.9V	$6.2mW$
Q3	-993μA	-110mV	$13.3mW$
Q5	-934μA	-644mV	$13.4mW$
Q6	-648μA	-14.4V	$0.389mW$

Gain stage voltage gain	$19.7dB$
Differential amplification stage voltage gain	$21.8dB$
Total voltage gain	$41.5dB$
Input impedance	$0.14M\Omega$
Output impedance	$15k\Omega$
CMRR	$42.44dB$
Voltages swing	-2.385V~ 2.385V

Results comparison:

	Differences		
Transistor	Collector Current	Collector Voltage	Power Dissipation
Q1	145μA	0V	$2.23mW$
Q2	135μA	0.57V	$1.6mW$
Q3	497μA	7.17V	$5.14mW$
Q5	284μA	26mV	$4.1mW$
Q6	2μA	0.1V	$0.071mW$

Results	Differences
Gain stage voltage gain	$0.2dB$
Differential amplification stage voltage gain	$0.7dB$
Total voltage gain	$0.9dB$
Input impedance	$0.12M\Omega$

Output impedance	0Ω
CMRR	∞dB
Voltages swing	0.245V

Comments on Discrepancies:

The collector current and power dissipation differences between theoretical and simulation results are quite significant, especially for Q3 and Q5. This could be due to several factors:

1. Model Accuracy: simulation models can't work 100% the same as the transistors in the real world, especially for their non-linear and thermal effects.
2. Parameter Variations: In simulation, β and V_{BE} are changing. Additionally, in the theoretical calculation, we assume the base current of each transistor is zero, but there is a base current of each transistor in the simulation.
3. Biasing Conditions: The biasing conditions between simulation and theories might differ.

Voltage Gain (Gain Stage, Differential Amplification Stage, Total Voltage Gain):

There was only a small difference among these three gains, which was caused by variation in the base current of transistors.

Input and Output Impedance:

There was a significant difference between the input impedance, because the method or assumptions used in theoretical calculations might differ from the simulation model.

CMRR (Common Mode Rejection Ratio):

The difference is infinite, because the common-mode gain is theoretically close to 0. However, in simulation, we can find the actual common-mode gain, which will cause a significant difference in CMRR.

Voltage Swing:

The little difference could be also due to variations in the base current of transistors.

Section 3: Improved op-amp design[1]

1. Design improved op-amp circuit

Differential amplification stage:

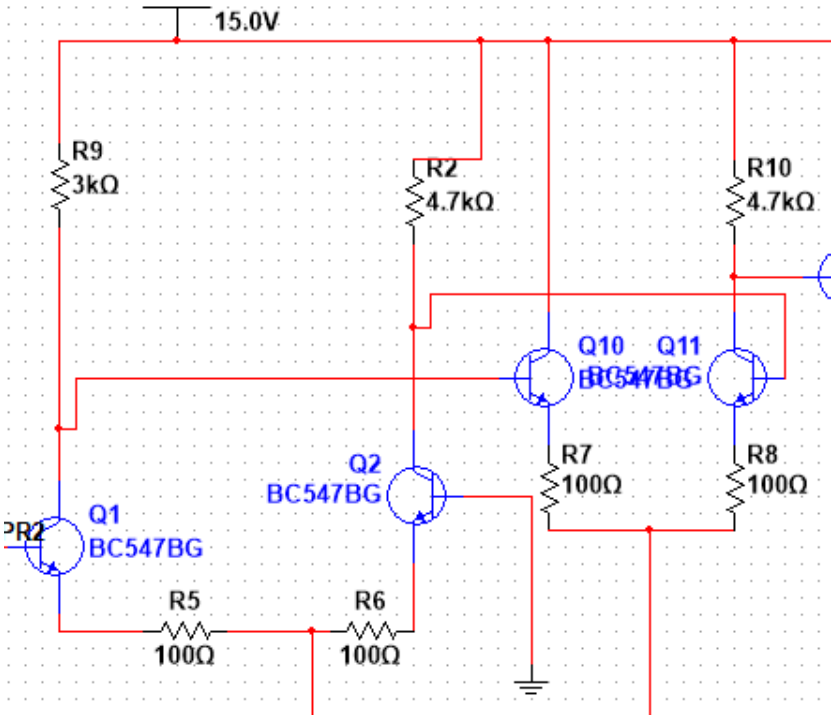


Figure 11 Schematic of Differential amplification stage

I used cascaded differential amplifiers to increase the voltage gain and CMRR in this stage. Also, it can significantly increase the input impedance.

The resistors in cascaded differential amplifiers are essential for setting up biasing conditions, determining gain, and protecting the circuit.

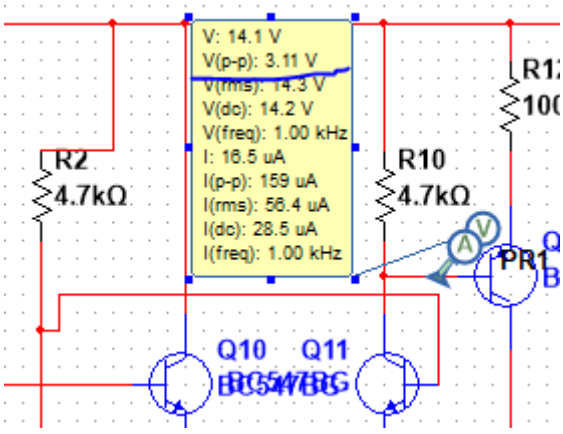


Figure 12 Output of differential amplification stage

As we can see, $V_{out} = 1.555V$

$$A_{d1} = \frac{V_{out}}{V_{in}} = \frac{1.555V}{20mV} = 77.75 = 20\log(77.75) = 37.8dB$$

The voltage gain of the differential amplification stage is 37.8 dB, which means the

cascaded differential amplifiers will work well in the improved design.

DC level shifting stage:

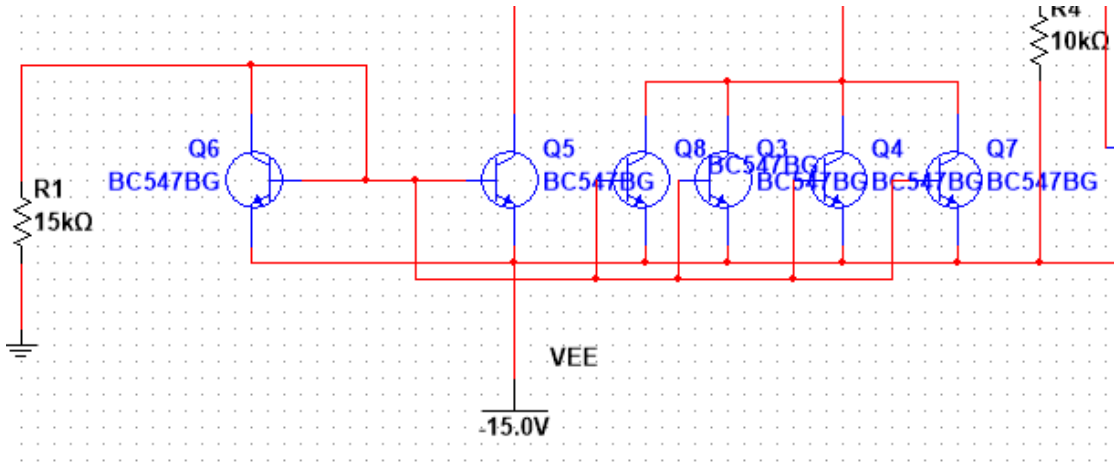


Figure 13 Schematic of DC level shifting stage

I used the current steering approach along with the current mirror to provide stable bias currents to various parts of the whole analogue circuit, which can also help the circuit achieve higher voltage gain and input/output impedance.

Gain stage:

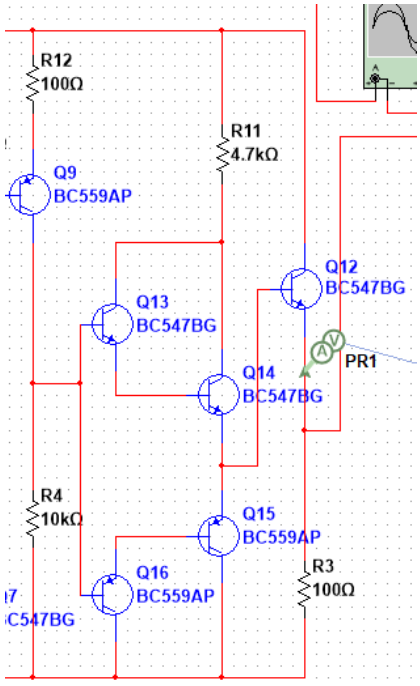


Figure 14 Schematic of Gain stage

I used the Darlington Pair in the output stage to bring higher input impedance for the whole circuit. Also, one more NPN BJT Q12 is connected with the output part of the Darlington Pair, which will eventually amplify the output voltage of the whole circuit.

The value of the R3 is the same as the output impedance, I set it to 100 ohms to satisfy the ideal result.

2. NI MultiSim schematic of improved design of op-amp circuit

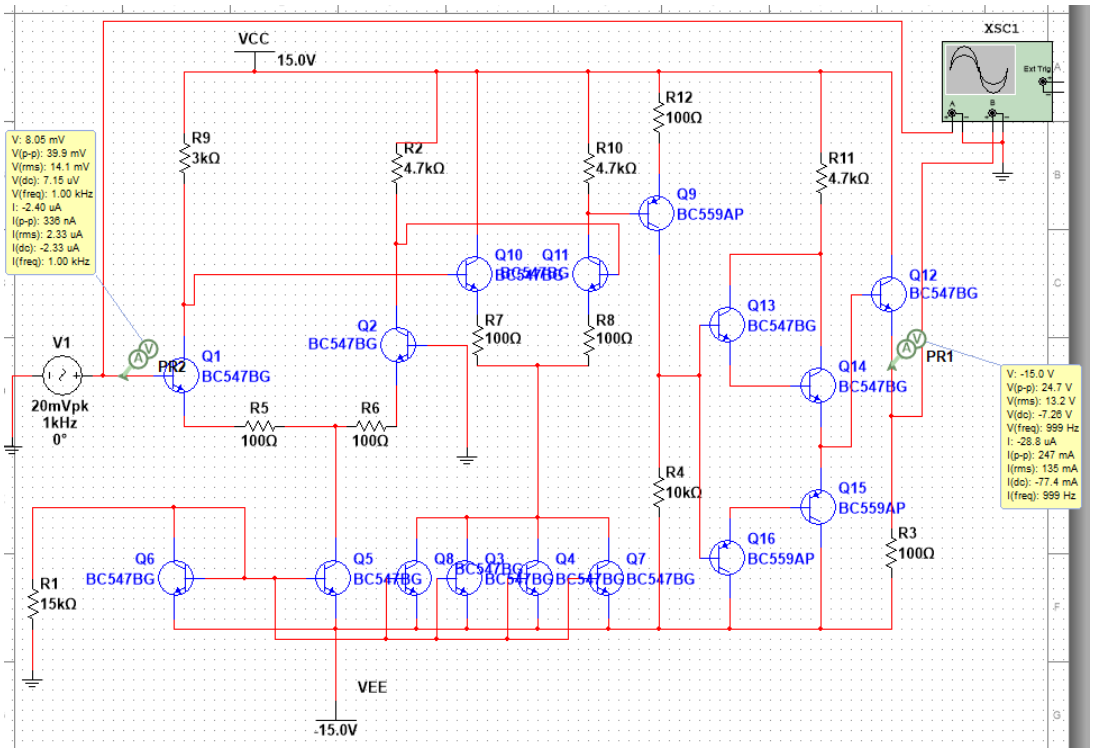


Figure 15 NI MultiSim schematic of improved design of op-amp circuit

3. AC characteristics of the given op-amp circuit

Total voltage gain:

$$V_{in} = 20mV, \qquad V_{out} = 12.35V$$

$$A_d = A_{tot} = \frac{V_{out}}{V_{in}} = \frac{12.35V}{20mV} = 617.5 = 20log617.5 = 55.8dB$$

Input and output impedance:

$$V_{in} = 20mV, \qquad I_{in} = 168.5nA$$

$$R_{in} = \frac{V_{in}}{I_{in}} = \frac{20mV}{168.5nA} = 0.12M\Omega$$

$$V_{out} = 24.7V, \qquad I_{out} = 247m\,A$$

$$R_{out} = \frac{V_{out}}{I_{out}} = \frac{24.7V}{247m\,A} = 100\Omega$$

CMRR:

Common-mode gain: (when there are two voltage sources connected.)

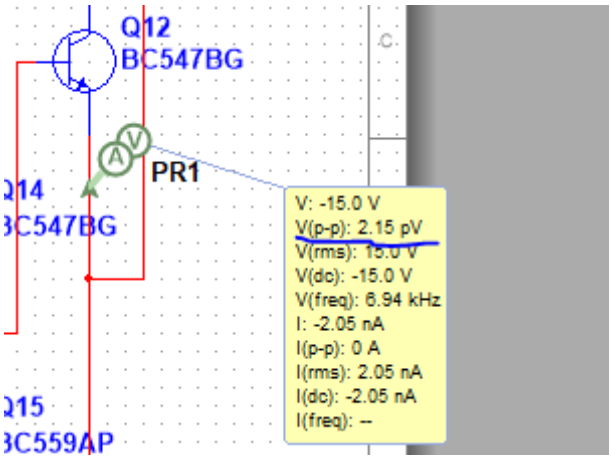


Figure 16 Common-mode gain

$$V_{in} = 10mV, \qquad V_{out} = 1.075pV$$

$$A_{cm} = \frac{V_{out}}{V_{in}} = \frac{1.075pV}{10mV} = 1.075 * 10^{-10} = -199.4dB$$

$$CMRR(dB) = 20log\frac{|A_d|}{|A_{cm}|} = 20log\frac{617.5}{1.075 * 10^{-10}} = 255.2dB$$

Hence, the improved values are shown below:

$$R_{in} = 0.12M\Omega$$
$$R_{out} = 100\Omega$$
$$A_{tot} = 617.5 = 55.8dB$$
$$A_{CM} = 1.075 * 10^{-10} = -199.4dB$$
$$CMRR(dB) = 255.2dB$$

Comparison with ideal results:

	Improved results	Ideal results
Input impedance	$0.12M\Omega$	$M\Omega$
Output impedance	100Ω	$10 - 100\Omega$
Total voltage gain	$55.8dB$	$> 100dB$
CMRR	$255.2dB$	$> 100dB$

By comparison, except for the total voltage gain, the results of the improved design circuit were relatively great.

Section 4:Conclusions and future work

Conclusions:

After completing this assignment, I have a deep understanding of analyzing, measuring, and designing operational amplifiers (op-amps). Also, my simulation skill in NI multisim software is significantly developed, which allows me to understand the practical aspects of op-amp behaviour. Additionally, during improved design, by using current mirrors, cascaded differential amplifiers and Darlington pairs, my design skills and understanding of how different configurations affect an op-amp's performance were enhanced as well, although I didn't get the perfect results.

Future work:

Because I didn't get the perfect results in improved design this time, I will investigate more complex op-amp configurations to find better design and results. Explore how analogue systems like op-amps can be integrated with digital systems. This includes studying analogue-to-digital (ADC) and digital-to-analogue (DAC) converters and understanding the challenges in mixed-signal environments.

References:

[1] Adel S. Sedra. (2015). Microelectronic Circuits (7th ed.). Oxford University Press.