Architecture: 68K

Key characteristics:

- 24 bit address bus, 16 bit data bus
- 2 Privilege mode:
  - Supervisor: All instructions can be executed, used for OS
  - User: Can't execute 'privileged instructions', used for app
- Registers:
  - Data registers: eight 32-bit data registers: D0, D1, ..., D7 | Store any data

D0.B: 8 Least significant bits of D0
D0.W: 16 " " " " " "
D0.L: 32 (all) bits of D0

  - Address registers: eight 32-bit address registers: A0, A1, ..., A7 | Store addresses

⚠ A0.B doesn't exist. Only .W and .L

- 2 stack pointers, 32-bit long

SSP when in supervisor mode

USP when in user mode

- Program counter, 32 bit register, holds the next instruction.

- Status register: 16 bit register

Condition Code Register

- C: Carry, 1 if unsigned overflow
- V: OverFlow, 1 if signed overflow
- Z: Zero, 1 if result is null
- N: Negative, is equal to the MSB of the result.
- X: Extend, same as C

CCR are the eight LSB of the SR

- S: 1 if Supervisor state is active

⚠ Each bits of the SR are referred to as **Flags**

Examples:

Positive + Positive = Negative } V=1
Negative + Negative = Positive }

1111 + 0001 = 10000 } C=1, X=C

1001+0111 } Z=1 ; 01011000 } Z=0