Report: Summer Internship 2014
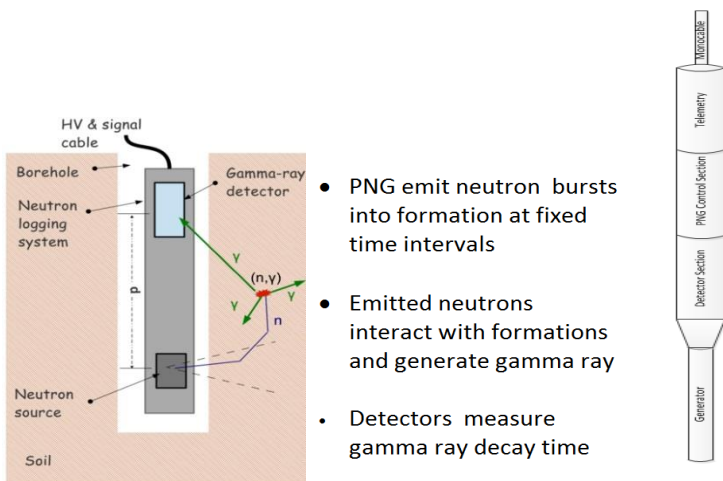Company: C&J Energy Services
Department: Research and Technology
Title: Firmware Engineer Intern
Manager: Dalong Zhang

I have worked on 2 projects at C&J Energy Services in the Research and Technology department. The Electrical Engineering team is working on the Pulsed Neutron Tool (PNT). And I was assigned to develop firmware for this tool.

Operation Principle and PNT Layout

- PNG emit neutron bursts into formation at fixed time intervals

- Emitted neutrons interact with formations and generate gamma ray

- Detectors measure gamma ray decay time

Developed Firmware for the DPC board of the PNT

DIGITAL PROCESSING CONTROLLER BOARD
(DPC)

microcontroller
dsPIC33FJ256MC710A

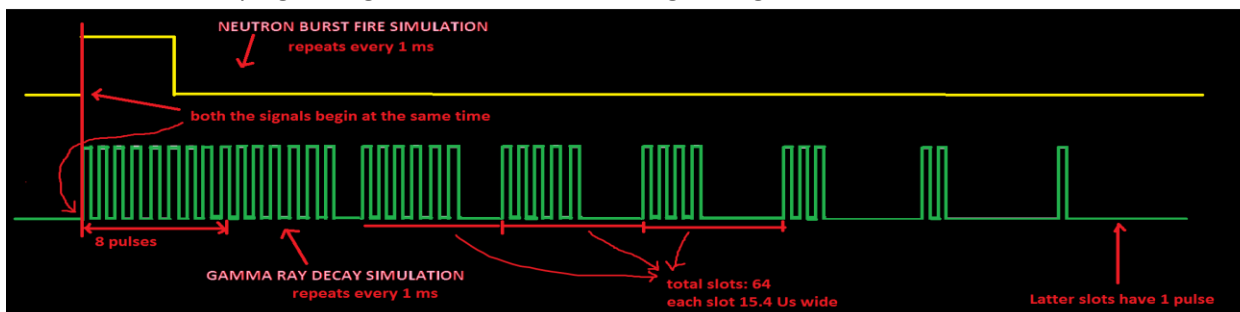FPGA by Actel
AGL250V2VQ100

Project 1: Firmware Development for the detector section of the PNT
Objective: Verify synchronization of the generator and detector in the PNT
Strategy: develop 2 simulative signals for the neutron bursts firing and the gamma ray count decaying.
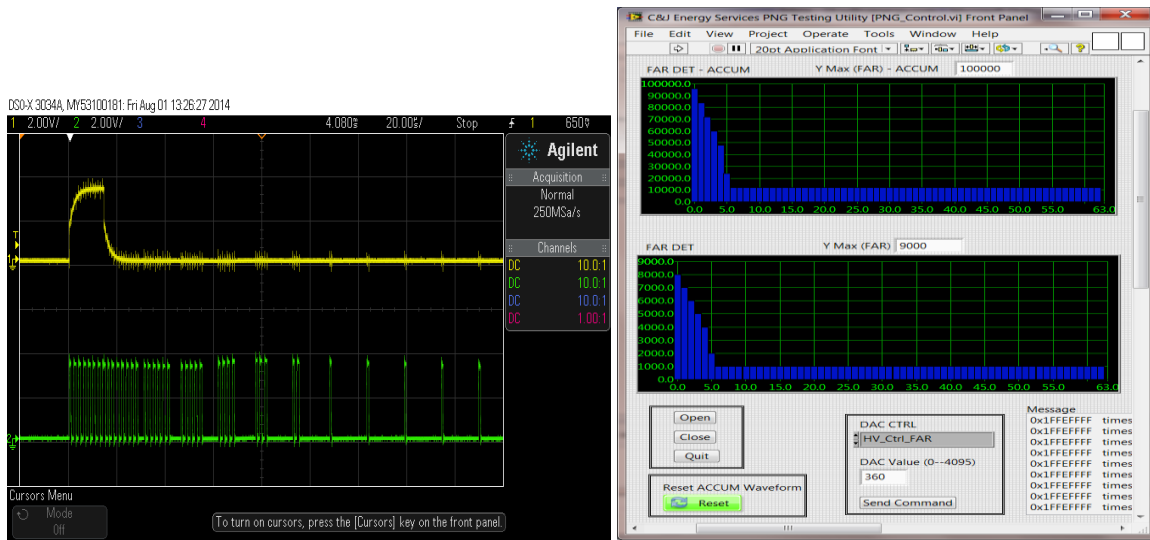Used PIC for developing the signals and FPGA for routing the signals

Results:

Picture 1: Signals captured on the oscilloscope

Picture 2: Test results on testing the PNT Detector DPC

Conclusion: completed the project in 2 weeks. Real measurements at the C&J labs and Thermo Fisher labs for water and concrete formations have yielded accurate results. The firmware will be used by C&J for testing the electronic boards once manufacturing starts

Project 2: Firmware development for the Telemetry section of the PNT

Objective: Make PNT compatible with Probe© tools.

Strategy:

Divide the project in 2 parts. First implement the Probe PTX telmetry Scheme and next implement the Porbe Message Protocol.
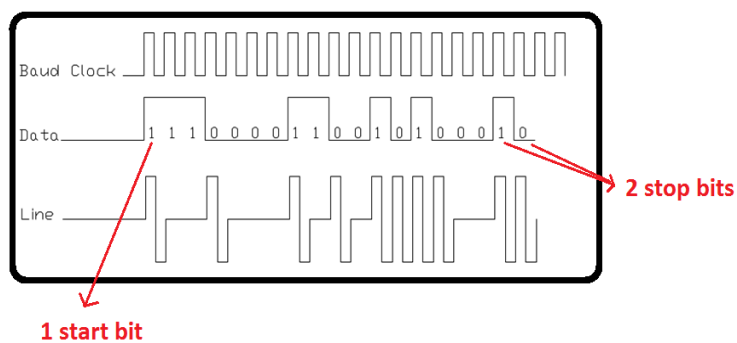
Probe PTX Telemetry Scheme

- Generate data using PIC. Send data via SPI bus to FPGA. FPGA generates 2 signals for driving the gates of drive circuitry which generates Probe compatible signal.
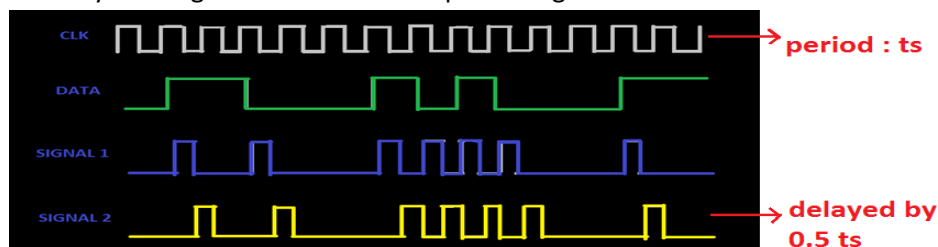
Results:

Data and FPGA signals captured on the oscilloscope
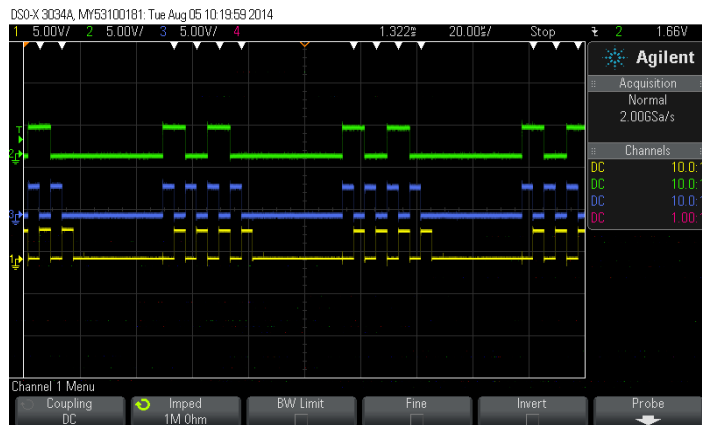
Probe's Message Protocol implemented in PIC.

Additionally, developed a virtual instrument in LabVIEW so that user can send the data he wishes to send. PIC receives this data via UART.

Conclusion: Working on the project since 4 weeks. Next step is appending start bits and stop bits. Also working on the driver circuitry.

Challenges:

Programming the FPGA chip.

Developing a VI in LabVIEW.

Timing accuracy of the signals in project 1.

Achievements:

Received the award for Best Summer Intern 2014 in the 2nd place.