# PCI Bus & Devices

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# 32-bit PCI connector pinout – Part 1

| Pin | Side B | Side A | Comments |
|---|---|---|---|
| 1 | −12 V | TRST# | JTAG port pins (optional) |
| 2 | TCK | +12 V | |
| 3 | Ground | TMS | |
| 4 | TDO | TDI | |
| 5 | +5 V | +5 V | |
| 6 | +5 V | INTA# | Interrupt pins (open-drain) |
| 7 | INTB# | INTC# | |
| 8 | INTD# | +5 V | |
| 9 | PRSNT1# | Reserved | Pulled low to indicate 7.5 or 25 W power required |
| 10 | Reserved | IOPWR | +5 V or +3.3 V |
| 11 | PRSNT2# | Reserved | Pulled low to indicate 7.5 or 15 W power required |
| 12 | Ground | Ground | Key notch for 3.3 V-capable cards |
| 13 | Ground | Ground | |
| 14 | Reserved | 3.3 V aux | Standby power (optional) |
| 15 | Ground | RST# | Bus reset |
| 16 | CLK | IOPWR | 33/66 MHz clock |
| 17 | Ground | GNT# | Bus grant from motherboard to card |
| 18 | REQ# | Ground | Bus request from card to motherboard |
| 19 | IOPWR | PME# | Power management event (optional) 3.3 V, open drain, active low.[19] |

# 32-bit PCI connector pinout – Part 2

| | | | |
|---|---|---|---|
| 20 | AD[31] | AD[30] | Address/data bus (upper half) |
| 21 | AD[29] | +3.3 V | |
| 22 | Ground | AD[28] | |
| 23 | AD[27] | AD[26] | |
| 24 | AD[25] | Ground | |
| 25 | +3.3 V | AD[24] | |
| 26 | C/BE[3]# | IDSEL | |
| 27 | AD[23] | +3.3 V | |
| 28 | Ground | AD[22] | |
| 29 | AD[21] | AD[20] | |
| 30 | AD[19] | Ground | |
| 31 | +3.3 V | AD[18] | |
| 32 | AD[17] | AD[16] | |
| 33 | C/BE[2]# | +3.3 V | |

# 32-bit PCI connector pinout – Part 3

| | | | | |
|---|---|---|---|---|
| 34 | Ground | | FRAME# | Bus transfer in progress |
| 35 | IRDY# | | Ground | Initiator ready |
| 36 | +3.3 V | | TRDY# | Target ready |
| 37 | DEVSEL# | | Ground | Target selected |
| 38 | PCIXCAP | Ground | STOP# | PCI-X capable; Target requests halt |
| 39 | LOCK# | | +3.3 V | Locked transaction |
| 40 | PERR# | | SMBCLK | *SDONE* | Parity error; SM Bus clock or *Snoop done (obsolete)* |
| 41 | +3.3 V | | SMBDAT | *SBO#* | SMBus data or *Snoop backoff (obsolete)* |
| 42 | SERR# | | Ground | System error |
| 43 | +3.3 V | | PAR | Even parity over AD[31:00] and C/BE[3:0]# |

# 32-bit PCI connector pinout – Part 4

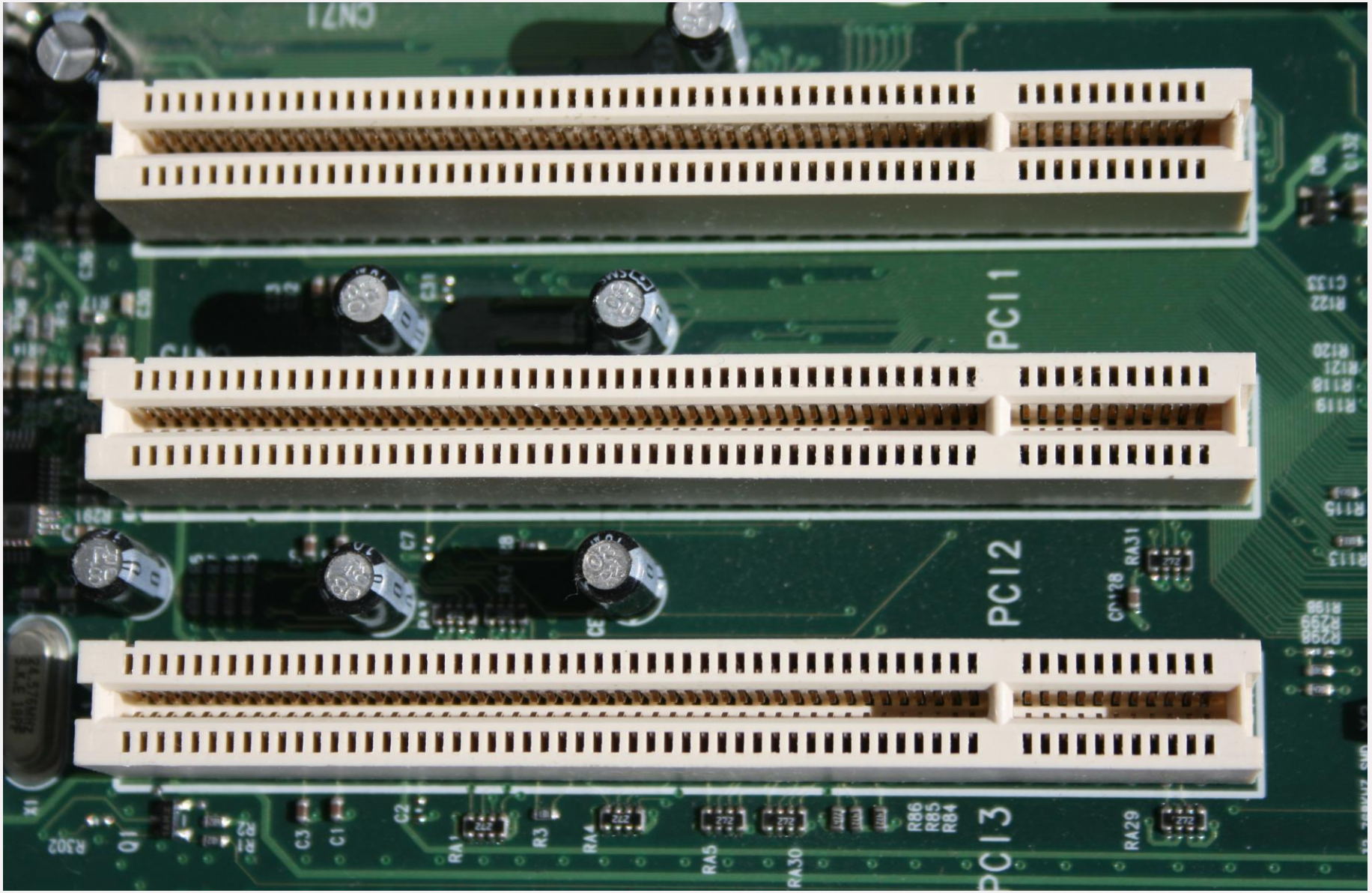
| | | | |
|---|---|---|---|
| 44 | C/BE[1]# | AD[15] | Address/data bus (higher half) |
| 45 | AD[14] | +3.3 V | |
| 46 | Ground | AD[13] | |
| 47 | AD[12] | AD[11] | |
| 48 | AD[10] | Ground | |
| 49 | M66EN / Ground | AD[09] | |
| 50 | Ground | Ground | Key notch for 5 V-capable cards |
| 51 | Ground | Ground | |
| 52 | AD[08] | C/BE[0]# | Address/data bus (lower half) |
| 53 | AD[07] | +3.3 V | |
| 54 | +3.3 V | AD[06] | |
| 55 | AD[05] | AD[04] | |
| 56 | AD[03] | Ground | |
| 57 | Ground | AD[02] | |
| 58 | AD[01] | AD[00] | |
| 59 | IOPWR | IOPWR | |
| 60 | ACK64# | REQ64# | For 64-bit extension; no connect for 32-bit devices. |
| 61 | +5 V | +5 V | |
| 62 | +5 V | +5 V | |

# 32-bit PCI connector pinout – Legend

| | |
|---|---|
| Ground pin | Zero volt reference |
| Power pin | Supplies power to the PCI card |
| Output pin | Driven by the PCI card, received by the motherboard |
| Initiator output | Driven by the master/initiator, received by the target |
| I/O signal | May be driven by initiator or target, depending on operation |
| Target output | Driven by the target, received by the initiator/master |
| Input | Driven by the motherboard, received by the PCI card |
| Open drain | May be pulled low and/or sensed by multiple cards |
| Reserved | Not presently used, do not connect |

# PCI Card (PCI Slave Device – for Desktops)

# Host PCI Slots (On Desktops)



# Mini PCI Card (For Laptops)

# Mini PCI Slots (On Laptops)

# PCI Bus Architecture - 1

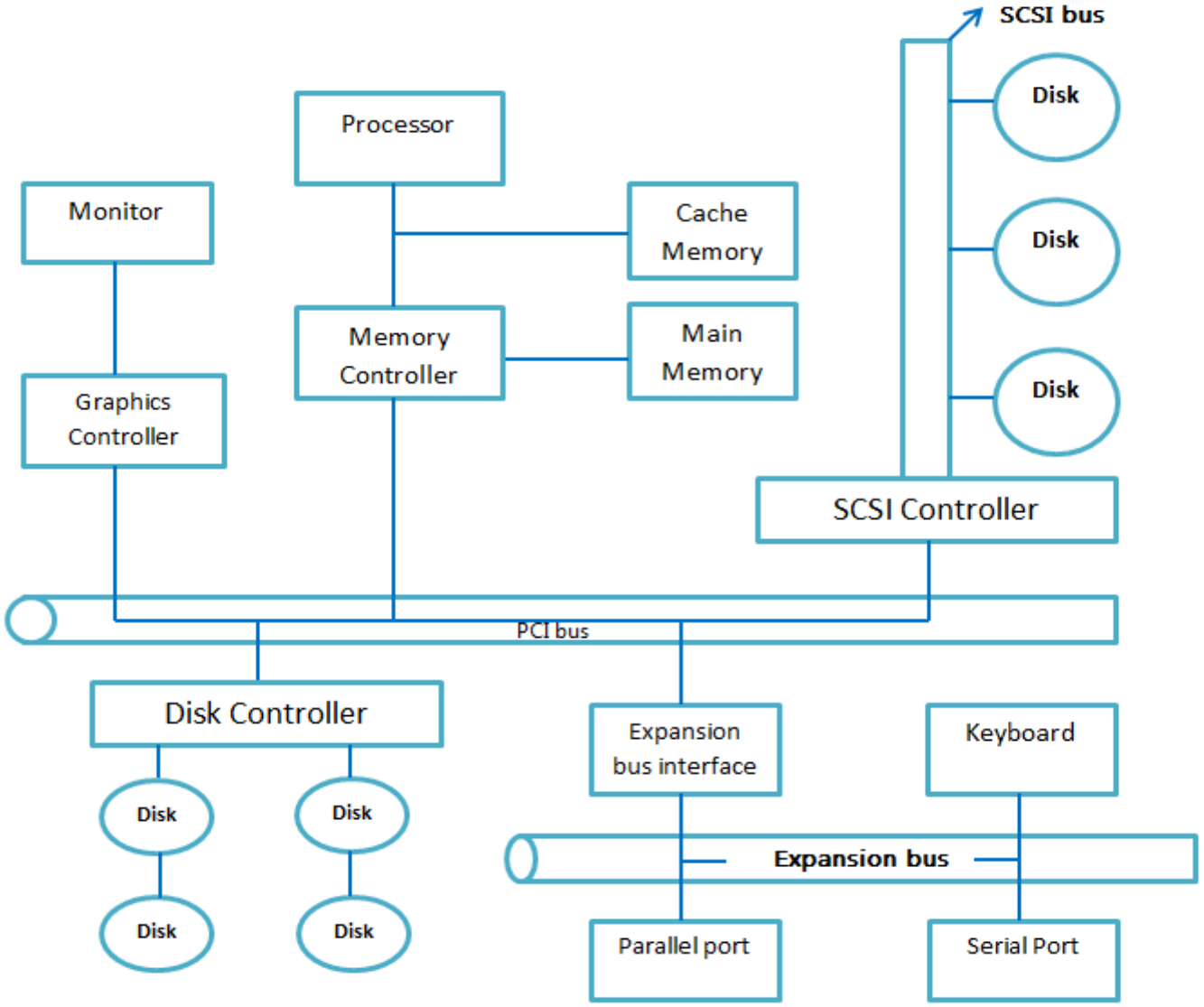
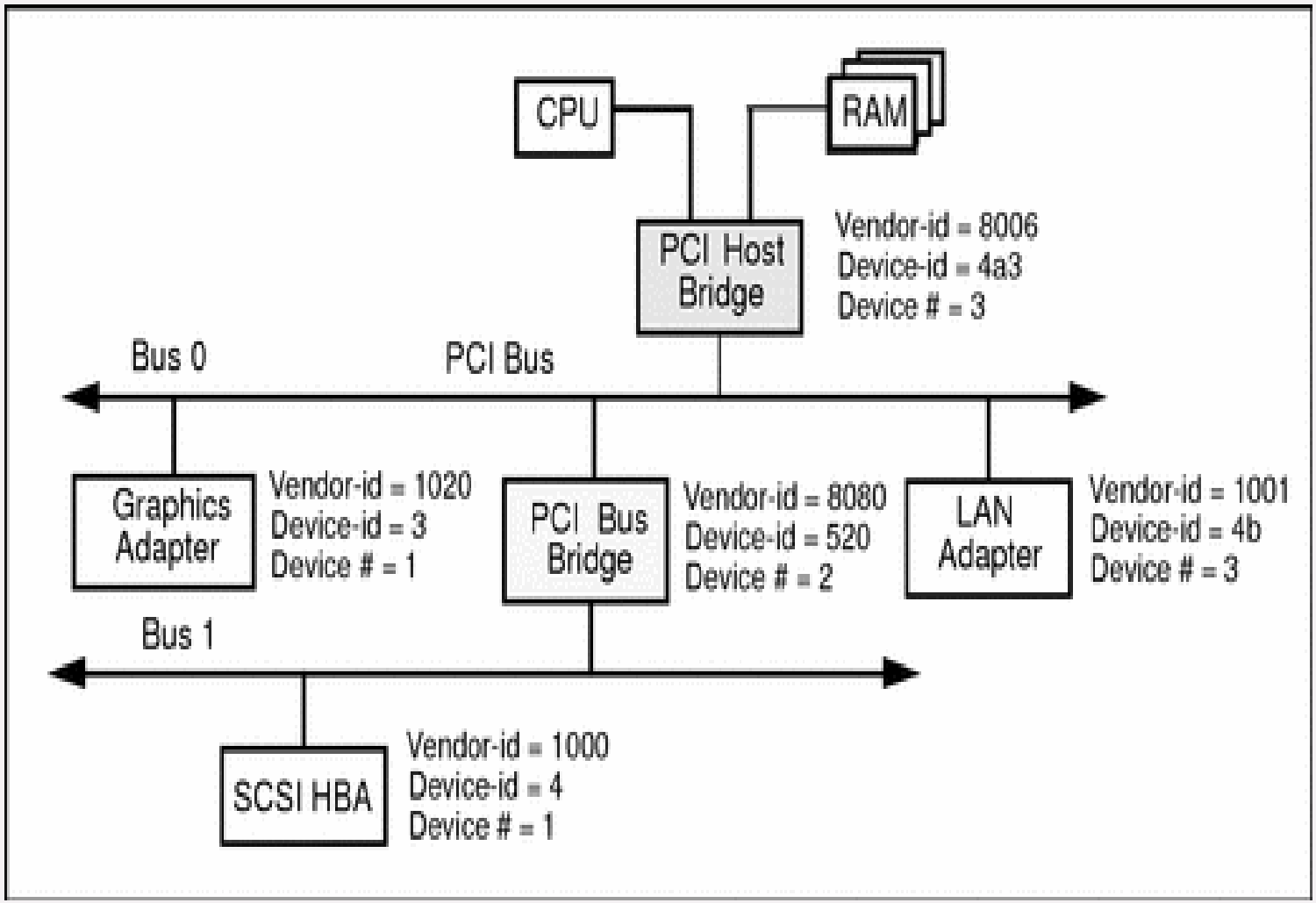
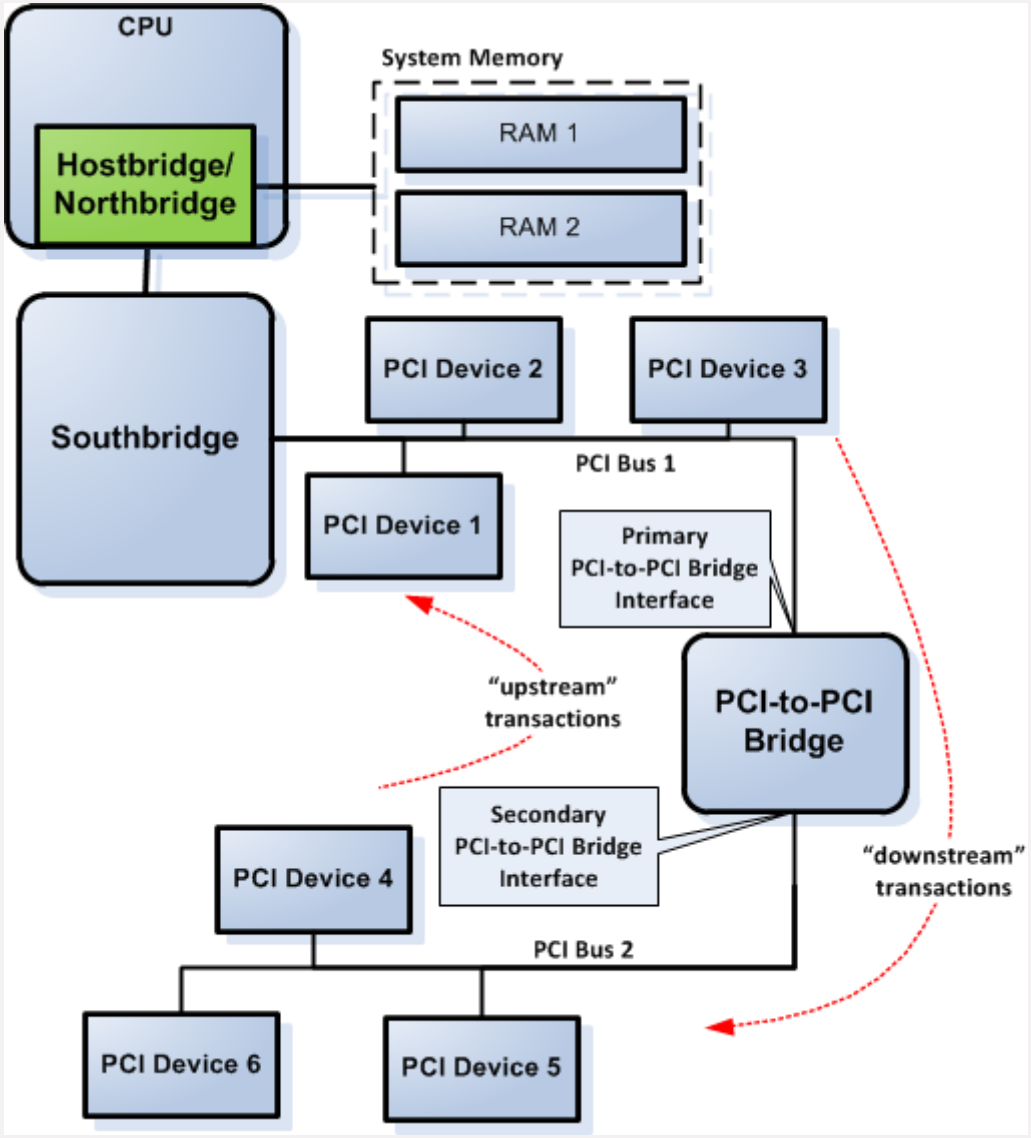



Fig: PCI Bus Architecture

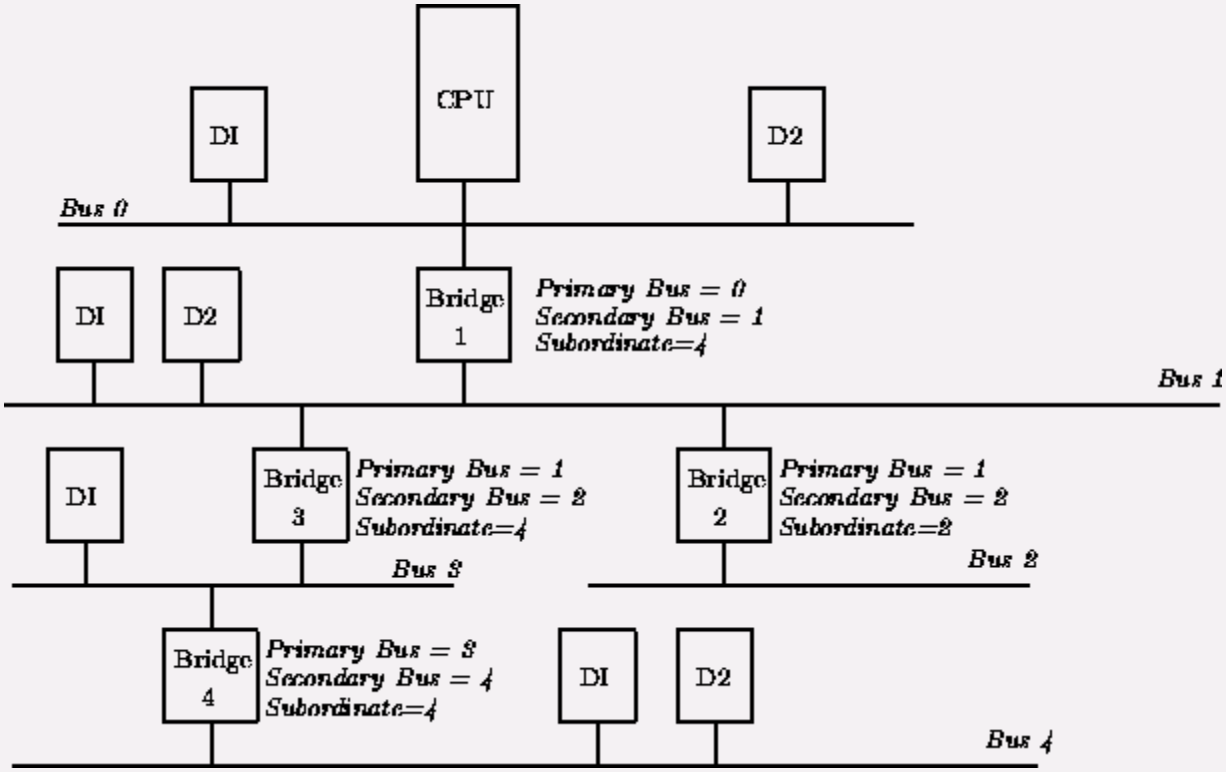
# PCI Bus Architecture - 2



# PCI Bus Architecture - 3



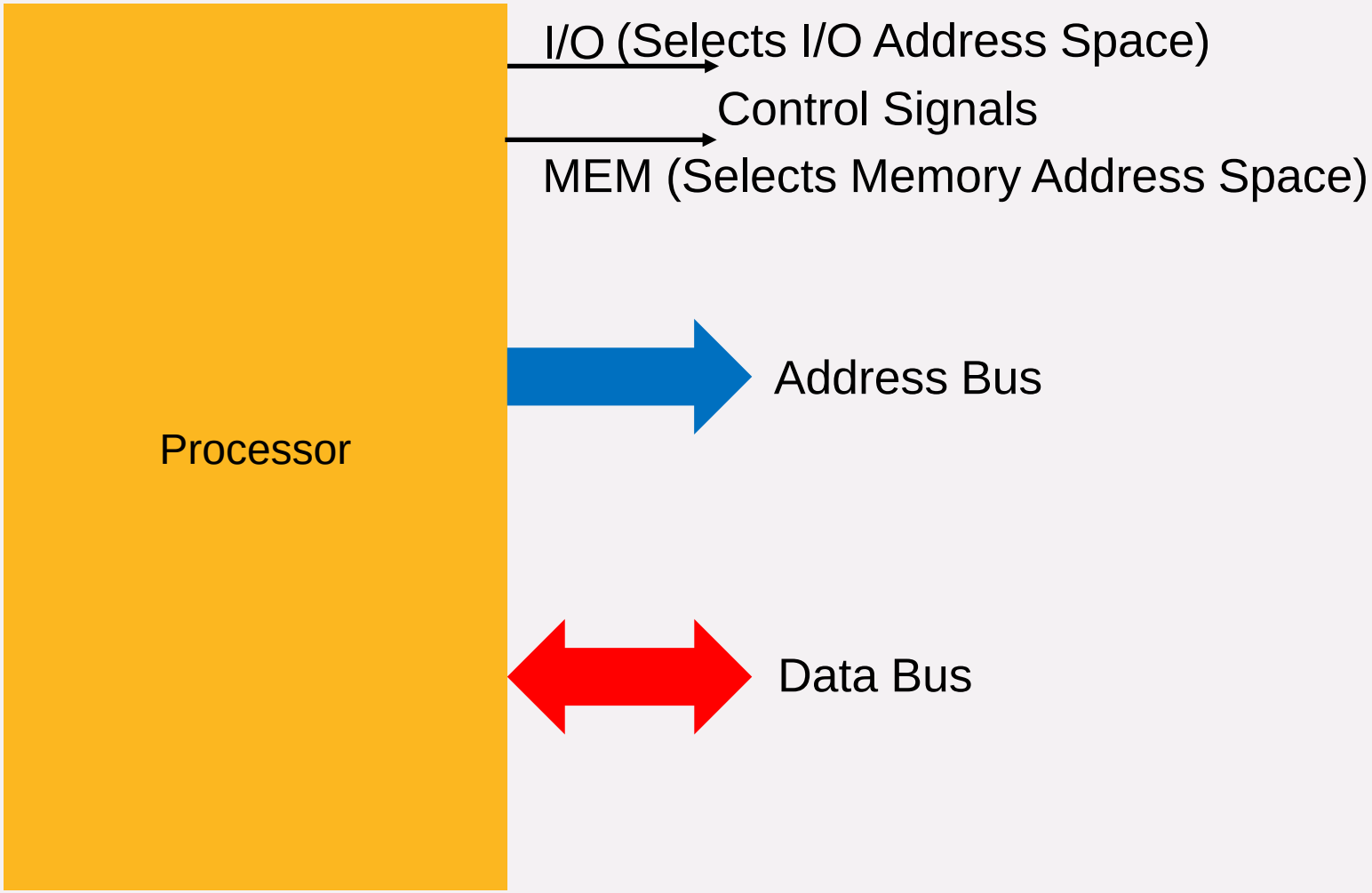
# PCI Bus Architecture - 4



# Processor Address Spaces

- Processor Memory Address Space
- Processor I/O Address Space

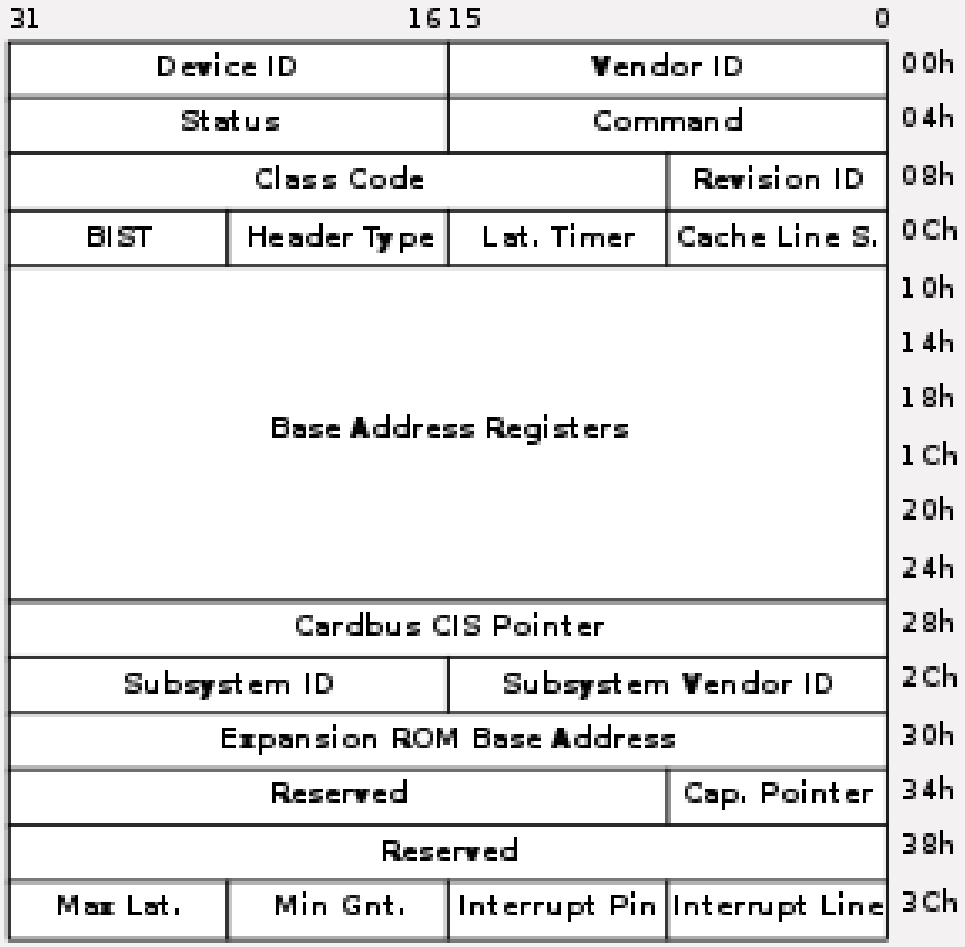
# Processor Address Space Selection



# PCI Address Spaces

- PCI Memory Address Space
- PCI I/O Address Space
- PCI Configuration Space

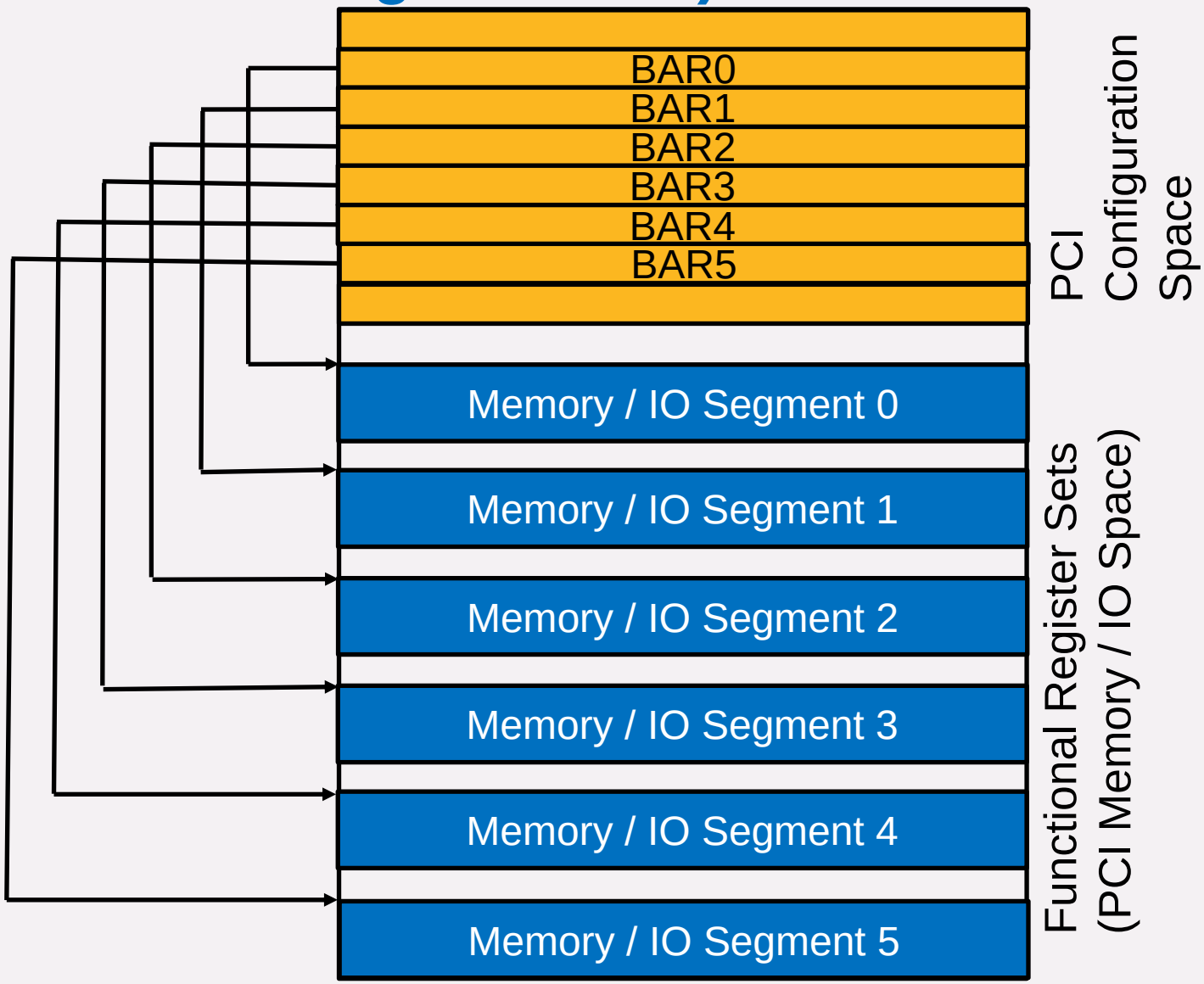
# PCI Configuration Space



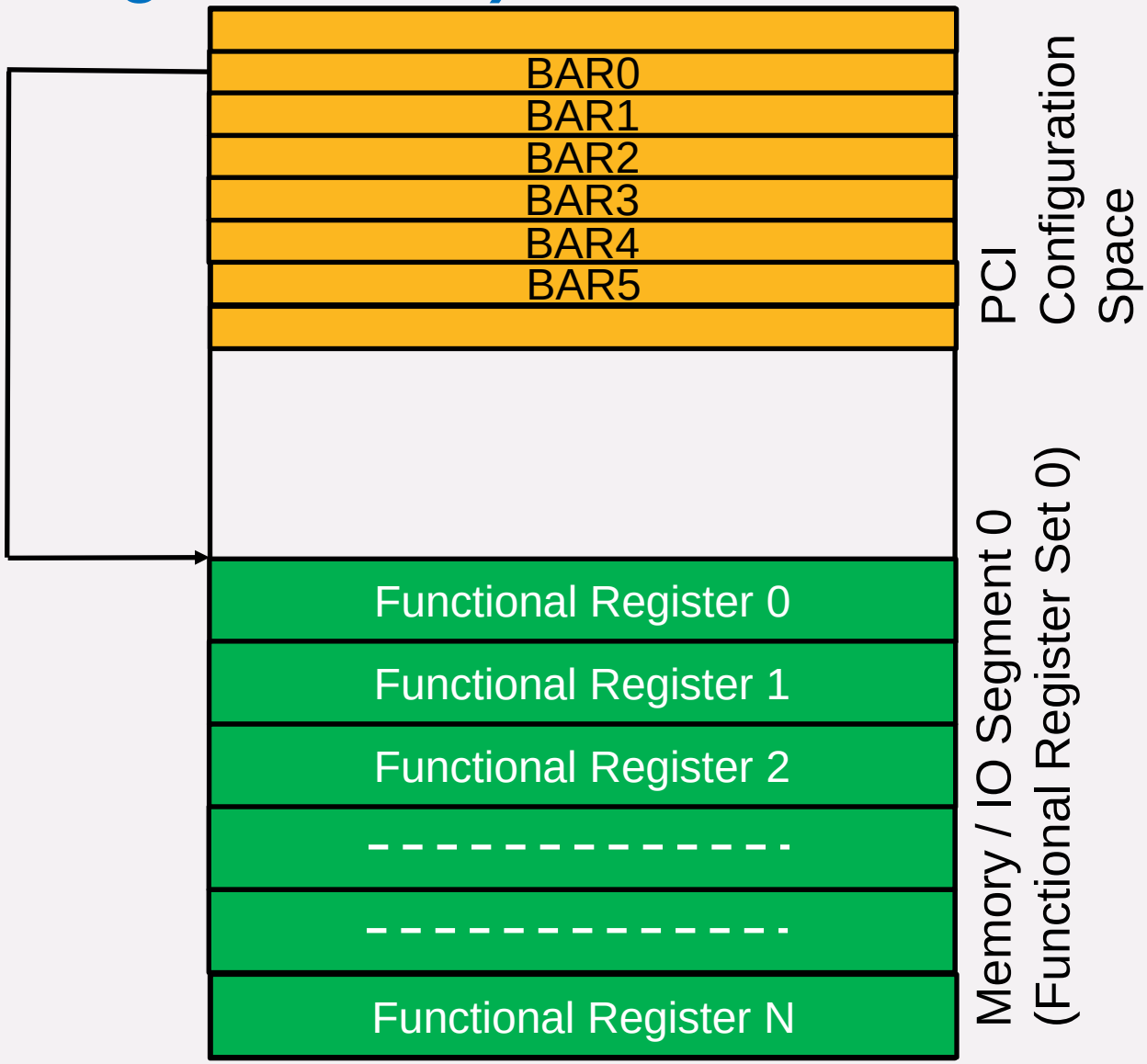
# PCI Config Space – Base Address Register (BAR)

| Bits | Description | Values |
|---|---|---|
| *For all PCI BARs* | | |
| 0 | Region Type | 0 = Memory<br>1 = I/O |
| *For Memory BARs* | | |
| 2-1 | Locatable | 0 = any 32-bit<br>1 = < 1 MB<br>2 = any 64-bit |
| 3 | Prefetchable | 0 = no<br>1 = yes |
| 31-4 | Base Address | naturally 16-byte aligned |
| *For I/O BARs* | | |
| 1 | Reserved | |
| 31-2 | Base Address | naturally 4-byte aligned |

# PCI Config Space & Memory / IO Segments (Functional Register Sets)



# PCI Config Space & Memory / IO Segment 0 (Functional Register Set 0)



# PCI References

1) https://en.wikipedia.org/wiki/Peripheral_Component_Interconnect

2) https://en.wikipedia.org/wiki/PCI_configuration_space