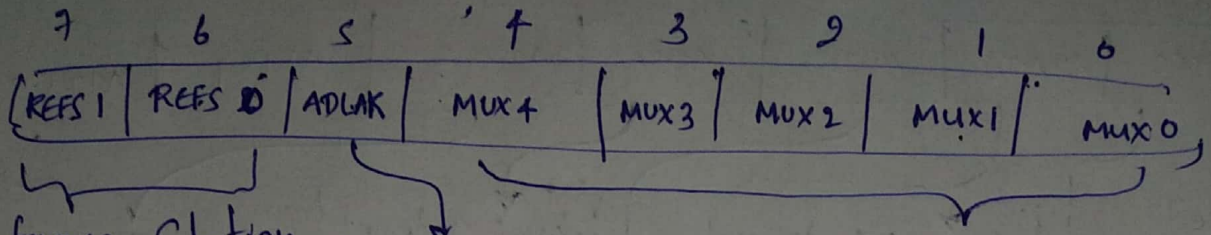
ADMUX Register



Reference Selection (Voltage for ADC)

00 → our own voltage

01 → Vcc +5V with capasitor.

10 → Reserved

11 → 2.56 with capasitor.

- AREF
- GND
- AVCC

} voltage for ADC

ADC left Adjust Result

if we want → 1

Pin selection, (Analog channel and Gain channel.)

00000 → ADC 0
00001 → ADC 1
⋮
00111 → ADC 7
are only use above

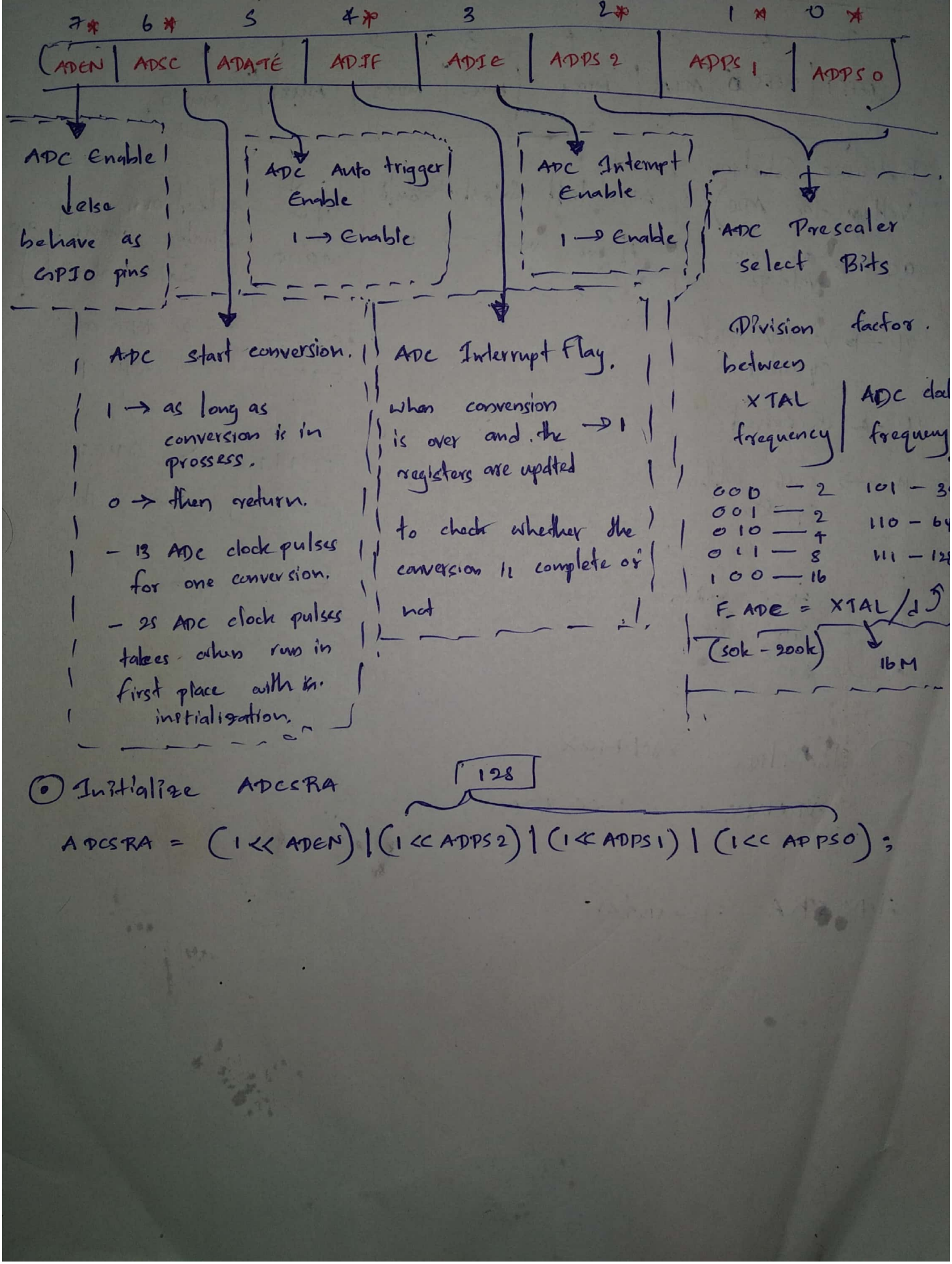
---

① Initialize ADMUX

ADMUX = (1 << REFS0)

ADCSRA Register

ADCSRA Register



⊙ Initialize ADCSRA

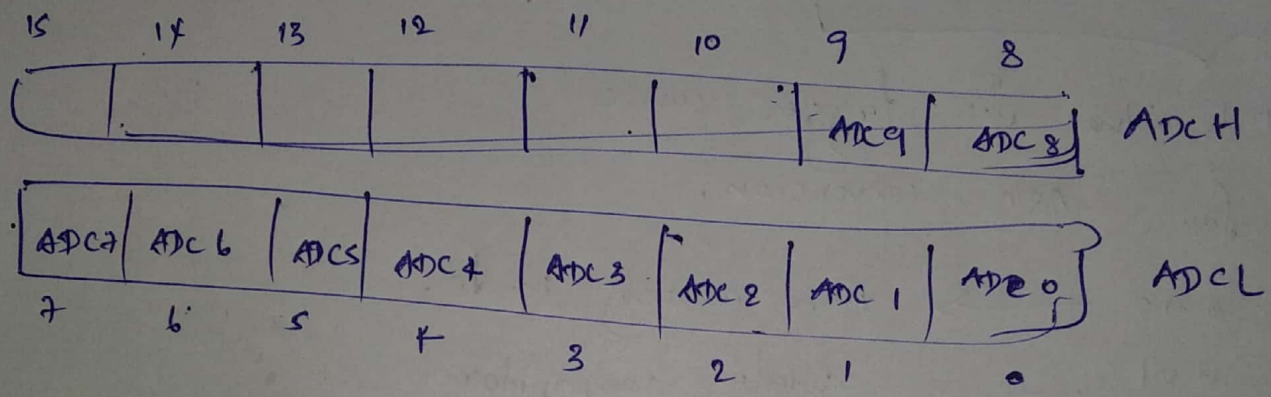
128

```
ADCSRA = (1 << ADEN) | (1 << ADPS2) | (1 << ADPS1) | (1 << ADPS0);
```

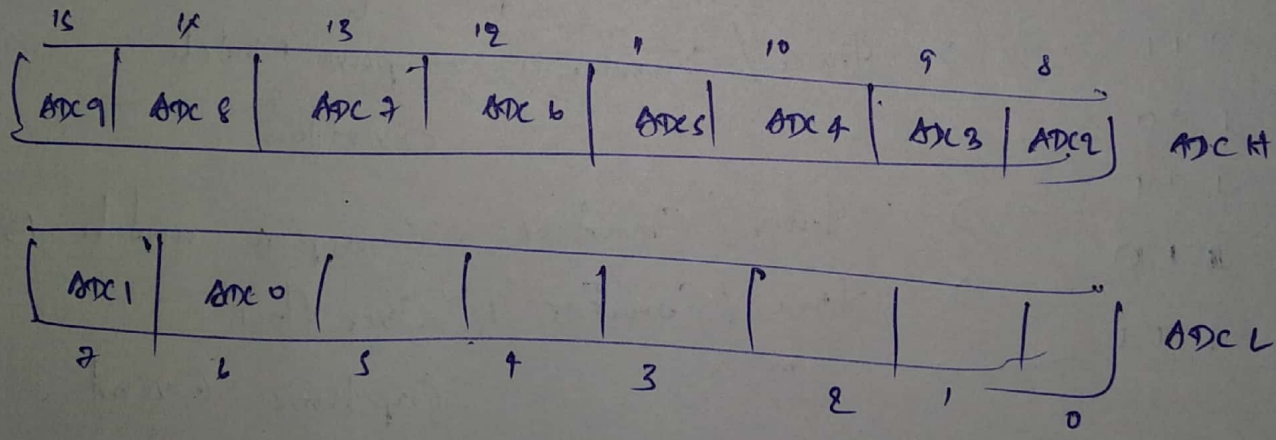
ADCL and ADCH Registers

ADC needs 10 bits to represent the value. but we only have 8 bits registers. thus we need two registers.

When ADCAR = 0

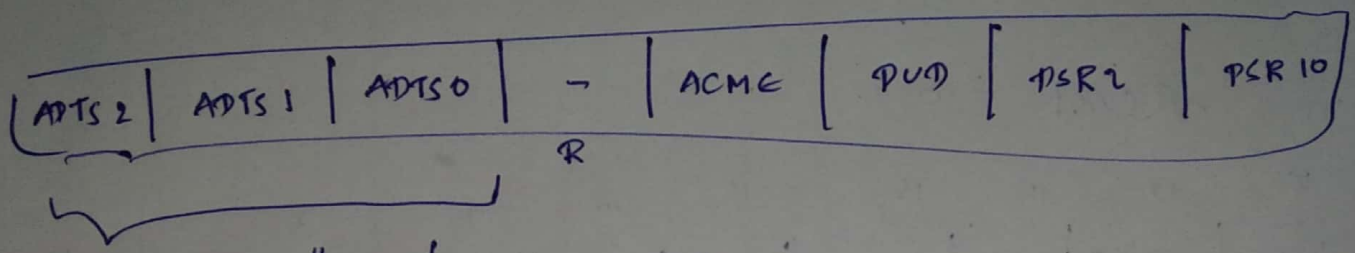


when ADCAR = 1



SFIOR Register

This register only works when ADATE = 1



Determine the trigger source for ADC conversion.

000 → Free running mode.
001 → Analog comparator
010 → External Interrupt Request 0
011 → Timer/Counter 0 compare Match
100 → " Overflow
101 → Timer/Counter Compare match B
110 → Time/Counter 1 Over flow
111 → " Capture Event