CS221 HW_Lab Report

Name : Kartik Disawal

Roll number: 2003119

Branch : Computer Science and Engineering

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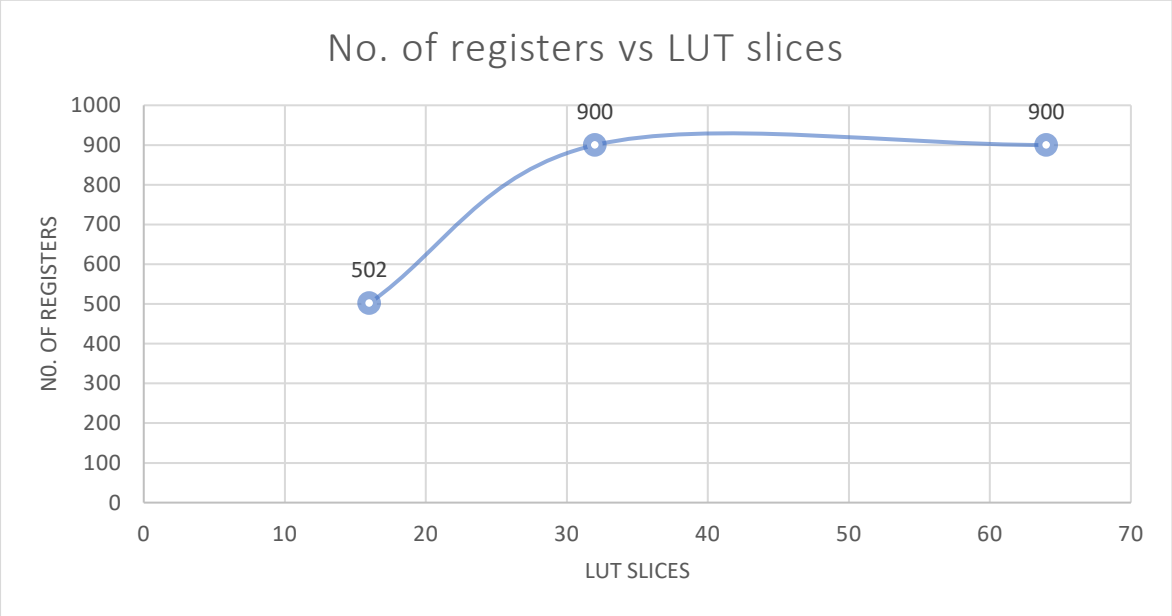
Submitted to :

Sharad sir

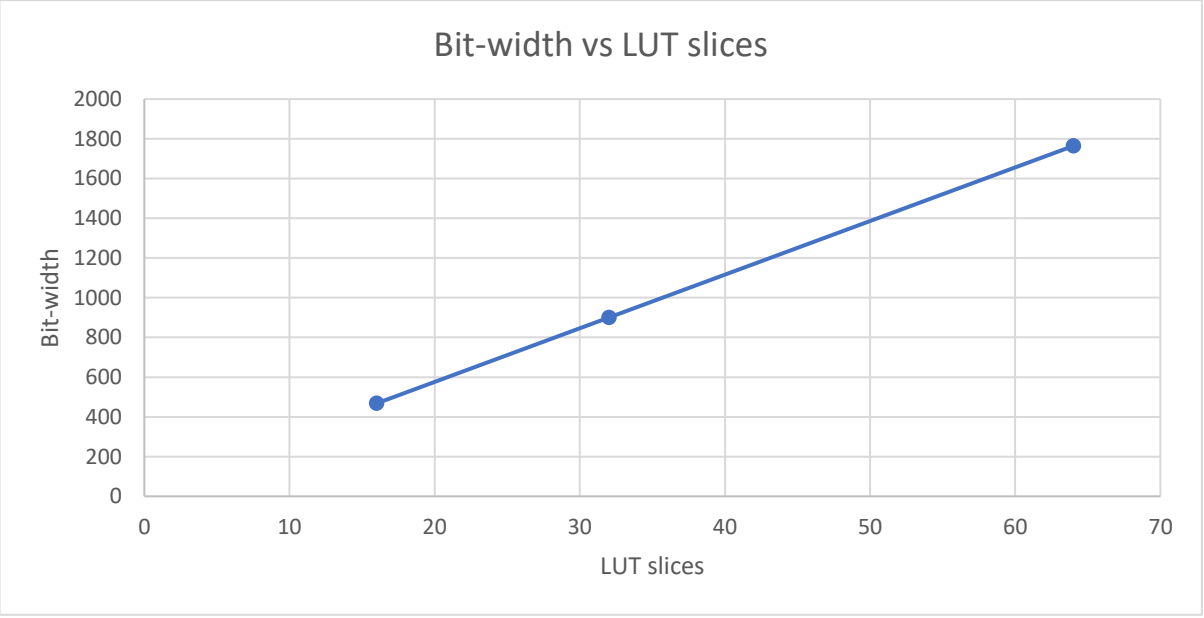
Question : Synthesize the given behavioural code and plot the ‘number of slices’ used vs ‘No. of registers’ and ‘the minimum clock cycle period’ in ns vs ‘No. of registers’ (change the parameter for No. of registers {NREG=16, 32, 64}). Here we can keep the bit-width of each register (DSIZE parameter) to be constant (for example DSIZE=32).

No. of registers (NREG)	Bit-width (DSIZE)	No. of register slices used	No. of LUT slices used	Min clock period in ns
4	32	128	186	3.899
8	32	256	302	4.345
16	32	512	502	4.546
32	32	1024	900	6.456
64	32	1024	900	7.786

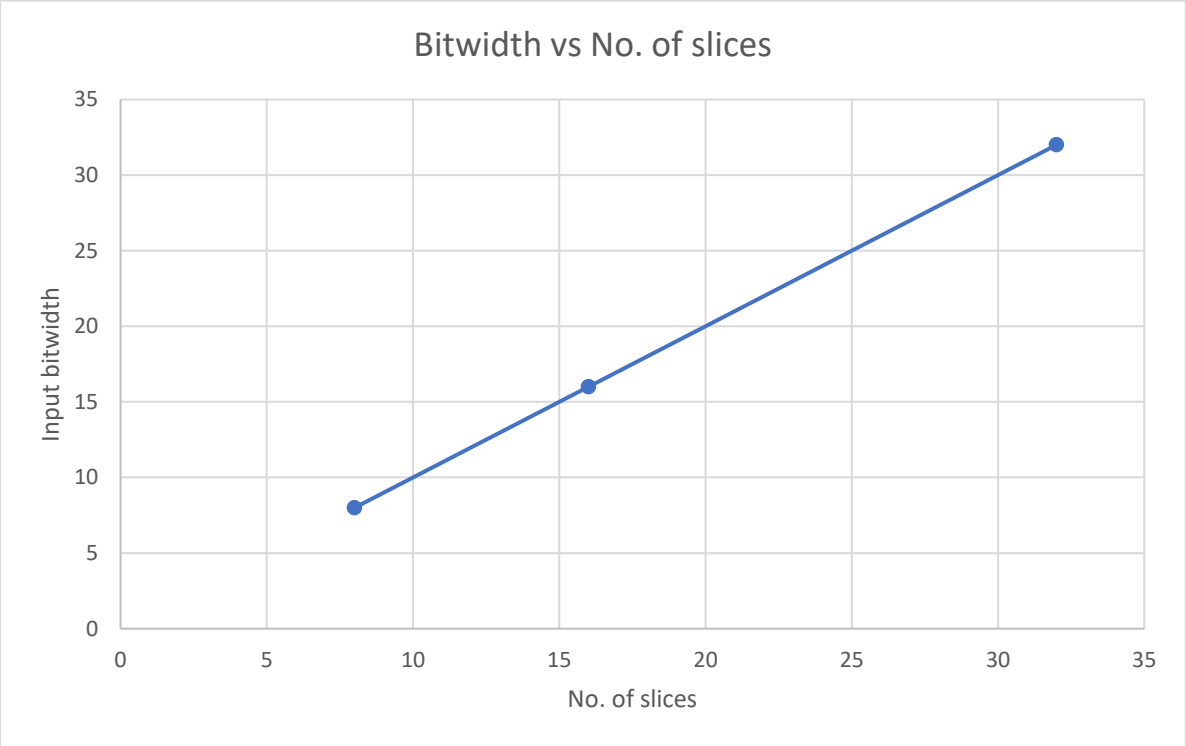


Question : Synthesize the given behavioralcode and plot the number of slices used vs bit-width of the register (DSIZE) and delay in ns vs bit-width of the register (change the parameter for bit-width of the registers {DSIZE=16, 32, 64}). Here we can keep the number of registers (NREGparameter) to be constant (for example NREG=32) and thus ASIZE will be a constant =5.

No. of registers (NREG)	Bit-width (DSIZE)	No. of register slices used	No. of LUT slices used	Min clock period in ns
32	4	128	144	6.756
32	8	256	252	6.998
32	16	512	468	6.435
32	32	1024	900	6.363
32	64	2048	1764	IO port insufficienct



Question : You are given the Verilog code as well as the test bench for ALU. You have to test whether the ALU gives correct results. B.You need to set the input bit-width to 8, 16and32 (one by one) and find out the number of slices used. You need to plot area (vs) bit-width as well as delay (vs) bit-width for the ALU module. In FPGA you cannot find area directly so instead of area you can take number of slices, which would be considered proportional to the area.



Input bitwidth	No. of registers(NREG)	No. of slices	Min clock period in ns
8	32	8	8.234
16	32	16	8.654
32	32	32	11.765