Analog and Digital VLSI Design, EEE/INSTR F313
Assignment-1
I sem. 2023-2024
Department of Electrical & Electronics Engineering, BITS Pilani
August 2023

The objective of this assignment is to familiarize you with the digital circuit design, layout, and simulation techniques prevalent in the industry. You will get to know how our digital circuits/ units function at the circuit level by the co-ordination between voltages and currents. You will get a better insight into the Digital VLSI Design.

I. PROCESS TECHNOLOGY DETAILS

- Use the digital MOSFETs in SCL/ TSMC 180 nm technology.
- Core voltage (VDD) for this technology is 2 V.
- Model file (contains both NMOS and PMOS transistor)

II. GENERAL INSTRUCTIONS

For part (a) of the Problem (Every group need to present this design and answer the viva questions . Viva Session/s will be arranged by instructor/s later.

- This assignment shall be done in group/ team. Each group shall have 3 members.
- Students need to create their groups on their own, chose an assignment problem from the list and fill the information at the following link. Problem assignment is on first come-first served basis.
- No two groups should choose same problem.
- kindly choose your team (**3 students per team**) and fill in the details at the following link---

  https://forms.gle/Nycq1xbLzRvXdPMYA

- You have to keep in mind that the critical path delay of your design should be minimized.
- Students can deviate from the design specs. provided by us, but they have to prove that their specs are better than provided.
- You are encouraged to look for papers, articles, or books about in order to optimize your design.
- You have to draw the full-custom layout of your design. It should pass DRC, LVS and PEX and then post-layout simulation for performance analysis.
- Assume any suitable and relevant data that you feel is missing.
- Use output load capacitance to be **300 fF** in your design. (if not stated).
- Use proper Sizing for designing your circuit. Take length as minimum i.e. 180nm and compute W using logical effort. Any random sizing used will be penalized.
- Layout for capacitance and resistor should not be drawn (if any).
- For all the design find the minimum power, propagation delay and area.
- Body of PMOS is connected to VDD and body of NMOS is connected to GND.

- If W/L within the groups are found to be similar or close to each other than the groups will be penalized.
- Discussing with your friends is highly encouraged (but not copying). **Plagiarism will be penalized**.
- You are free to choose any CMOS implementation style for the design, including but not limited to: complementary CMOS, ratioed logic, DCVSL, pass-transistor logic, CPL, and dynamic logic. Feel free to mix the logic families in your design. All complimentary signals must be internally generated, and any number of levels of logic may be used.
- As the assignment will be based on relative grading, the more challenging you make from others the more marks you will be awarded.

For part (b) of the Problem:

- Each group should develop a mini subsystem composed of digital circuit allotted to them in verilog . Simulate the circuit using Modelsim and verify its functionality.
- The understanding obtained from this part **may be** assessed through a **quiz** .

III. ASSIGNMENT PROBLEMS

You have to work on this assignment in groups of 3 only.

Problem 1.

(a) Design a 8-Bit odd Parity Generator/ detector at 1GHz with load capacitance of 1pF.

(b) Design a synchronous counter which counts the sequence 0→2→4→5 using JK flip flop . Avoid lock out.

Problem 2.

(a) Design a full adder using CMOS style.

(b) Design a synchronous sequential circuit has one input and an output. The output, 'O' will go high and remain so if input is high for two consecutive inputs followed by low for two consecutive inputs.

Problem 3.

(a) Design a 4-bit even parity checker circuit. If the 4-bit message received (3 bit data and 1-bit parity) consists of even number of 1s then output is '0' and output is '1' if the message contains odd number of 1s(hence the error occurred). Design using the basic gates (use minimum type of gates).

(b) Design a sequential circuit has two inputs, 'A' and 'B', and an output, 'O'. Its function is to compare the input sequences on the two inputs. If A != B (not equal to) during any four consecutive clock cycles, the circuit produces O = 1; otherwise, O = 0.

Problem 4.

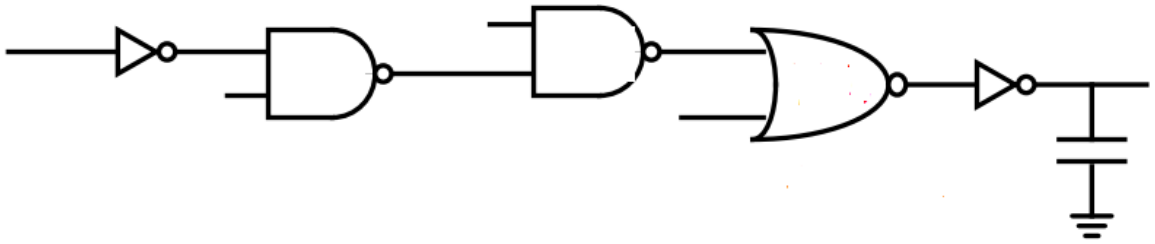
(a) Design a 3:8 decoder. Design using the basic gates (use minimum type of gates).

(b) Design a synchronous sequential circuit has one input and an output. The output, 'O' will go low and remain so if input is high for two consecutive inputs followed by low for two consecutive inputs.

Problem 5.

(a)

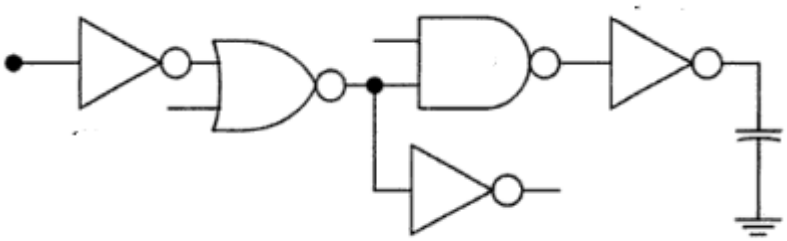
Design the circuit to minimize the delay of the path. Assume 300 fF capacitance at the output.



(b) Design a 4-bit Universal Shift Register

Problem 6.

(a) Design the circuit to minimize the delay of the path. Assume 300 fF capacitance at the output



(b) Design a 16-bit adder using 4-bit ripple carry adders.

Problem 7.

(a) Design a 4 x 4 signed Wallace tree multiplier . Simulate at 1GHz with load capacitance of 500fF. You may use XOR, OR, NOT and AND gates for the implementation of the same.

(b) Design a row decoder circuit for 8 x 8 SRAM memory array. Take column/ column ' capacitance 10pF

Problem 8.

(a) Design a 8 x 8 signed radix 2 Booth multiplier . Simulate at 1GHz with load capacitance of 500fF. You may use XOR, OR, NOT and AND gates for the implementation of the same.

(b) Design a column decoder circuit for 8 x 8 SRAM memory array. Take column/ Column' capacitance 10pF

Problem 9.

(a) Design a Sense amplifier based latch. Simulate at 1GHz with load capacitance of 200fF.

(b) Design a clocked NOR based S R latch .

Problem 10.

(a) Design a Sense amplifier based latch (Q, & Q' output) . Simulate at 1GHz with load capacitance of 200fF.

(b) Design a clocked NOR based S R latch . Simulate at 1GHz with load capacitance of 200fF.

Problem 11.

(a) Design a JK FILP FLOP . Simulate at 1GHz with load capacitance of 200fF.

(b) Design a clocked T FLIP FLOP to generate two quadrature square waveform . Simulate at 1GHz with load capacitance of 200fF.

Problem 12.

(a) Design an SRAM (6 transistor) cell . Simulate at 1GHz with load capacitance of 200fF.

(b) Design a clocked D FLIP FLOP to generate Using MOSFETs only. Simulate at 1GHz with load capacitance of 200fF.

Problem 13.

(a) Design an UP counter cell which counts from 0 to 8. Input is a from output of XOR gate. The inputs to XOR gate are 2 phase shifted square waveform with equal frequency. . Simulate at 1GHz with load capacitance of 200fF.

(b) Design a clocked DIFFERENTIAL 2 input XOR gate Using MOSFETs only. Simulate at 1GHz with load capacitance of 200fF.

Problem 14.

(a) Design an DOWN counter cell which counts from 8 to 0. Input is a from output of XOR gate. The inputs to XOR gate are 2 phase shifted square waveform with equal frequency. . Simulate at 1GHz with load capacitance of 200fF.

(b) Design a clocked DIFFERENTIAL 2 input XNOR gate Using MOSFETs only. Simulate at 1GHz with load capacitance of 200fF.

Problem 15.

(a) Design an DIVIDE BY 2 CIRCUIT cell. Input is a square waveform of frequency 20MHz and output is a square waveform of frequency 10MHz . Simulate at with load capacitance of 200fF.

(b) Design a clocked DIFFERENTIAL 3 input XNOR gate Using MOSFETs only. Simulate at 1GHz with load capacitance of 200fF.

Problem 16.

(a) Exclusive-NOR: Design a 3-input transmission gate based exclusive-nor circuit at 500 MHz frequency with 500 fF load capacitance.

(b) Implement a sequential circuit that can count no. of ones in a stream of incoming bits (one bit per clock cycle). The circuit should have a start, stop external signals.

Problem 17.

a--. Design a 8-to-3 encoder using transmission gate logic A.
b--Design a synchronous mod-6 counter using positive edge triggered JK flip flops whose counting sequence is 000, 110,101,011,010,001,000 etc.

Problem 18.

a----Design a CMOS logic to realize the logic function

$$F = \overline{(A + \overline{B})(\overline{A}C+B)}$$

b----Realize a 4-bit ring counter using shift register. Use parallel load capability of the register to initialize the counter

Problem 19.

(a) Half Adder: Realization of half-adder circuit using Static CMOS design style at 1 GHz for load capacitance of 500 fF.

(b) Design a sequence detector, if the in sequence "0110" (the leading '0' can't use in more than one sequence). Implement the FSM using Logic gates and D FF.

Problem 20.

a)---A. Design a CMOS logic to realize the logic function

$$F = \overline{\bar{A}\,(\,\bar{B}\,\bar{C} + AC\bar{D}\,)}$$

b)----Design a synchronous mod-10 counter using D flip-flops whose counting sequence is 0000,0001,0010,0011,0100,1000,1001,1010,1011,1100

Problem 21.

a)----. Design a 1-to-8 de-multiplexer using transmission gate logic

b)---Design a 4-bit carry look ahead adder to implement sum and carry in CMOS logic

Problem 22.

a)----. Design a circuit to implement the given function in pass transistors logic

$$F = \overline{A + \bar{A}\,\bar{B}\,(B + C)}$$

b)-----. Design a comparator to determine if two n-bit numbers are equal. First design the 1-bit comparator which can be cascaded to achieve the task

Problem 23.

a)---. Design a circuit to implement the given functions in pass transistor logic

$$F = \overline{(AB + \bar{A}\,B)} + BC$$

b)----. Design a shift register for handling a 4-bit string to implement the below table functionality.

S1	S0	Action
0	0	No change
0	1	Shift right 1 bit position
1	0	Shift right 2 bit position
1	1	Shift left 1 bit position

Problem 24.

(a) Design an UP/DOWN counter cell which counts from (8 to 0.) OR (0 TO 8). Up/ down selection is through a SELECT Signal. Input is a from output of XOR gate. The inputs to XOR gate are 2 phase shifted square waveform with equal frequency. . Simulate at 1GHz with load capacitance of 200fF.

(b) Design a clocked differential comparator to determine if two n-bit numbers are equal. First design the 1-bit comparator which can be cascaded to achieve the task .

Problem 25.

a)--. Design a 3-to-8 decoder using transmission gate logic

b)--Design a synchronous mod-6 counter using positive edge triggered JK flip flops whose counting sequence is 000, 001,100,110,111,101,000 etc.

Problem 26.

(a) Design a 4 x 4 signed multiplier using left shift algorithm Simulate at 1GHz with load capacitance of 500fF. You may use XOR, OR, NOT and AND gates for the implementation of the same.

(b) Design a 3:2 compressor for Wallace tree multiplier

Problem 27.

(a) Logic Function Realization

F= AB +AD +BD+ CD

Realization of a logic function using Transmission gate logic style. (use load of 100 fF)

(b) Implement an eight bit barrel shifter where there are three bits that specify the amount of shift on the input. The design should be implemented using multiplexers of suitable size in gate level modeling. Multiplexers can be implemented as per the choice of the designer.

Problem 28.

(a) Decoder Circuit: Realization of 2-bit decoder circuit using Transmission gate logic style at 1GHz for load capacitance of 500fF.

(b) Implement a sequential circuit that can convert a stream of incoming bits (one bit per clock cycle starting form MSB) into its two's complement form. The circuit should have a start, stop external signals for identifying the start and end of the sequence.

Problem 29.

(a) Full CMOS implementation of XOR

Design a 2-input Full CMOS implementation of XOR function circuit at 500MHz frequency with 500fF load capacitance.

Note: Use less than 15 transistors including both NMOS and PMOS in your design.

(b) Build an electronic combination lock with two number buttons (0 and 1), a reset button and a unlock output. The combination should be 01011.

a) Design FSM.
b) Write verilog code for 8:1 MUX and D FF
c) Use 8:1 MUX and D-FF to impelement FSM using Verilog.

Problem 30.

(a) Design a 4:1 multiplexor using CMOS logic style. Simulate with a 500fF load capacitance

(b) Design a modulo-6 counter, which counts in the sequence 0, 1, 2, 3, 4, 5, 0, 1,. The counter counts the clock pulses if its enable input, E, is equal to 1. Use D flip-flops in your circuit.

Problem 31.

(a) Logic Function Realization

Z=[(A+B).(C+D).(E+F+(G.H))]'

Realize above logic function using CMOS logic style (use load of 100fF)

NOTE: If group uses same no. of transistors as in problem no. 6 than penalty of 5 marks.

(b) Design a Machine which can detect 3 consecutive heads in a sequence of random trials of tossing fair coin. Develop a stimulus model for functional verification.

Problem 32.

(a) Logic Function Realization

F= AB +AD +BD+ CD

Realization of a logic function using CPL logic style. (use load of 100 fF)

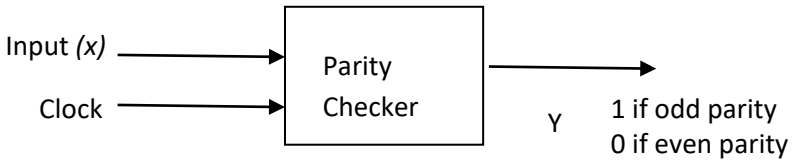
(b) Design and implement a sequence detector to detect the sequence 1011. Use behavioral modeling style and translate FSM exactly to its Verilog code. Perform the same using different state coding scheme such as one hot assignment and binary assignment (using gates/ FF/ MUX etc.) and compare results.

Problem 33.

(a) Four-input pseudo-NMOS NOR

Design a 4-input Four-input pseudo-NMOS NOR circuit at 500MHz frequency with 500fF load capacitance.

(b) A sequence of bits has odd parity if numbers of '1' are odd. Design a circuit which accepts string of bits and output a '1', if parity thus far is odd; or else output a '0'. Develop the FSM. Use structural level style to implement (MUX and FF). Develop a stimulus model for functional verification.



Problem 34.

(a) Design of XOR

Design of a 2-input six transistor CMOS transmission gate implementation of the XOR gate at 500MHz with load capacitance of 1pF.

Note: Complement can be generated using CMOS inverter

(b) Implement an eight-bit carry-select adder. Assume that there are two sub blocks each a four bit ripple carry adder. The individual blocks can be implemented as per the choice of the designer.

Problem 35.

(a) Multiplexer using transmission gate logic style

Design an 8-to-1 multiplexer using transmission gate logic at 800MHz frequency with 100fF load capacitance.

(b) Implement a 4:2 programmable priority encoder using gate level modeling. Use traditional combinational circuits implemented in behavioral modeling. Programmable in the sense the user should be in a position to decide which input will have the highest priority while the others follow in regular order. Example if 3^{rd} input has highest priority then follows 4^{th}, 1^{st} and 2^{nd} inputs.

Problem 36.

(a) Design of an Inverter

Design a CMOS Inverter at 500MHz with load capacitance of 10pF.

(a)Plot the energy and delay graph.

(b)Plot the short circuit and switching power graph.

(b) Design a sequence detector (Moore machine), if the in sequence "0110" (the leading '0' can't use in more than one sequence). Implement the FSM using Logic gates, Mux and D-FF.

Problem 37.

(a) Implementation of Boolean function

F= AB +A'C' +AB'C

Design of a 3-variable boolean function using Static CMOS gate at IGHz with load capacitance of 1pF.

(b) Implement a Mealy type FSM that has an input x and an output y. The machine is a sequence detector that produces y = 1 when the previous two values of x were 00 or 11; otherwise z = 0. Implement the FSM using minimum number of Gates and Flip - Flop (use don't care).

Problem 38.

(a) Multiplexer using transmission gate logic style

Design a 8-to-1 multiplexer using transmission gate logic at 200 MHz frequency with 500 fF load capacitance.

(b) Derive a Mealy type FSM that has an input x and an output y. The machine is a sequence detector that produces y = 1 when the previous two values of x were 00 or 11; otherwise z = 0. Implement the FSM using MUX and Flip - Flop (use don't care). Develop a stimulus model for functional verification.

Problem 39.

(a) Half Adder

Realization of half-adder circuit using Pseudo-NMOS design style at 1GHz for load capacitance of 500fF.

(c) Implement a four bit synchronous gray counter. The circuit should have a reset input, enable input and should run on rising edge of the clock. All the signals are active high and have their usual meaning.

Problem 40.

(a) Exclusive-NOR

Design a 3-input transmission gate based exclusive-nor circuit at 1GHz frequency with 100fF load capacitance.

(c) Implement a combinational circuit that computes |A-B| where A, B are two eight bit numbers. Gate level modeling is to be used.

Problem 41.

(a) Four-input pseudo-NMOS NAND

Design a 4-input Four-input pseudo-NMOS NAND circuit at 500 MHz frequency with 500 fF load capacitance.

(c) Implement a simple 8:3 priority encoder using behavioral modeling and gate level/ structural modeling.

Problem 42.

(a) Design of a Schmitt trigger

CMOS implementation of a Schmitt trigger circuit using total 6 transistors for a load of 100 fF at 1GHz frequency.

(b) Implement a 4:2 programmable priority encoder using gate level modeling. Use traditional combinational circuits implemented in behavioral modeling. Programmable in the sense the user should be in a position to decide which input will have the highest priority while the others follow in regular order. Example if 3^{rd} input has highest priority then follows 4^{th}, 1^{st} and 2^{nd} inputs.

Problem 43.

(a) Design of a buffer circuit

CMOS implementation of a buffer circuit for a load of 500fF at 1GHz.

(b) Implement an overlapping sequence detector that can detect the sequence 101 in a stream of incoming bits. Behavioral level modeling is to be used with Moore type FSM.

Problem 44.

(a) Design of an Inverter

Design a CMOS Inverter at 1GHz with load capacitance of 1pF.

(a)Plot the energy and delay graph.

(b)Plot the leakage, short circuit and switching power graph.

(b) Implement an eight bit barrel shifter where there are three bits that specify the amount of shift on the input. The design should be implemented using multiplexers of suitable size in gate level modeling. Multiplexers can be implemented as per the choice of the designer. Use only 2X1 multiplexers in the whole design.

Problem 45.

(a) Design of an Equality gate

Design a 2-bit equality CMOS gate implementation at 1GHz with load capacitance of 10pF.

(b) Design a simple four bit carry-look- ahead (CLA) adder using gate level modeling and cascade two such stages carry select adder style to build an eight bit adder. Use only 2 input NOR Gates.

Problem 46.

(a) Design of a tri-state buffer circuit

CMOS implementation of a tri-state buffer circuit for a load of 1pF at 500MHz.

Note: Function for tri-state buffer is given by; F=ena'.Z+ena.x

(b) Design a serial adder using J-K flip-flop.

Problem 47.

(a) Decoder Circuit

Realization of 2-bit decoder circuit using Static CMOS logic style at 1GHz for load capacitance of 500fF.

(b) Implement a BCD counter using T flip-flops.

Problem 48.

(a) Encoder Circuit

Realization of 2-bit output encoder circuit using Static CMOS logic style at 1GHz for load capacitance of 500fF.

(b) Implement a sequential circuit that can count the number of 1's in an incoming stream of bits one per clock cycle. The Design style is gate level modeling.

Problem 49.

(a) Design of a tri-state buffer circuit

CMOS implementation of a tri-state buffer circuit for a load of 1pF at 1GHz.

Note: Function for tri-state buffer is given by; F=ena'.Z+ena.x

(b) Design a simple four bit carry-look- ahead (CLA) adder using gate level modeling and cascade two such stages in ripple carry fashion to build an eight bit adder.

Problem 50.

(a) XOR and Exclusive-NOR

Design a 3-input DCVSL logic gate based XOR-XNOR gate circuit at 1 GHz frequency with 100 fF load capacitance.

(b) Implement a simple two bit magnitude comparator using gate level modeling. Cascade two such comparators so that they can act as a four bit magnitude comparator.

Problem 51.

(a) Design of a XOR gate

Design and simulate Static CMOS gate based 3-input XOR gate at 1GHz with load capacitance of 500fF.

(b) Two eight bit numbers need to be compared using serial fashion. There should be only one single bit comparator circuit used repeatedly per each bit. The two eight bit numbers are to be stored in two eight bit registers. The registers and any other components necessary can be implemented using modeling style of your choice.

Problem 52.

(a) Exclusive-NOR

Design a 3-input Static CMOS gate based exclusive-nor circuit at 1GHz frequency with 100fF load capacitance.

(b) Let us think about a special shifter circuit, which is capable of shifting by more bit positions at a time, this circuit rotates the bits of input vector X[3:0] by a specified number of bit positions. This circuit is known as barrel shifter. Design a four bit barrel shifter. Use structural level design style. Develop a stimulus model for functional verification.

Problem 53.

(a)Half Adder

Realization of half-adder using Transmission gate logic style at 1 GHz for load capacitance of 500 fF.

(b) Implement a two bit multiplier using basic gates. This two built multiplier is to be used as a fundamental building block to build a four bit multiplier. The gate level modeling style is to be used.

Problem 54.

(a) Design of a XOR gate

Design and simulate Pseudo-NMOS logic style 3-input XOR gate at 500 MHz with load capacitance of 1pF.

(b) Implement a four bit universal shift register using JK-flip flops. Gate level/ Structural modeling style need to be used.

Problem 55.

(a) Multiplexer using pass-transistor logic style

Design a 8-to-1 multiplexer using pass-transistor logic at 200MHz frequency with 500fF load capacitance.

(b) Design a sequence detector (Mealy Machine) that searches for a series of binary inputs to satisfy the pattern 01[0*]1, where [0*] is any number of consecutive zeroes. The output (Z) should become true every time the sequence is found.

Problem 56.

a---. Design a CMOS logic to realize the logic function

$$F = \overline{\overline{A}\,(\overline{B} + C) + \overline{D}}$$

b---Design a synchronous mod-10 counter using D flip-flops whose counting sequence is 0000,1001,0111,0010,1011,0100,1101,1000,0110,1111

Problem 57.

(a) Implementation of Boolean function

F= AB +A'C' +AB'C

Design of a 3-variable boolean function using transmission gate using transistors less than 15 at 500MHz with load capacitance of 1pF.

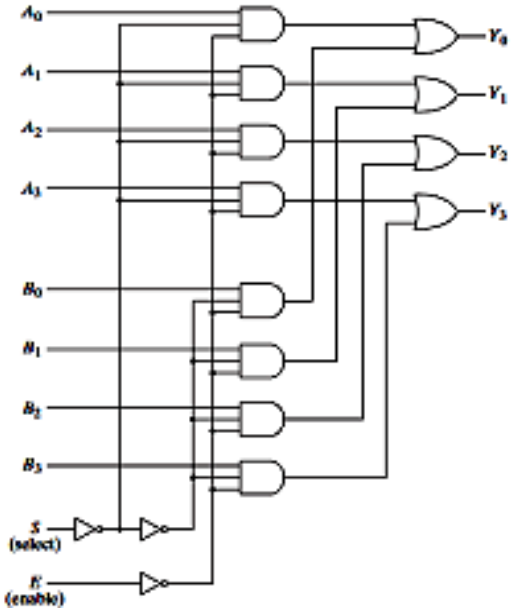
Note: Complement can be generated using CMOS inverter.

(b) Two eight bit numbers need to be added using a serial bit adder. A serial bit adder is a circuit has only one full adder cell and a memory element to hold the carry. The two eight bit numbers are to be stored in two eight bit registers. The registers and any other components necessary can be implemented using modeling style of your choice.

Problem 58.

(a) Quadruple 2-to-1 multiplexer

Design a Quadruple two to one multiplexer as shown below. Use CMOS logic style for circuit implementation with 100fF load. Use proper sizing for designing your circuit.



NOTE: Any random sizing used will be penalized. Optimize your design in terms of power and delay.

(b) Design a Finite State Machine to detect “10110” sequence, leading "10" can be taken in more than one sequence. Develop Mealy Machine. Finally implement using D FF and MUX.

Problem 59.

(a) Logic Function Realization

$$Z= [(A \,.\, B.\, F + (C+(D.F)+E.C + H))]'$$

Realization of a logic function using CMOS logic style having load capacitance of 100fF.(minimize use of transistors including both NMOS and PMOS in your design.

(b) Design a sequence detector, if the in sequence “0111” (the leading ‘1’ or ‘0’ can’t use in more than one sequence). Implement the FSM using Logic gates and D FF.

Problem 60.

(a) Design of a buffer circuit

CMOS implementation of a buffer circuit for a load of 1pF at 500MHz.

(b) Implement an eight bit carry-select adder. Assume that there are two sub blocks each a four bit ripple carry adder. The individual blocks can be implemented as per the choice of the designer.

Problem 61.

(a) Logic Function Realization

$$X= [(A.\, B.F + (B+D.E.F) + H)]'$$

Realization of a logic function using CPL logic style having load capacitance of 200fF. use minimum no. of transistors.

(b) Implement 3 bit asynchronous ripple counter using T flip-flops.

Problem 62.

(a) NAND/AND USINF CPL

Design of a 3-input NAND/AND logic gate using CPL logic style at 500MHz with load capacitance of 500fF.

(b) Implement a 3 bit asynchronous ripple counter using JK flip-flops

Problem 63.

(a) Design of a Schmitt trigger

CMOS implementation of a Schmitt trigger circuit using total 6 transistors for a load of 500fF at 500MHz frequency.

(b) Design a simple four bit carry-look- ahead (CLA) adder using gate level modeling and cascade two such stages in ripple carry fashion to build an eight bit adder.

Problem 64.

(a) OR/NOR gate using CPL

Design of a 3-input OR/NOR logic gate using CPL logic style at 1GHz with load capacitance of 500fF.

(b) Design a synchronous BCD counter using D-FF.

Problem 65.

(a) Logic Function Realization

$$F= AB +AD +BD+ CD$$

Realize the above logic function using CMOS logic style. (use less than 21 transistors including both NMOS and PMOS in your design) (use load of 100fF)

(b) Two eight bit numbers need to be added using a serial bit adder. A serial bit adder is a circuit has only one full adder cell and a memory element to hold the carry. The two eight bit numbers are to be stored in two eight bit registers. The registers and any other components necessary can be implemented using modeling style of your choice.

Problem 66.

(a) XOR/NXOR USINF CPL

Design of a 3-input XOR/NXOR logic gate using CPL logic style at 1GHz with load capacitance of 500 fF.

(b) Design a Machine which can detect 3 consecutive heads in a sequence of random trials of tossing fair coin. Use one hot assignment for defining the states.

Problem 67.

(a) Multiplexer using pass-transistor logic style

Design an 8-to-1 multiplexer using pass-transistor logic at 800 MHz frequency with 100 fF load capacitance.

(b) Implement a four bit universal shift register using D-flip flops. Gate level modeling style is to be used.

Problem 68.

(a) Design of a XOR gate

Design and simulate Transmission gate based 3-input XOR gate at 1GHz with load capacitance of 500fF.

(b) Design/ implement logic function F= [AB+E] [C+D] using NOR gate only. Used gate-level modelling.

Problem 69.

(a) Implementation of Boolean function

F= AB +A'C' +AB'C

Design of a 3-variable Boolean function using CPL using minimum transistors at 500MHz with load capacitance of 1pF.

Note: Complement can be generated using CMOS inverter.

(b) Design a simple four bit carry-look- ahead (CLA) adder using gate level modeling and cascade two such stages in ripple carry fashion to build an eight bit adder. Use only two input NAND gates in the whole design.

Problem 70.

(a) Logic Function Realization (use switch logic)

X= [(A + B.F + (C+D+E.G + H)]

Realization of a logic function using Pseudo-NMOS logic style having load capacitance of 200fF (use less than 15 transistors including both NMOS and PMOS in your design (a).

(b) Implement an overlapping sequence detector that can detect the sequence 101 in a stream of incoming bits. Behavioral level modeling is to be used with Mealy type FSM.

Problem 71.

(a) Multiplexer using NAND gate logic

Design a 2-to-1 multiplexer using NAND gates only at 500MHz frequency with 500fF load capacitance.

(b) Implement the function F= AB +A'C' +AB'C using only NOR gates. Use gate level modelling for the implementation.

Problem 72.

(a) Multiplexer using NAND gate logic

Design a 2-to-1 multiplexer using NAND gates only at 1 GHz frequency with 1 pF load capacitance.

(b) Implement 4 bit Binary to Gray code converter using gate level modeling.

Problem 73.

(a) Encoder Circuit

Realization of 2-bit output encoder circuit using Transmission gate logic style at 1GHz for load capacitance of 500fF.

(b) Implement the function F= AB +A'C' +AB'C using only NAND gates. Use gate level modelling for the implementation.

Problem 74.

(a) Design a three-bit synchronous down counter. You may use D or JK flip flops, and other required gates if any. Simulate at 1GHz with load capacitance of 1pF

(b) Design a sequential state machine that has an input 'A' and an output 'Z'. The machine has to generate Z = 1 when the previous four values of A were 1001 or 1111; otherwise, Z = 0. Overlapping input patterns are allowed.

Eg:

If A : 010111100110011111 THEN Z : 000000100100010011

Problem 75.

(a) Half Adder

Realize a half-adder using DCVSL logic style at 1GHz for load capacitance of 500fF.

(b) Design a sequence detector, if the in sequence "0110" (the leading '0' can't use in more than one sequence). Implement the FSM using MUX and D FF.

Problem 76.

(a) Design a 4:1 multiplexor using pass transistor logic style. Simulate with a 500fF load capacitance

(b) Design a synchronous counter which counts the sequence 1→3→15→5→8→2→0→12→6→9 continuously

Problem 77.

(a) Design a 3-bit asynchronous counter using D flip flops.

(b) Design a sequential circuit which produces an output '1' every time a sequence "1110" is detected, otherwise the output is '0'. Overlapping sequence detection has to be implemented.

Problem 78.

(a) Design a 4-bit equality comparator using the basic gates (use minimum type of gates)

(b) Design a moore type serial adder to generate sum of two bits with carry.

Problem 79.

(a) Design a 4-bit magnitude comparator using the basic gates (use minimum type of gates). The comparator should indicate equal, less than and greater than conditions.

(b) Design a mealy type serial adder to generate sum of two bits with carry.

Problem 80.

(a) Design a combinational circuit to check if all bits of an 8 bit input are zero. Design using the basic gates (use minimum type of gates).

(b) Design a synchronous counter which counts the sequence 9→6→12→0→2→8→5→15→3→1continuously

Problem 81.

(a) Design a combinational circuit to check if all bits of an 8-bit inputs are ones. Design using the basic gates (use minimum type of gates).

(b) Design a synchronous counter which counts the sequence 6→7→3→1 using JK flip flop . Avoid lock out.

Problem 82.

(a) Design a 4-bit XOR gate using CMOS logic

(b) Design a synchronous counter which counts the sequence 1→3→5→7 using JK flip flop . Avoid lock out.

Problem 83.

(a) Half Adder

Realization of half-adder using Pass-transistor logic style at 1GHz for load capacitance of 500fF.

(b) Implement three input XOR gate using NAND gates. Use gate level modelling for the implementation.

Problem 84.

(a) Magnitude Comparator

Design a 2-bit magnitude comparator using CMOS logic style. Use load capacitance of 100fF

(b) Implement an 8:1 MUX using 2:1 MUX. Use gate level modelling to define 2:1 MUX.

Problem 85.

(a) Design a Mod-100 Decimal Counter at 1GHz with load capacitance of 1pF.

(b) Design a circuit that finds the $\log_2$ of an operand that is stored in an n-bit register. Show all steps in the design process and state any assumptions made. Give verilog code that describes your circuit.

Problem 86.

(a) Design a 8:1 multiplexer using pass transistor logic.

(b) Give a binary to gray code convertor. Code this as verilog program

Problem 87.

(a) Design a 4-bit Universal Shift Register at 1GHz with load capacitance of 1pF.

(b) Design a three-bit counter like circuit controlled by the input w. If w=1, then the counter adds 2 to its contents, wrapping around if the count reaches 8 or 9. Thus if the present state is 8 or 9, them the next state becomes 0 or 1, respectively. If w=0, then the counter subtracts 1 from its contents, acting as normal down-counter. Use D flip-flops in your circuit.

Problem 88.

(a) Design a 1-bit magnitude comparator using CMOS logic style. Use load capacitance of 200fF

(b) Write a verilog code that represents an 8-bit Johnson counter. Synthesize the code with your CAD tools and give a timing simulation that shows the counting sequence.

Problem 89.

(a) Design a BCD-to-4-bit Gray code Converter 500 MHz with load capacitance of 500 fF.
(b) Create a verilog module named if2to4 that represents a 2-to-4 decoder using an if-else statement. Create a second module named h3to8 that represents the 3-to-8 binary decoder using two instances of the if2to4 module.

Problem 90.

(a) Design a Binary-to-Gray code Converter at 1GHz with load capacitance of 500fF.
(b) Implement a 8-bit multiplier which makes use of a 2-bit full adder (shift-add algorithm).

Problem 91.

(a) Design a Gray-to-Binary code Converter at 1GHz with load capacitance of 500fF.
(b) Implement an 16:1 MUX using 4:1 MUX. Use gate level modelling to define 4:1 MUX.

Problem 92.

(a) Design a 8-Bit Parity checker at 1GHz with load capacitance of 1pF.
(b) A 3-to-8 decoder is used to select the bit that is to be changed in a 8-bit register. The register's bit selected by the 3-bit input is XORed with '1' and all the remaining bits of the register are ANDed with '1's. Assume that the LSB (bit 0) is the right-most bit and MSB (bit 7) is the left-most bit of the 8-bit register. Write a Verilog code for this circuit.

Problem 93.

(a) Design a TSPC D Flip-flop with load capacitance of 500fF. Also optimize switching speed or maximum operating frequency.
(b) Develop a data-flow model of an 8-bit odd parity checker. The parity checker has eight inputs, i1 to i8, and an output p. The logic equation of the parity checker is:

$$p = ((i_1 \oplus i_2) \oplus (i_3 \oplus i_4)) \oplus ((i_5 \oplus i_6) \oplus (i_7 \oplus i_8))$$

Code the above logic equation by using two statements.

Problem 94.

(a) Implementation of Boolean function

$$Y = \overline{A + B} + \overline{A}\,\overline{C}$$

Design of a 3-variable Boolean function using CPL using minimum transistors at 500MHz with load capacitance of 1pF.

(b) Show a FSM model of a synchronous circuit that counts the number of 1s in a continuous stream of bit data that consists of 1s and 0s which arrive at each positive clock edge. When the count of 1s reaches 128, it outputs a signal that turns on a red light for a period equal to five numbers of positive clock edges. The red light is then switched-off and the default state of green light on is set.

Problem 95.

(a) Design a half subtractor using NAND gates only at 500MHz frequency with 500fF load capacitance.
(b) Design a Moore machine that samples a serial bit stream and asserts an output if the last three samples are 1.Assume that the samples are made at the inactive edges of the clock. Design the machine using D Flip Flops.

Problem 96.

(a) Design a 8-bit carry-select adder at 1GHz with load capacitance of 500fF.
(b) Design the state transition Moore machine that converts a NRZ bit stream into a NRZI bit stream.

Problem 97.

(a) Design a full adder using NAND gates only at 500MHz frequency with 500fF load capacitance.
(b) Design a 4 bit signed magnitude comparator using structural model.

Problem 98.

(a) Design a 8-Bit Parity Detector at 1GHz with load capacitance of 1pF.
(b) Design a decade (mod-10) counter with asynchronous reset using structural model.

Problem 99.

(a) Design a full subtractor using NOR gates only at 500 MHz frequency with 500 fF load capacitance.
(b) A universal shift register can shift in both the left to right and right to left directions, and it has parallel load capability. Design this shift register with n bits.

Problem 100.

(a) Design a half adder using NAND gates only at 500 MHz frequency with 500fF load capacitance.
(b) Design a counter that counts pulses on line w and displays the count in the sequence 0,2,1,3,0,2,……Use D flip flops in the circuit.

Problem 101.

(a) Logic Function Realization

$$F' = [(D+E+A)(B+C)]$$

Realization of a logic function using CMOS logic style with a load capacitance of 100fF

(b) Design a sequential circuit which produces an output '1' every time a sequence "1010" is detected. Overlapping sequence detection has to be implemented. For e.g.: if the incoming sequence (input is provided serially) is 11001101010 the output sequence generated should be 00000000101 .Use D filp flops to realize the circuit.

Problem 102.

(a) Design a 4-bit carry ripple adder using propagate generate (PG) logic. Simulate at 1GHz with load capacitance of 500fF. You may use XOR, OR, NOT and AND gates for the implementation of the same. Simulate at

(b) Design a 3-bit odd parity generator/ detector using JK Flip flops.

Problem 103.

(a) Design a CMOS full adder circuit at 1 GHz with load capacitance of 500 fF.

(b) Design a serial adder circuit. The circuit designed should be a synchronous circuit which accepts serial inputs 'X1' & 'X2' and a carry bit 'C1' serially and produces an output 'Z'. You may use D-flip flops and other basic digital gates for the implementation of the circuit.

Problem 104.

(a) Design a four bit synchronous up counter. You may use D or JK flip flops, and other required gates if any. Simulate at 1 GHz with load capacitance of 1 pF

(b) Design a sequential circuit has two inputs, ‘A’ and ‘B’, and an output, ‘O’. Its function is to compare the input sequences on the two inputs. If A = B during any four consecutive clock cycles, the circuit produces O = 1; otherwise, O = 0.

Eg:

A: 0110111000110

B: 1110101000111

O: 0000100001110 derive a suitable circuit

IV. DEADLINES-SUBMISSION

Submission of a report (.pdf and hard copy) containing theoretical description of your design (circuit parameters, equations & calculations, transistor-level schematic). Please use extra font size for labels and wider lines for plots (so that they are readable even when you reduce the figure size in your pdf). In-case of performance comparison you are suppose to make a proper table.

Your report should also contain the full-custom layout with DRC, LVS & PEX. Finally the post layout simulation results which you have to compare with you pre-layout result. The submission deadline is **1 Oct. 2023.**

NOTE: Evaluation is solely based on this document, viva.

V. DEADLINES

Posting of Assignment	**27 August**
Choosing one of the problem	
Submission of the complete report (.pdf) having schematic & netlist, waveforms & other design specs, full-custom layout with DRC, LVS, PEX and post-layout simulation	**1 Oct**

VI. REFERENCES

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[5] Ken Martin, " Digital IC Design", Oxford.

[6] I.E. Sutherland & Bob. F. Sproull., “Logical effort: Designing fast CMOS circuits, Advanced research in VLSI”, Morgan Kaufmanns Publishers, 1999.

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[8] Palnitkar Samir. Verilog HDL: A guide to digital design and synthesis. Vol. 1. Prentice Hall Professional, 2003.

[9] Padmanabam TA, and B. Bala Tripura Sundari. Design through verilog HDL. John Wiley & Sons, 2004.

Report Submission Guidelines---

A detailed report should be submitted with following sections—

- Problem statement and specifications
- Schematic of your design, Layout of your design, Verilog code
- Table containing (w/L) of each transistor
- Results –
  Conclusion--- (all results obtained in Tabular format along with a column giving specification values)
- Problems faced during the design
- Innovation in the design (some design innovation, you have thought on your own)

First page of report should contain name/ id of all team members

SAVE YOUR REPORT AS (PROBLEM_XX. PDF) (EXAMPLE--- PROBLEM_55.PDF)