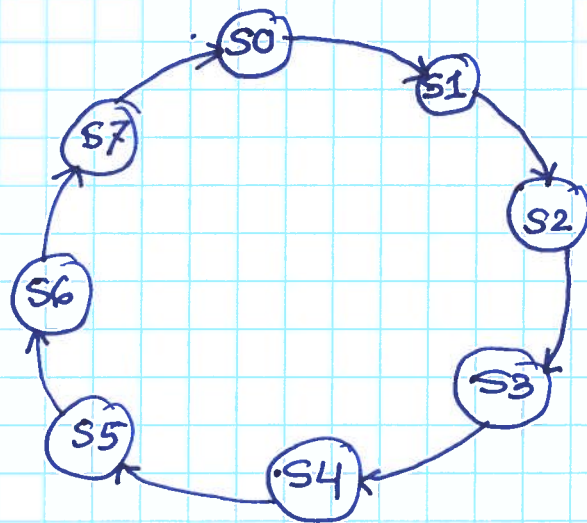


Design a 3-bit synchronous up counter using SR flip-flop



Circuit Excitation Table:

Present State			Next State			S_2	R_2	S_1	R_1	S_0	R_0
Q_2	Q_1	Q_0	Q_2^*	Q_1^*	Q_0^*						
0	0	0	0	0	1	0	X	0	X	1	0
0	0	1	0	1	0	0	X	1	0	0	1
0	1	0	0	1	1	0	X	X	0	1	0
0	1	1	1	0	0	1	0	0	1	0	1
1	0	0	1	0	1	X	0	0	X	1	0
1	0	1	1	1	0	X	0	1	0	0	1
1	1	0	1	1	1	X	0	X	0	1	0
1	1	1	0	0	0	0	1	0	1	0	1

Q_1, Q_0		00	01	11	10
Q_2	0	0	0	1	0
	1	X	X	0	X

$$S_2 = Q_2' Q_1 Q_0$$

Q_1, Q_0		00	01	11	10
Q_2	0	X	X	0	X
	1	0	0	1	0

$$R_2 = Q_2 Q_1 Q_0'$$

Q_1, Q_0		00	01	11	10
Q_2	0	0	1	0	X
	1	0	1	0	X

$$S_1 = Q_1' Q_0$$

Q_1, Q_0		00	01	11	10
Q_2	0	X	0	1	0
	1	X	0	1	0

$$R_1 = Q_1 Q_0$$

Q_1, Q_0		00	01	11	10
Q_2	0	1	0	0	1
	1	1	0	0	1

$$S_0 = Q_0'$$

Q_1, Q_0		00	01	11	10
Q_2	0	0	1	1	0
	1	0	1	1	0

$$R_0 = Q_0$$

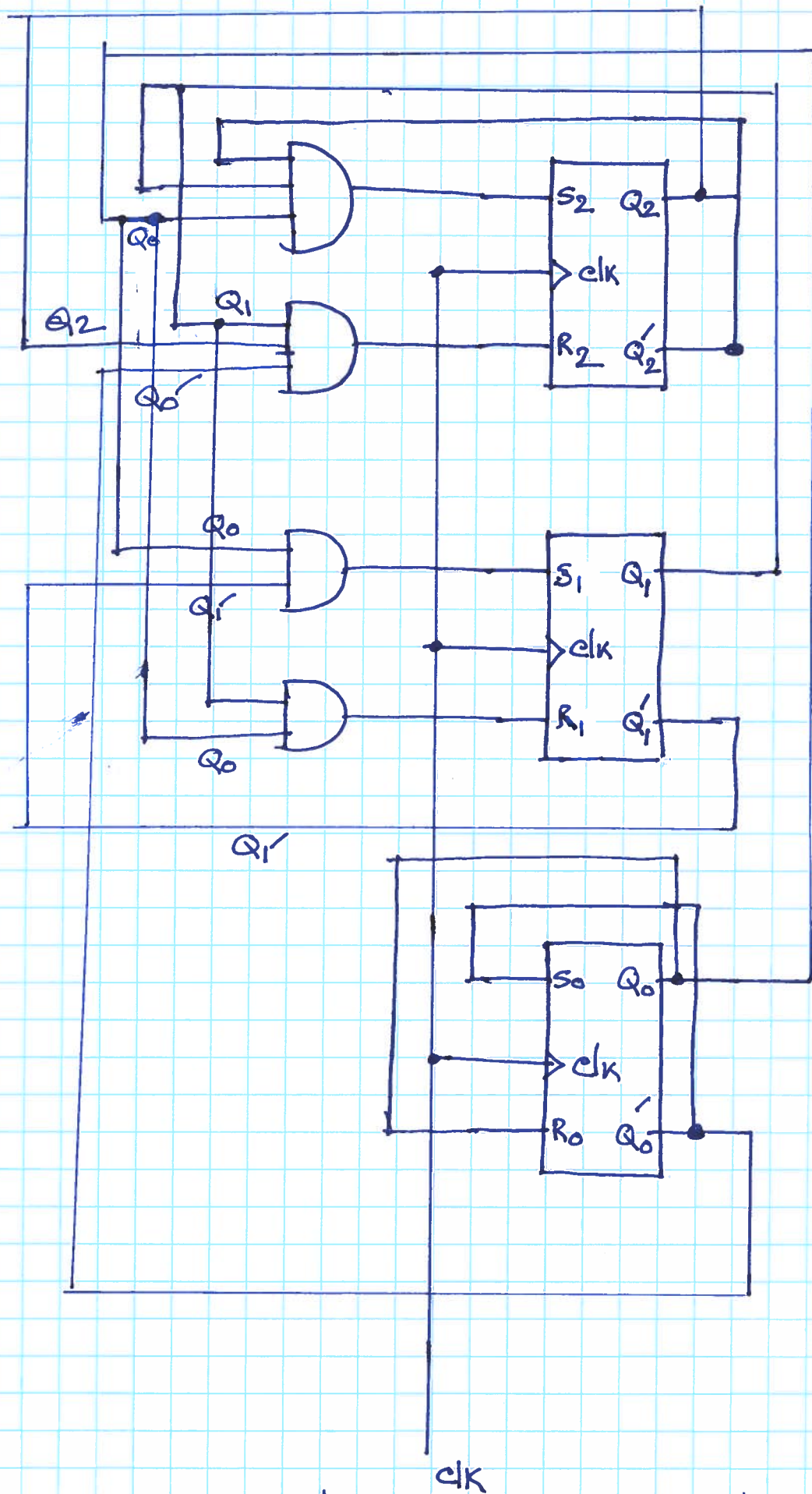


Fig: 3-bit synchronous-up counter with SR flipflop.