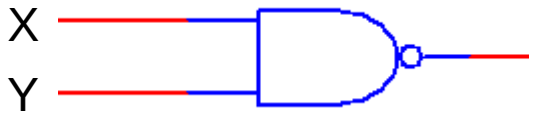
Universal Gate – NAND

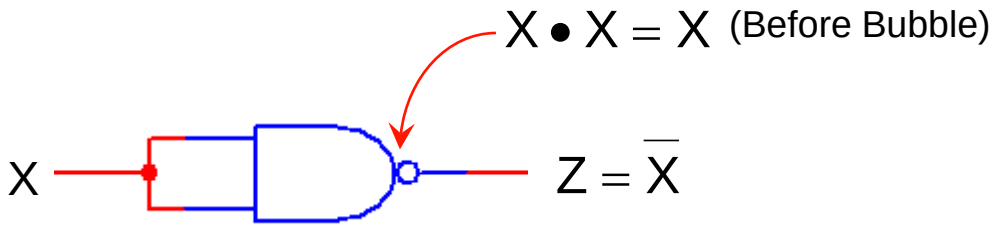
NAND Gate



$$Z = \overline{X\,Y} = \overline{X} + \overline{Y}$$

X	Y	Z
0	0	1
0	1	1
1	0	1
1	1	0

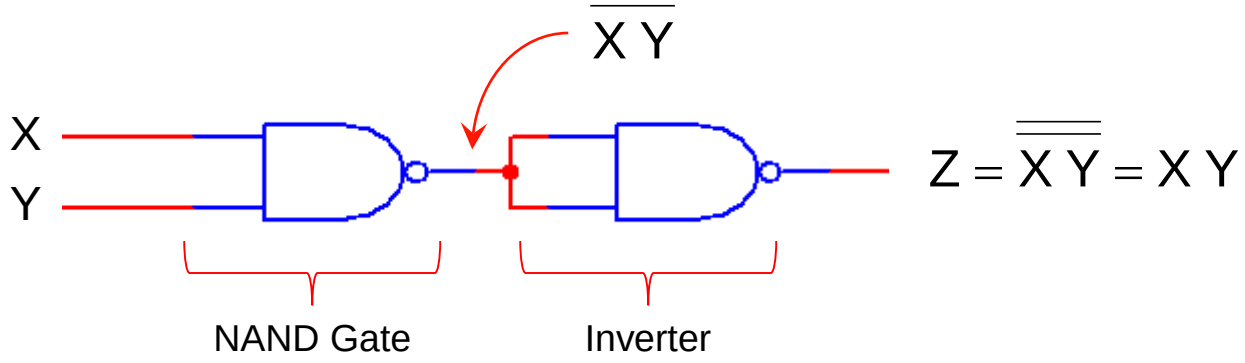
NAND Gate as an Inverter Gate



X	Z
0	1
1	0

Equivalent to Inverter

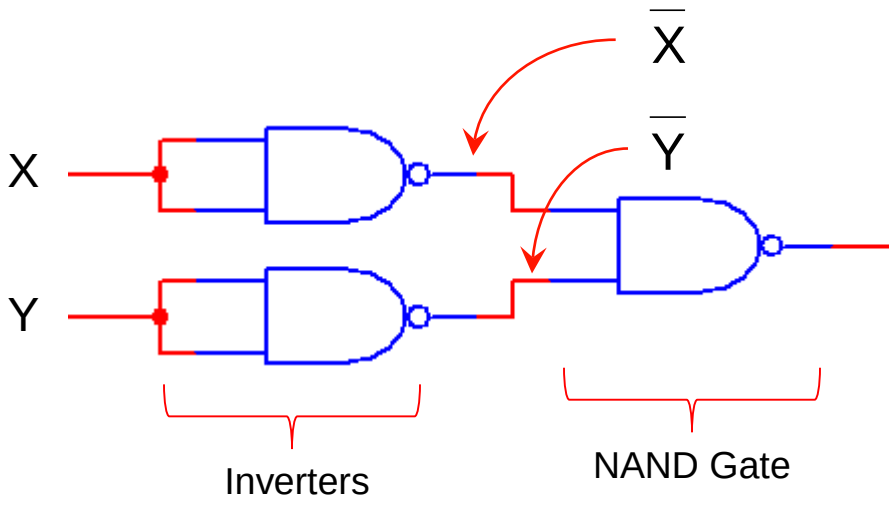
NAND Gate as an AND Gate



X	Y	Z
0	0	0
0	1	0
1	0	0
1	1	1

Equivalent to AND Gate

NAND Gate as an OR Gate



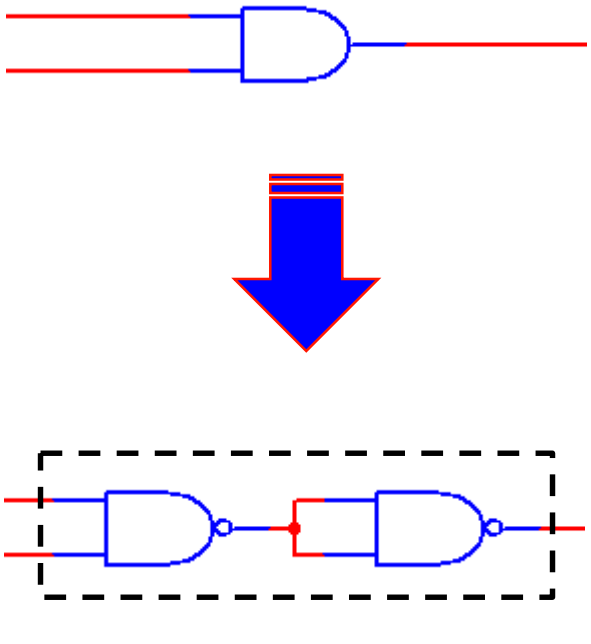
$$Z = \overline{\overline{X}\,\overline{Y}} = \overline{\overline{X}} + \overline{\overline{Y}} = X + Y$$

X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	1

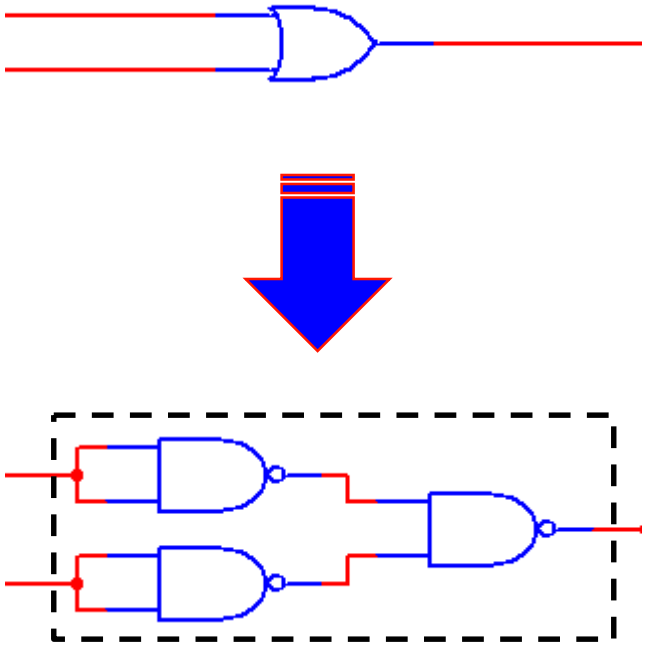
Equivalent to OR Gate

NAND Gate Equivalent to AOI Gates

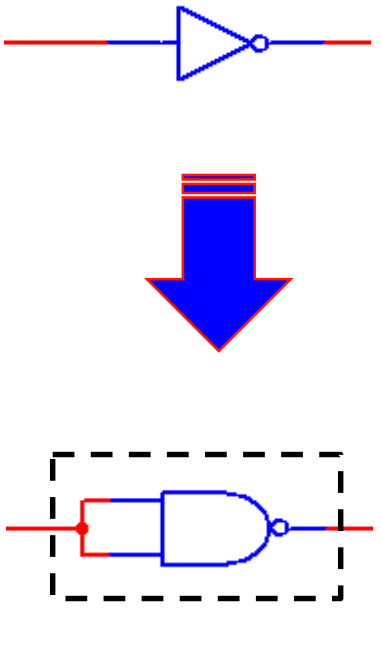
AND



OR



INVERTER



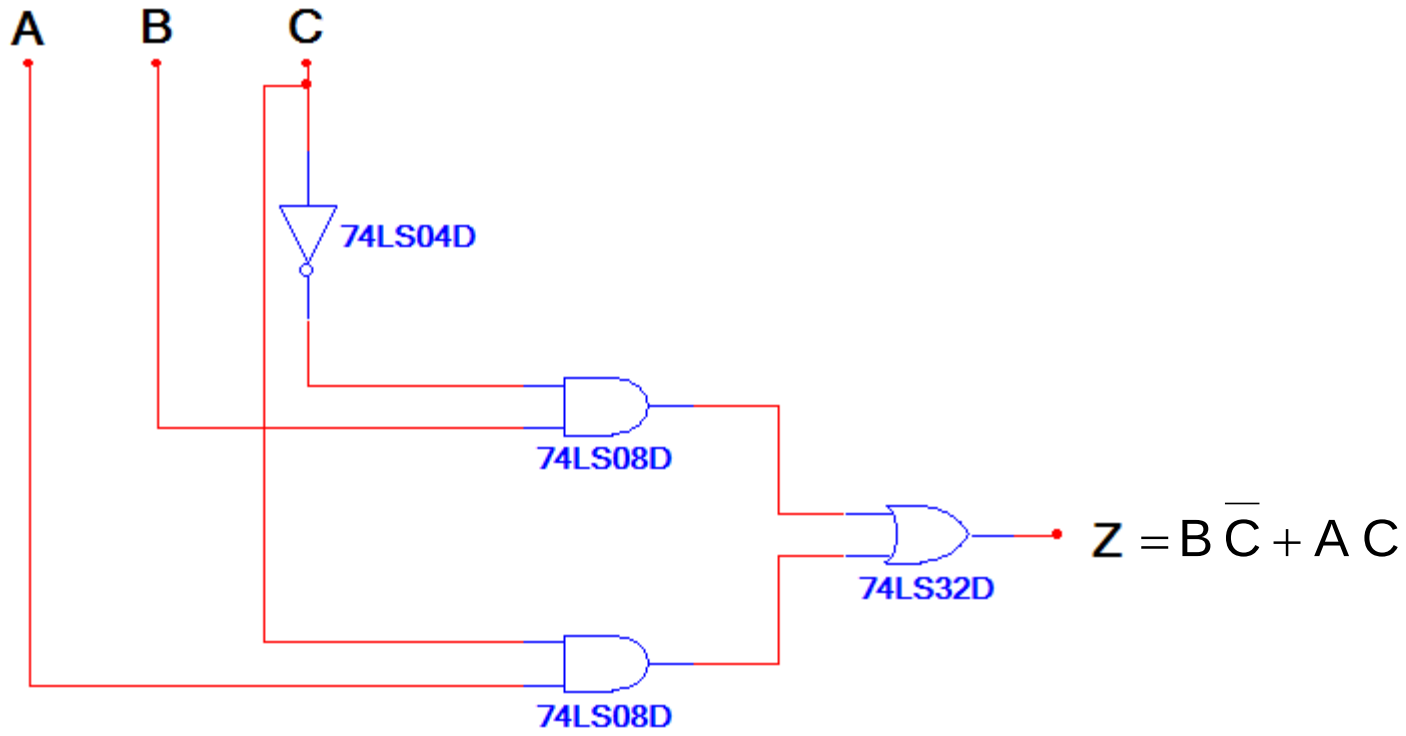
Process for NAND Implementation

1. If starting from a logic expression, implement the design with AOI logic.
2. In the AOI implementation, identify and replace every AND,OR, and INVERTER gate with its NAND equivalent.
3. Redraw the circuit.
4. Identify and eliminate any double inversions (i.e., back-to-back inverters).
5. Redraw the final circuit.

NAND Implementation

Example:

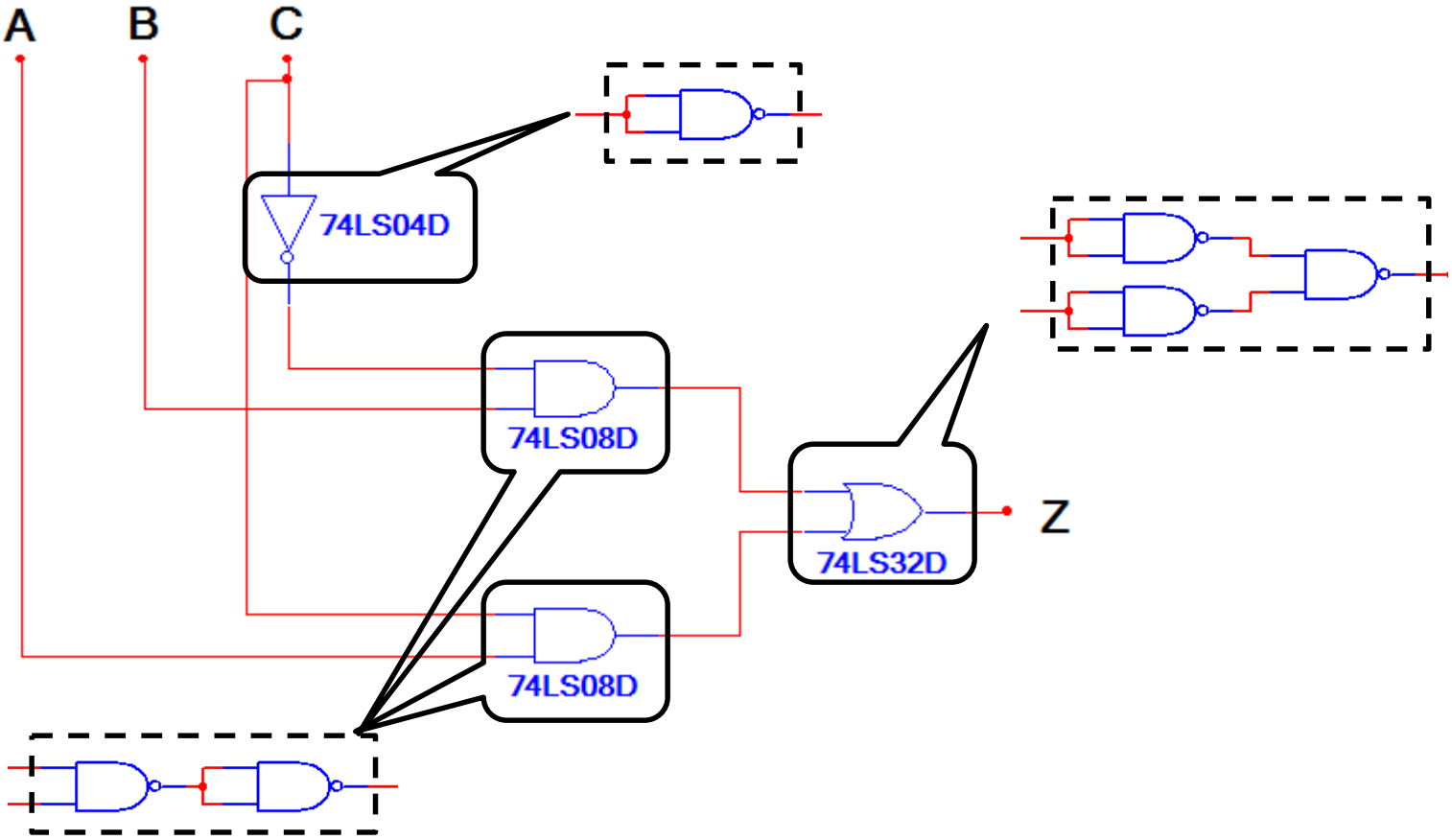
Design a NAND Logic Circuit that is equivalent to the AOI circuit shown below.



NAND Implementation

Solution – Step 2

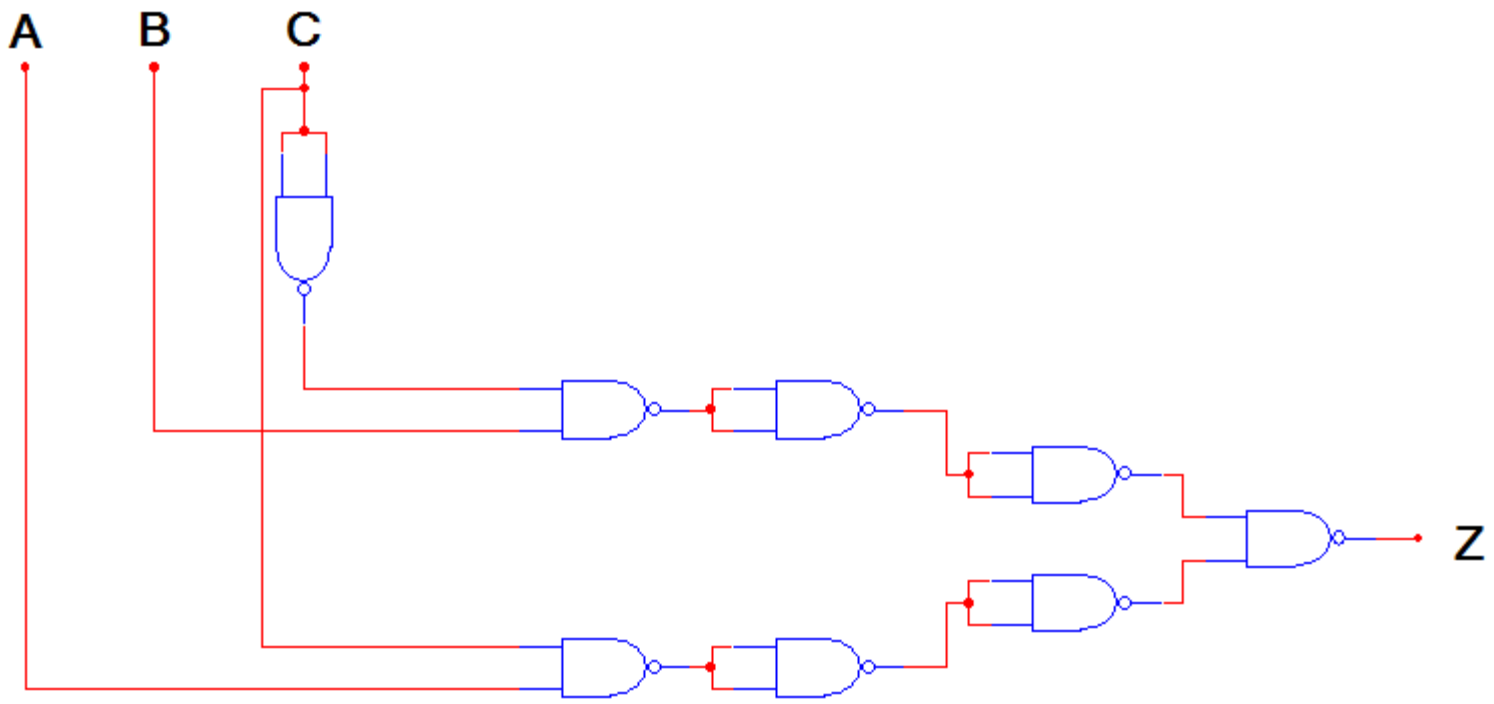
Identify and replace every AND,OR, and INVERTER gate with its NAND equivalent.



NAND Implementation

Solution – Step 3

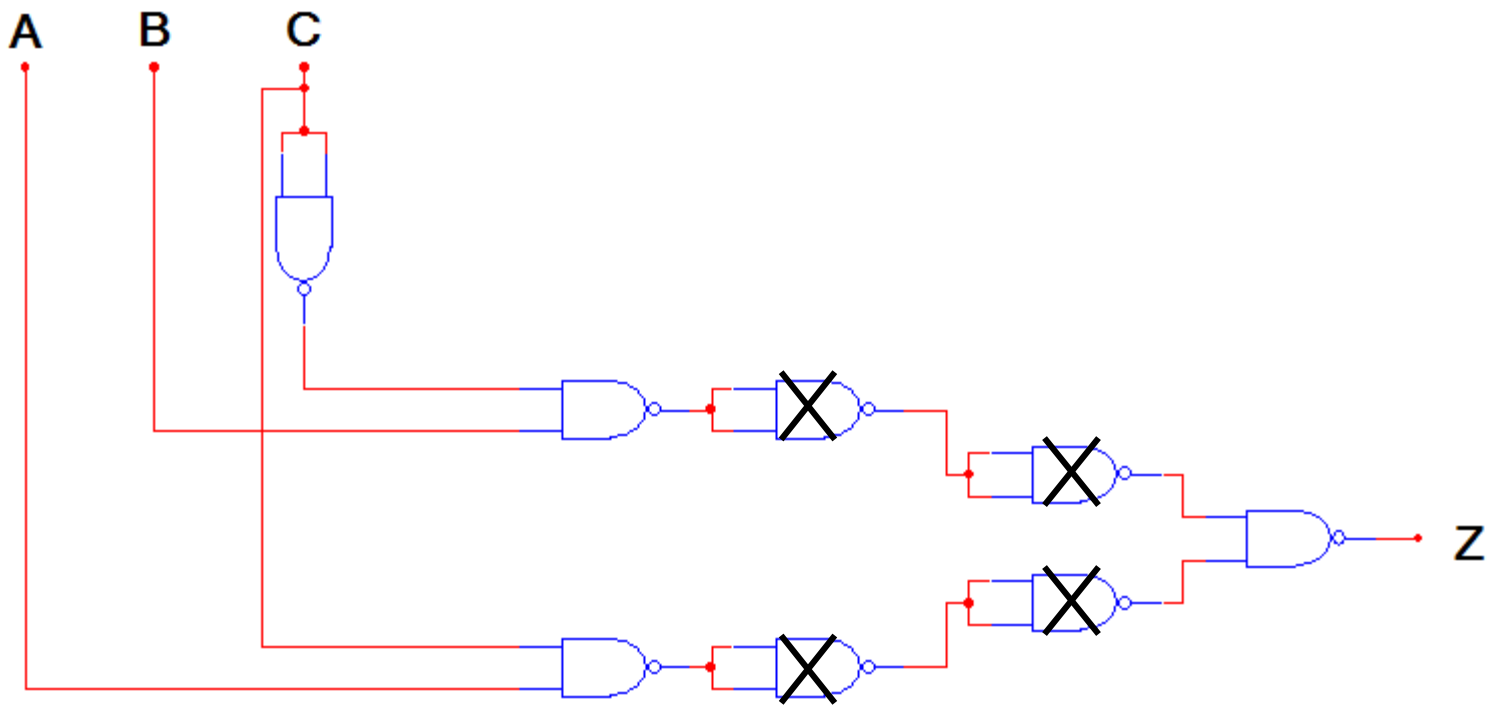
Redraw the circuit.



NAND Implementation

Solution – Step 4

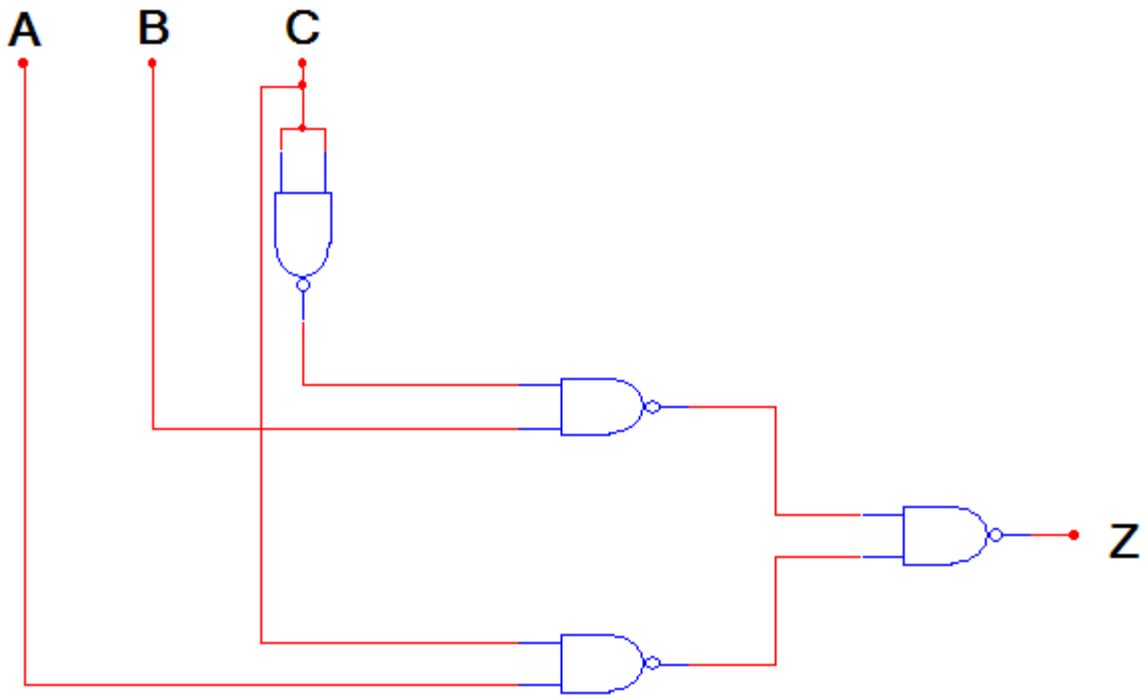
Identify and eliminate any double inversions.



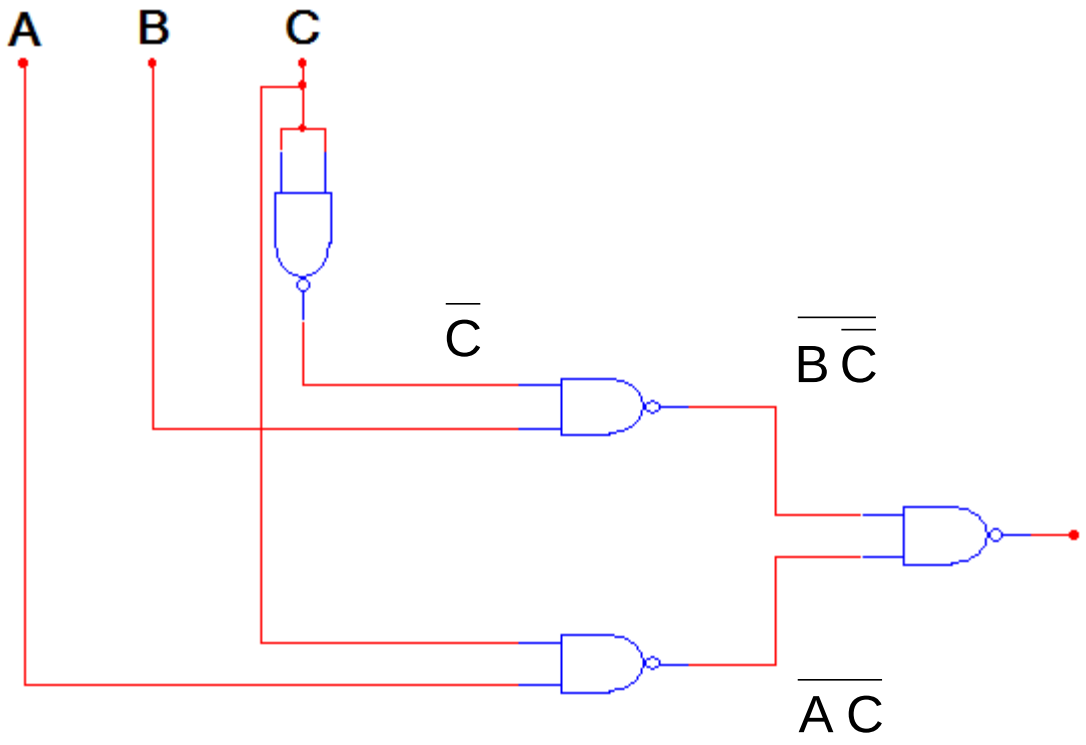
NAND Implementation

Solution – Step 5

Redraw the circuit.



Proof of Equivalence

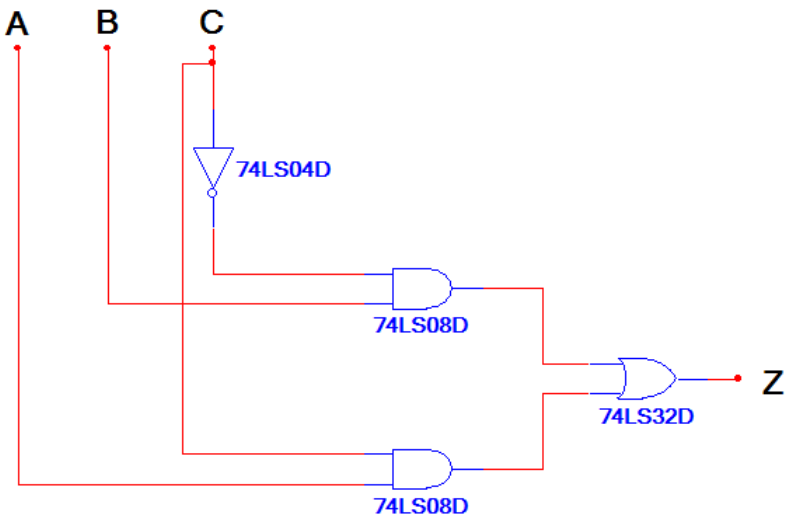


$$Z = \overline{\overline{B\,\overline{C}}\;\overline{A\,C}}$$

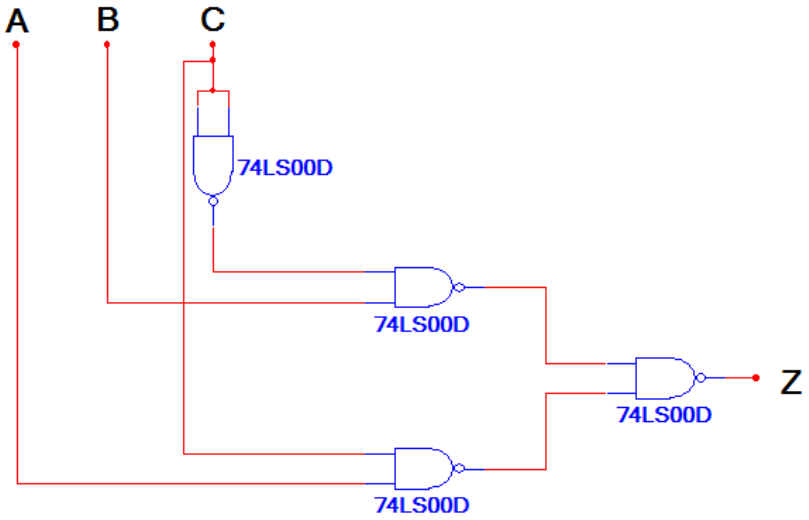
$$Z = \overline{\overline{B\,\overline{C}}} + \overline{\overline{A\,C}}$$

$$Z = B\,\overline{C} + A\,C$$

AOI vs. NAND



IC Type	Gates	Gate / IC	# ICs
74LS04	1	6	1
74LS08	2	4	1
74LS32	1	4	1
Total Number of ICs →			3



IC Type	Gates	Gate / IC	# ICs
74LS00	4	4	1
Total Number of ICs →			1