WICHITA STATE UNIVERSITY

CS 194: Introduction to Digital Design, Fall 2017

Instructor:	Manira Rani
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Preferred Method of Contact:	During office hours or right after class or email
Office Hours:	Mon & Wednesday 10:00-12:00 am
Classroom; Days/Time:	123 Wallace Hall; T, R: 8:00-9:15 pm.
Lab:	EE 262 W: 3:45-6:15pm and 7:20- 9:50 pm EE 262 R: 9:45-12:15
Prerequisites:	MATH 111

General University Policies

Some general university policies pertaining to all syllabi can be found at:

https://webs.wichita.edu/?u=ofdss&p=/students/syllabusinformation/

Academic Honesty

Students are responsible for knowing and following the Student Code of Conduct http://webs.wichita.edu/inaudit/ch8_05.htm and the Student Academic Honesty policy http://webs.wichita.edu/inaudit/ch2_17.htm.

All homework assignments in this course are individual assignments. You can discuss them with others, but you cannot write the solution together; your submission (wording) should be substantially different from others'. There will be severe consequences for academic dishonesty. This includes copying home works and cheating during exams. Cheating in any exam will automatically result in an F grade for the course; this applies to ALL the parties involved (including the ones who help/show). Be aware that I do NOT have to catch you (or even notice) cheating during the exam; I could catch you later, based on any unusual similarities in your answers.

Course Description

CS 194. Introduction to Digital Design (4). 3R; 2L. An introduction to digital design concepts. Includes number systems, Boolean algebra, Karnaugh maps, combinational circuit design, adders, multiplexers, decoders, sequential circuit design, state diagram, flip flops, sequence detectors and test different combinational and sequential circuits. Uses CAD tools for circuit simulation. Prerequisite: MATH 111 or equivalent.

Definition of a Credit Hour

Success in this 4 credit hour course is based on the expectation that students will spend, for each unit of credit, a minimum of 45 hours over the length of the course (normally 3 hours per unit per week with 1 of the hours used for lecture). Students will spend approximately 3 hours for instruction, 3 hours for labs, and another 6 hours for preparation/studying or other course related activities each week for a total of about 180 hours for the semester.

Measurable Student Learning Outcomes:

After passing this course, students will be able to:

1. Demonstrate knowledge of different digital logic gates used in the design of digital circuits.
2. Reduce digital circuits using Boolean algebra and Karnaugh maps to implement digital circuits efficiently with minimal gate count and interconnections.
3. Design digital circuits that use only NAND gates from a minimum Sum of Products expression.
4. Design digital circuits that use only NOR gates from a minimum Product of Sums expression.
5. Design larger combinational circuits like adders, decoders, multiplexers.
6. Design and analyze sequential digital circuits using combinational logic and memory elements like flip flops.
7. Design shift registers sequential counters and simple sequence generators.

Required Texts

DIGITAL DESIGN with an introduction to the Verilog HDL by M. Morris Mano and Michael D. Ciletti; Prentice Hall; 5th Ed.

Grading Scale

WSU uses a +/- grading scale for final grades and to calculate grade point averages.
The letter grades and the corresponding grade points are as follow:

A: 4.00 denotes excellent performance
A-: 3.70
B+:3.30
B: 3.00 denotes good performance
B-: 2.70
C+: 2.30
C: 2.00 denotes satisfactory performance
C-: 1.70
D+:1.30
D: 1.00 denotes unsatisfactory performance
D-: 0.70
F: 0.00 denotes failing performance

Grading Policy

Your letter grade will be based on the following components:

Home Work:	10%
Lab Assignments	20%
Exam I	15%
Exam II	15%
Exam III	15%
Exam IV	25%

Your final course grade will be approximately based on the following:

A	A-	B+	B	B-	C+	C	C-	D+	D	D-	F
93	90	87	83	80	77	73	70	67	63	60	50

Homework

Home works, and their exact due dates will be announced in class. Late assignments will not be accepted without strong reasons. Tentative schedule for the homework's are as follows:

Home Work 1: Chapter1, covers Outcome 1
Home Work 2: Chapter 2, covers Outcome2

Home Work 3: Chapter 2, cover Outcome 2 and 3
Home Work 4: Chapter 3, cover Outcome 2, 3 and 4
Home Work 5: Chapter 3, cover Outcome 2, 3 and 4
Home Work 6: Chapter 4, covers Outcome 5
Home Work 7: Chapter 4, covers Outcome 5
Home Work 8: Chapter 4, covers Outcome 5
Home Work 9: Chapter 5, covers Outcome 6
Home Work 10: Chapter 6, covers Outcome 7

Missed Exams

Makeup for missed exams will be given only when there is an emergency, with clear proof. It is your responsibility to provide the proof. It is also recommended that, you should talk to me before the exam.

Academic Dates

- August 22, 2017: First day of class
- TBD: Last day to withdraw from course with W ("withdrawn")
- December 7, 2017: Last day of class
- December 7, 2017: Final Exam
- December 9 - 14, 2017: Final exam week. For this course there is no final on the final week.

Tentative Schedule

Week	Date	Topics, Text book Chapters
1		Introduction and Overview Chapter 1: Digital Systems and Binary Numbers
2		More Number system and Number Codes
3		Chapter 2: Boolean Algebra and Logic Gates
4		More Boolean Algebra
5		More Logic Functions NAND NOR XOR
6		Chapter 3:Minimization with Karnaugh Maps
7		More Karnaugh Maps and Don't Cares
8		NAND and XOR Implementations
9		Chapter 4: Circuit Analysis Procedure
10		Chapter 4:Combinational Design Procedure
11		More on Combinational design Procedure: Binary Adders and Subtractors, Decoders, Multiplexers
12		Chapter 5: Sequential Circuits: Latches Sequential Circuits: Flip flops
13		Analyzing Sequential Circuits, Finite State Machine Design Procedure
14		Shift Registers, Counters
15		Review for Final and Final Exam