You are expected to solve homework problems individually. If needed, you may seek help from your friends. However, do not copy. Show all steps with your solutions for full credit.

**Name: / 50**

1. (4+2+2+2 points) Construct a truth table for a half-adder. Write reduced SOP expressions for the two outputs of a half-adder.
   1. Show algebraic expression in sum of minterms form
   2. Draw the circuit (half-adder) using **AND, OR and NOT** gates (do not use XOR gate).
   3. Design a NAND (or NOR) gate implementation for the circuit.
2. (2 + 8 points) Construct a truth table for a full-adder. Write reduced SOP expressions for the two outputs of a **full-adder**. [Show your work]
3. (1+1+8 points) Write the truth table for the **exclusive-OR (XOR) gate**.
4. Design a **half-adder** using XOR and AND gates. Draw the circuit.
5. Design a **full-adder** using XOR, AND and OR gates. Show that a full-adder can be built using two half-adders and one OR gate. Draw the circuit.
6. (10 points) Design a 4-bit adder/subtractor module. Please use the block diagram for the full adder.
7. (10 points) The adder–subtractor circuit has the following values for mode input *M* and data inputs *A* and *B.*

*M A B*

(a) 0 0111 0110

(b) 0 1000 1001

(c) 1 1100 1000

(d) 1 0101 1010

(e) 1 0000 0001

In each case, determine the values of the four *SUM* outputs, the carry *C,* and overflow *V.*