SSD1680

Product Preview

176 Source x 296 Gate Red/Black/White
Active Matrix EPD Display Driver with Controller

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Appendix: IC Revision history of SSD1680 Specification

Version	Change Items	Effective Date
0.10	Initial Release	28-Feb-19
0.11	Updated Feature list	02-Apr-19
0.12	Updated AC Characteristics Updated Component list	21-May-19
0.13	Updated Component list	24-May-19
0.14	Updated Component list, removed case size for C0 and C1.	5-Jun-19

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1 GENERAL DESCRIPTION

SSD1680 is an Active Matrix EPD display driver with controller for Red/Black/White EPD displays.

It consists of 176 source outputs, 296 gate outputs, 1 VCOM and 1VBD (for border), which can support displays with resolution up to 176x 296. In addition, SSD1680 has a cascade mode which provides two-chip solutions for displays with higher resolution.

In the SSD1680, data and commands are sent from MCU through hardware selectable serial peripheral interface. It has embedded booster, regulator and oscillator which is suitable for EPD display applications.

2 FEATURES

- Design for dot matrix type active matrix EPD display, support Red/Black/White color
- Resolution: 176 source outputs, 296 gate outputs, 1 VCOM and 1VBD (for border)
- Power supply:
    - VCI: 2.2 to 3.7V
    - VDDIO: Connect to VCI
    - VDD: 1.8V, regulate from VCI supply
- On chip display RAM
    - Mono B/W: 176x296 bits
    - Mono Red: 176x296 bits
- On-chip booster and regulator for generating VCOM, Gate and Source driving voltage
- Gate driving output voltage: 2-level outputs (VGH, VGL), Max 40Vp-p
    - VGH: 10V to 20V (Voltage adjustment step: 500mV)
    - VGL: -VGH (Voltage adjustment step: 500mV)
- Source / VBD driving output voltage: 4-levels outputs (VSH1, VSH2, VSS and VSL)
    - VSH1/VSH2: 2.4V to 17V (Voltage adjustment step: 100mV for 2.4V to 8.8V, 200mV for 8.8V to 17V)
    - VSL: -5V to -17V (Voltage adjustment step: 500mV)
- VCOM output voltage
    - DCVCOM: -3V to -0.2V in 100mV resolution
    - ACVCOM: 3-level outputs (VSH1+DCVCOM, DCVCOM, VSL+DCVCOM)
- On-chip oscillator, adjustable frame rate from 25Hz to 200Hz
- Programmable output Waveform Settings:
    - Individual setting of 5 LUT [LUT0~4]
        - VS: 2-bit per 4 phases
    - Common setting of 5 LUT
        - 48 phases (4 phases/group, 12 groups with repeat and state repeat function)
        - TP: Max. 255 frame/phase
        - RP: 1 to 256 times for repeat count
        - SR: 1 to 256 times for state repeat count; state repeat count for phase A,B and 1 state repeat count for phase C,D
        - FR: Selective Frame Rate for each group
        - XON: All Gate On Selection for each phase A,B and phase C,D
- Embedded OTP to store the waveform settings and parameters:
    - 36 sets of Waveform Settings (WS) including
        - waveform look up table (LUT),
        - Gate/Source voltage, VCOM value
        - Option for LUT end
    - 36 sets of Temperature Range (TR)
    - Display mode selection
    - 4-byte waveform version
    - 10-byte User ID
- Embedded OTP to store the init code setting
- External or internal generated voltage for burning OTP
- Built-in CRC checking method for RAM content and WS & TR in OTP
- Panel break diagnostic
- VCI low voltage detection
- Driving voltage ready detection
- Support display partial update

- Auto write RAM command for regular patterns
- Internal Temperature Sensor of +/-2degC accuracy from -25degC to 50degC
- I2C single master interface to communicate with external temperature sensor
- MCU interface: 4-wire or 3-wire Serial peripheral interface (maximum SPI write speed 20MHz)
- Cascade mode to support displays with higher resolution
- Available in COG package

3 ORDERING INFORMATION

Table 3-1 : Ordering Information

Ordering Part Number	Package Form	Remark
SSD1680Z	Gold Bump Die	Bump Face Up On Waffle pack Die thickness: 300um Bump height: 12um
SSD1680Z8	Gold Bump Die	Bump Face Down On Waffle pack Die thickness: 300um Bump height: 12um

4 BLOCK DIAGRAM

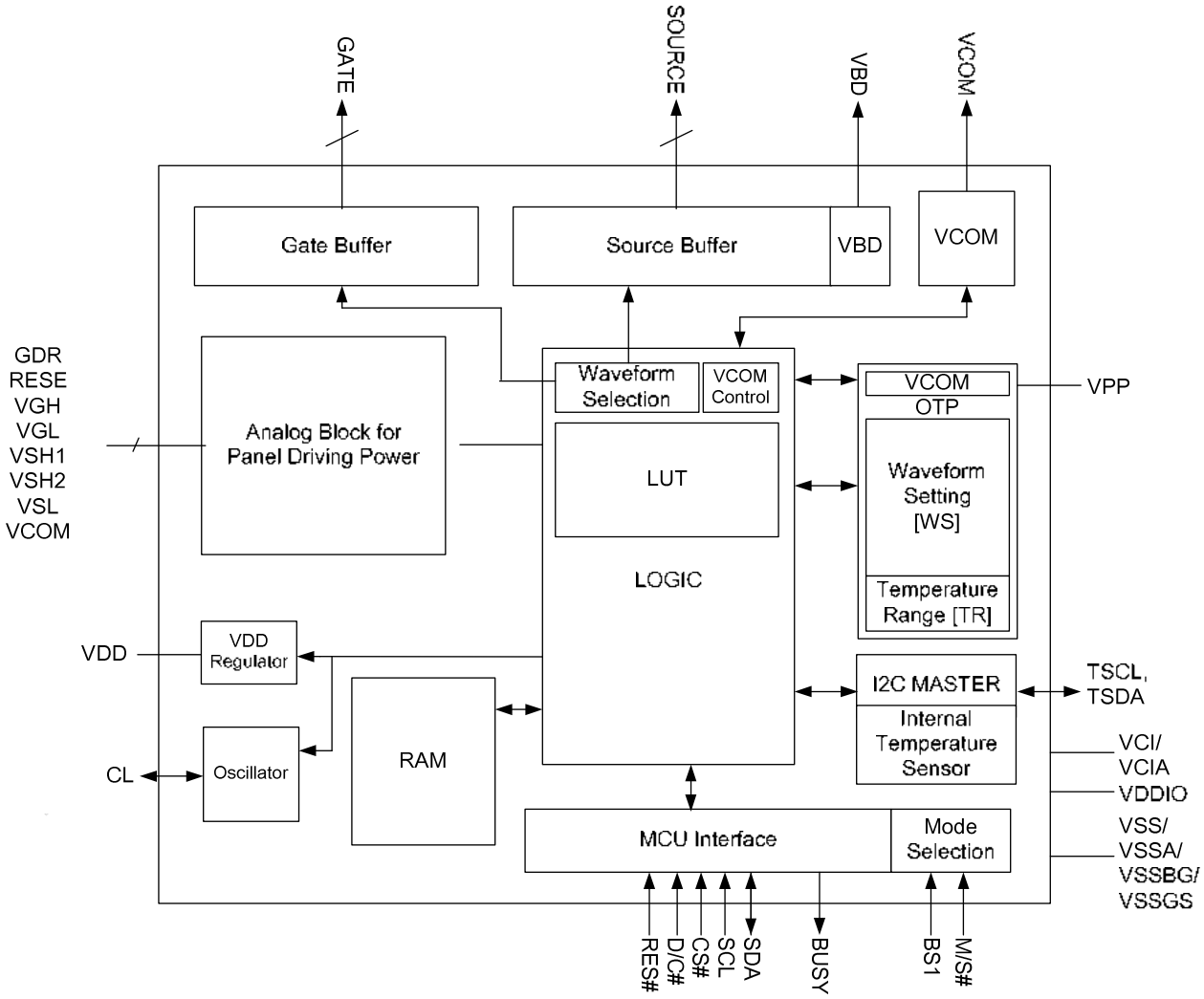


Figure 4-1 : SSD1680 Block Diagram

5 PIN DESCRIPTION

Key:

I = Input
O =Output
IO = Bi-directional (input/output)
P = Power pin
C = Capacitor Pin
NC = Not Connected

Table 5-1: Power Supply Pins

Name	Type	Connect to	Function	Description	When not in use
VCI	P	Power Supply	Power Supply	Power input pin for the chip.	-
VCIA	P	Power Supply	Power Supply	Power input pin for the chip. - Connect to VCI in the application circuit.	-
VDDIO	P	Power Supply	Power for interface logic pins	Power input pin for the Interface. - Connect to VCI in the application circuit.	-
VDD	P	Capacitor	Regulator output	Core logic power pin VDD can be regulated internally from VCI. - For the single chip application, a capacitor should be connected between VDD and VSS under all circumstances. - For the cascade mode application, a capacitor should be connected between VDD and VSS in the master chip under all circumstances. For the slave chip, the capacitor is not necessary as VDD will be supplied from the cascade master chip externally.	-
VSS	P	VSS	GND	Ground (Digital).	-
VSSA	P	VSS	GND	Ground (Analog) - Connect to VSS in the application circuit.	-
VSSBG	P	VSS	GND	Ground (Reference) pin. - Connect to VSS in the application circuit.	-
VSSGS	P	VSS	GND	Ground (Output) pin. - Connect to VSS in the application circuit.	-
VPP	P	Power Supply	OTP power	Power Supply for OTP Programming.	Open

Table 5-2: Interface Logic Pins

<table>
<tr><th>Name</th><th>Type</th><th>Connect to</th><th>Function</th><th>Description</th><th>When not in use</th></tr>
<tr><td>SCL</td><td>I</td><td>MPU</td><td>Data Bus</td><td>This pin is serial clock pin for interface.
Refer to MCU interface in Section 6.1.</td><td>-</td></tr>
<tr><td>SDA</td><td>I/O</td><td>MPU</td><td>Data Bus</td><td>This pin is serial data pin for interface.
Refer to MCU interface in Section 6.1.</td><td>-</td></tr>
<tr><td>CS#</td><td>I</td><td>MPU</td><td>Logic Control</td><td>This pin is the chip select input connecting to the MCU. Refer to MCU interface in Section 6.1.</td><td>VDDIO or VSS</td></tr>
<tr><td>D/C#</td><td>I</td><td>MPU</td><td>Logic Control</td><td>This pin is Data/Command control pin connecting to the MCU. Refer to MCU interface in Section 6.1.</td><td>VDDIO or VSS</td></tr>
<tr><td>RES#</td><td>I</td><td>MPU</td><td>System Reset</td><td>This pin is reset signal input.
Active Low.</td><td>-</td></tr>
<tr><td>BUSY</td><td>O</td><td>MPU</td><td>Device Busy Signal</td><td>This pin is Busy state output pin.
When Busy is High, the operation of the chip should not be interrupted, and command should not be sent.
For example., The chip would output Busy pin as High when
- Outputting display waveform; or
- Programming with OTP
- Communicating with digital temperature sensor

In the cascade mode, the BUSY pin of the slave chip should be left open.</td><td>Open</td></tr>
<tr><td>M/S#</td><td>I</td><td>VDDIO/VSS</td><td>Cascade Mode Selection</td><td>This pin is Master and Slave selection pin.
- For the single chip application, the M/S# pin should be connected to VDDIO.
- In the cascade mode:
For Master Chip, the M/S# pin should be connected to VDDIO.
For Slave Chip, the M/S# pin should be connected to VSS. The oscillator, booster and regulator circuits of the slave chip will be disabled. The corresponding pins including CL, VDD, VDDIO, VGH, VGL, VSH1, VSH2, VSL and VCOM must be connected to the master chip.</td><td>-</td></tr>
<tr><td>CL</td><td>I/O</td><td>NC</td><td>Clock signal</td><td>This pin is the clock signal pin.
- For the single chip application, the CL pin should be left open.
- In the cascade mode, the CL pin of the slave chip should be connected to the CL pin of the master chip.</td><td>Open</td></tr>
<tr><td>BS1</td><td>I</td><td>VDDIO/VSS</td><td>MCU Interface Mode Selection</td><td>This pin is for selecting 3-wire or 4-wire SPI bus.
<table><tr><th>BS1</th><th>MCU Interface</th></tr><tr><td>L</td><td>4-wire SPI</td></tr><tr><td>H</td><td>3-wire SPI (9-bit SPI)</td></tr></table></td><td>-</td></tr>
<tr><td>TSDA</td><td>I/O</td><td>Temperature sensor SDA</td><td>Interface to Digital Temp. Sensor</td><td>This pin is I^2C Interface to digital temperature sensor Data pin.
External pull up resistor is required when connecting to I^2C slave.</td><td>Open</td></tr>
<tr><td>TSCL</td><td>O</td><td>Temperature sensor SCL</td><td>Interface to Digital Temp. Sensor</td><td>This pin is I^2C Interface to digital temperature sensor Clock pin.
External pull up resistor is required when connecting to I^2C slave.</td><td>Open</td></tr>
</table>

Table 5-3: Analog Pins

Name	Type	Connect to	Function	Description	When not in use
GDR	O	POWER MOSFET Driver Control	VGH, VGL Generation	This pin is N-Channel MOSFET gate drive control pin.	-
RESE	I	Booster Control Input		This pin is Current sense input pin for the control Loop.	-
VGH	C	Stabilizing capacitor		This pin is Positive Gate driving voltage. Connect a stabilizing capacitor between VGH and VSS in the application circuit.	-
VGL	C	Stabilizing capacitor		This pin is Negative Gate driving voltage. Connect a stabilizing capacitor between VGL and VSS in the application circuit.	-
VSH1	C	Stabilizing capacitor	VSH1, VSH2, VSL Generation	This pin is Positive Source driving voltage, VSH1 Connect a stabilizing capacitor between VSH1 and VSS in the application circuit.	-
VSH2	C	Stabilizing capacitor		This pin is Positive Source driving voltage, VSH2 Connect a stabilizing capacitor between VSH2 and VSS in the application circuit.	
VSL	C	Stabilizing capacitor		This pin is Negative Source driving voltage. Connect a stabilizing capacitor between VSL and VSS in the application circuit.	-
VCOM	C	Panel/ Stabilizing capacitor	VCOM Generation	This pins is VCOM driving voltage Connect a stabilizing capacitor between VCOM and VSS in the application circuit.	-

Table 5-4: Driver Output Pins

Name	Type	Connect to	Function	Description	When not in use
S [175:0]	O	Panel	Source driving signal	Source output pin.	Open
G [295:0]	O	Panel	Gate driving signal	Gate output pin.	Open
VBD	O	Panel	Border driving signal	Border output pin.	Open

Table 5-5: Miscellaneous Pins

Name	Type	Connect to	Function	Description	When not in use
NC	NC	NC	Not Connected	This is dummy pin. It should not be connected with other NC pins.	Open
RSV	NC	NC	Reserved	This is a reserved pin and should be kept open.	Open
TPA, TPB, TPC, TPD, TPF, FB	NC	NC	Reserved for Testing	Reserved pins. - Keep open. - Do not connect to other NC pins and test pins including TPA, TPB, TPC, TPD, TPE, TPF, TIN and FB.	Open
TIN	I	NC	Reserved for Testing	This is a reserved pin and should be kept open.	Open
TPE	O	NC	Reserved for Testing	This is a reserved pin and should be kept open.	Open

6 Functional Block Description

6.1 MCU Interface

6.1.1 MCU Interface selection

The SSD1680 can support 3-wire/4-wire serial peripheral. MCU interface is pin selectable by BS1 shown in Table 6-1.

Table 6-1 : Interface pins assignment under different MCU interface

	Pin Name					
MCU Interface	**BS1**	**RES#**	**CS#**	**D/C#**	**SCL**	**SDA**
4-wire serial peripheral interface (SPI)	L	RES#	CS#	DC#	SCL	SDA
3-wire serial peripheral interface (SPI) – 9 bits SPI	H	RES#	CS#	L	SCL	SDA

Note

(1) L is connected to V_{SS} and H is connected to V_{DDIO}

6.1.2 MCU Serial Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCL, serial data SDA, D/C# and CS#. The control pins status in 4-wire SPI in writing command/data is shown in Table 6-2 and the write procedure 4-wire SPI is shown in Table 6-2

Table 6-2 : Control pins status of 4-wire SPI

Function	SCL pin	SDA pin	D/C# pin	CS# pin
Write command	↑	Command bit	L	L
Write data	↑	Data bit	H	L

Note:

(1) L is connected to VSS and H is connected to VDDIO
(2) ↑ stands for rising edge of signal
(3) SDA (Write Mode) is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0. The level of D/C# should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM (RAM)/Data Byte register or command Byte register according to D/C# pin.

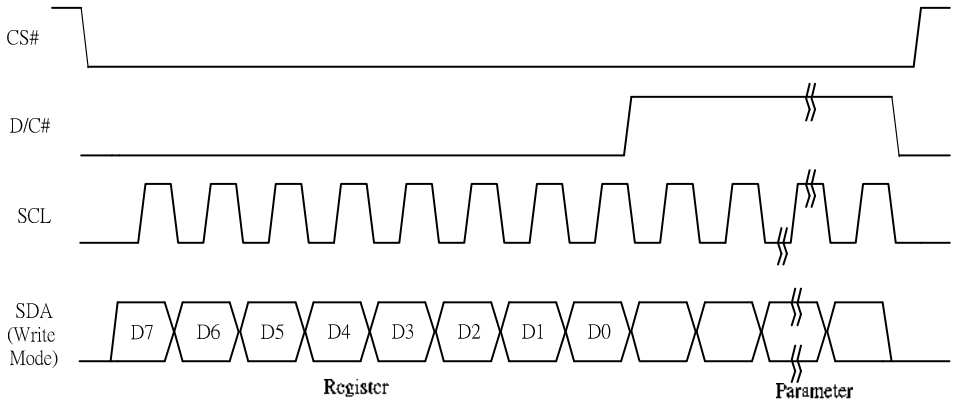


Figure 6-1 : Write procedure in 4-wire SPI mode

In the read operation (Command 0x1B, 0x27, 0x2D, 0x2E, 0x2F, 0x35). After CS# is pulled low, the first byte sent is command byte, D/C# is pulled low. After command byte sent, the following byte(s) read are data byte(s), so D/C# bit is then pulled high. An 8-bit data will be shifted out on every clock falling edge. The serial data SDA bit shifting sequence is D7, D6, to D0 bit. Figure 6-2 shows the read procedure in 4-wire SPI.

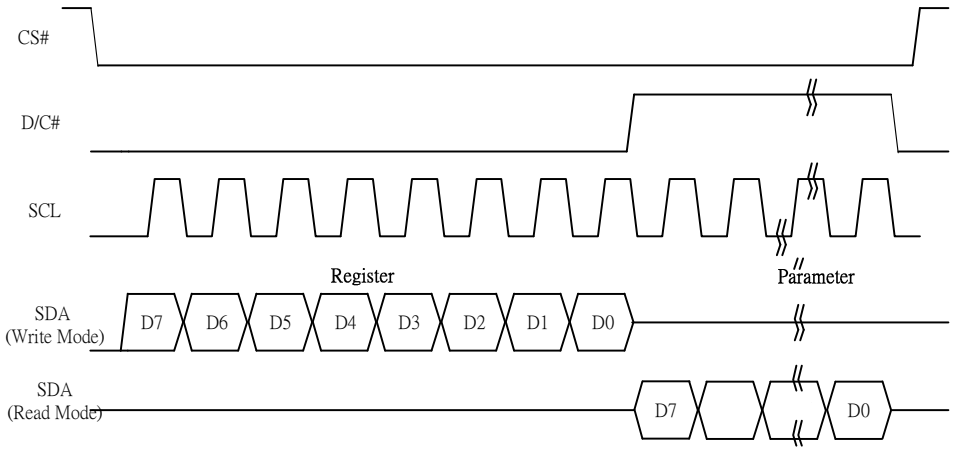


Figure 6-2 : Read procedure in 4-wire SPI mode

6.1.3 MCU Serial Peripheral Interface (3-wire SPI)

The 3-wire SPI consists of serial clock SCL, serial data SDA and CS#. The operation is similar to 4-wire SPI while D/C# pin is not used and it must be tied to LOW. The control pins status in 3-wire SPI is shown in Table 6-3.

In the write operation, a 9-bit data will be shifted into the shift register on every clock rising edge. The bit shifting sequence is D/C# bit, D7 bit, D6 bit to D0 bit. The first bit is D/C# bit which determines the following byte is command or data. When D/C# bit is 0, the following byte is command. When D/C# bit is 1, the following byte is data. Table 6-3 shows the write procedure in 3-wire SPI

Table 6-3 : Control pins status of 3-wire SPI

Function	SCL pin	SDA pin	D/C# pin	CS# pin
Write command	↑	Command bit	Tie LOW	L
Write data	↑	Data bit	Tie LOW	L

Note:

(1) L is connected to V_{SS} and H is connected to V_{DDIO}

(2) ↑ stands for rising edge of signal

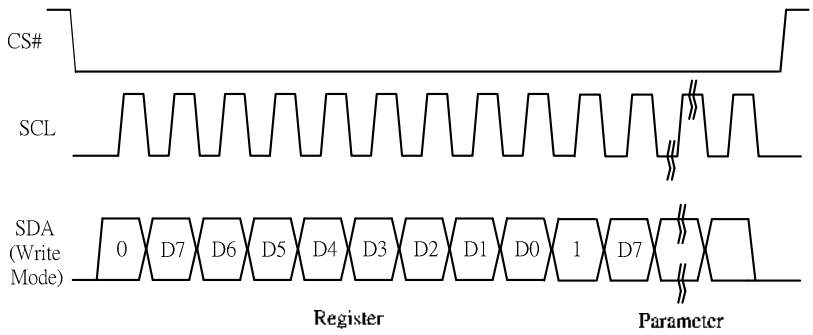


Figure 6-3 : Write procedure in 3-wire SPI

In the read operation (Register 0x1B, 0x27, 0x2D, 0x2E, 0x2F, 0x35). SDA data are transferred in the unit of 9 bits. After CS# pull low, the first byte is command byte, the D/C# bit is as 0 and following with the register byte. After command byte send, the following byte(s) are data byte(s), with D/C# bit is 1. After D/C# bit sending from MCU, an 8-bit data will be shifted out on every clock falling edge. The serial data SDA bit shifting sequence is D7, D6, to D0 bit. Figure 6-4 shows the read procedure in 3-wire SPI.

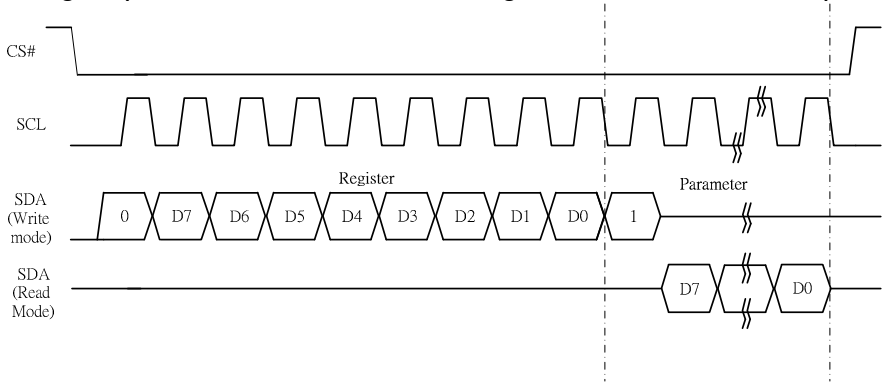


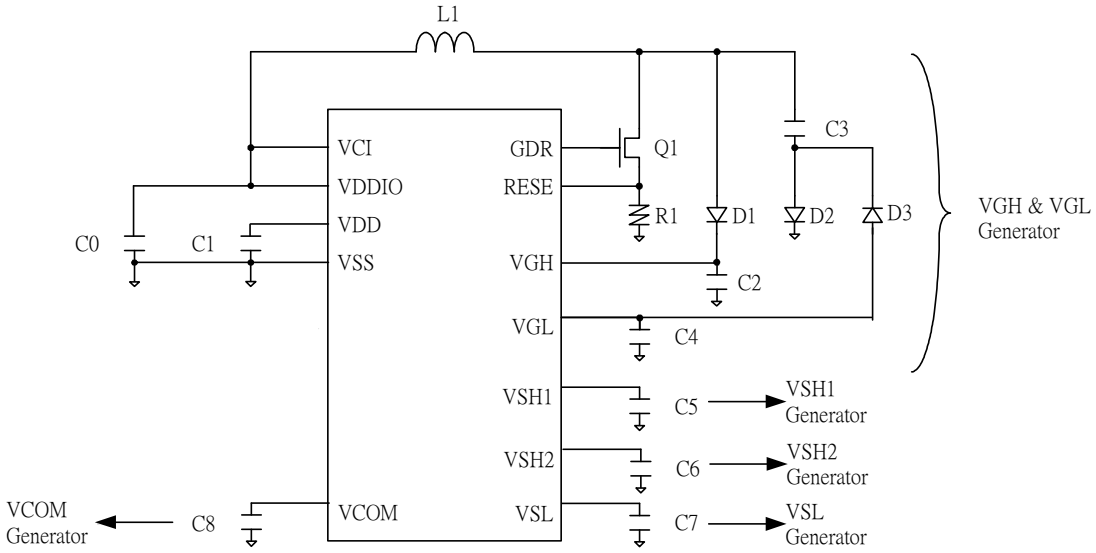
Figure 6-4 : Read procedure in 3-wire SPI mode

6.2 OSCILLATOR

The oscillator module generates the clock reference for waveform timing and analog operations.

6.3 BOOSTER & REGULATOR

A voltage generation system is included in the driver. It provides all necessary driving voltages required for an AMEPD panel including VGH, VGL, VSH1, VSH2, VSL and VCOM. External application circuit is needed to make the on-chip booster & regulator circuit work properly.



6.4 VCOM SENSING

This functional block provides the scheme to select the optimal VCOM DC level. The sensed value can be programmed into OTP.

The flow of VCOM sensing:

- Active Gate is scanning during the VCOM sense Period.
- Source are VSS.
- VCOM pin used for sensing.
- During Sensing period, BUSY is high.
- After Sensing, Active Gate return to non-select stage.

6.5 RAM

The On chip display RAM is holding the image data.
1 set of RAM is built for Mono B/W. The RAM size is 176x296 bits.
1 set of RAM is built for Mono Red. The RAM size is 176x296 bits.

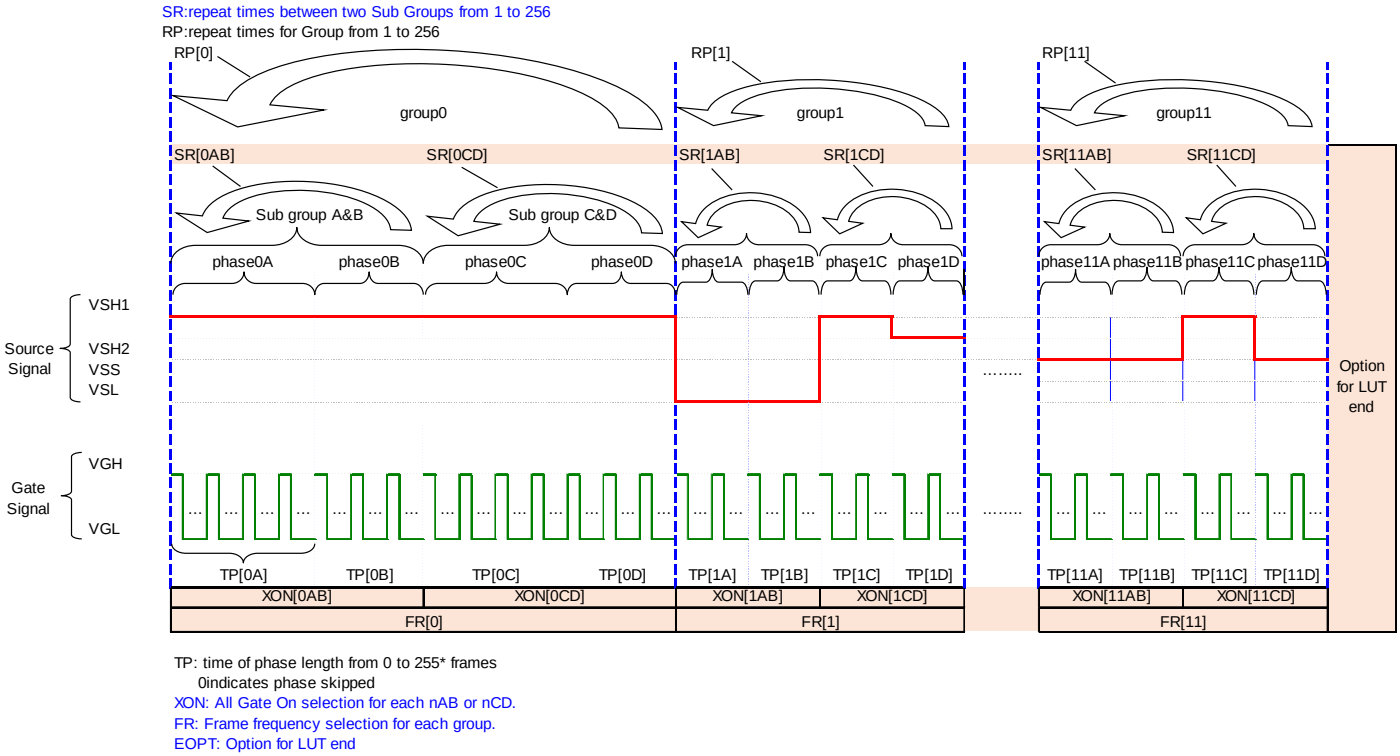
Table 6-4 : RAM bit and LUT mapping for 3-color display

Data bit in R RAM	Data bit in B/W RAM	Image Color	LUT
0	0	Black	LUT 0 for driving Black
0	1	White	LUT 1 for driving White
1	0	Red	LUT 2 for driving Red
1	1	Red	LUT 3 = LUT2

Table 6-5 : RAM bit and LUT mapping for black/white display

Data bit in R RAM	Data bit in B/W RAM	Image Color	LUT
0	0	Black	LUT 0 for driving Black
0	1	White	LUT 1 for driving White
1	0	Black	LUT 2 = LUT0
1	1	White	LUT 3 = LUT1

6.6 Programmable Waveform for Gate, Source and VCOM



TP: time of phase length from 0 to 255* frames
0indicates phase skipped
XON: All Gate On selection for each nAB or nCD.
FR: Frame frequency selection for each group.
EOPT: Option for LUT end

Figure 6-5 : Gate waveform and Programmable Source and VCOM waveform illustration

In the programmable waveform for Source and VCOM, there are 12 groups (Group0 to Group11) and each group has 4 phases (Phase A to Phase D) and 2 state repeats (Phase A and B, Phase C and D). Totally, there are 48 phases. In addition, in each phase, the phase length (TP[nX]) can be set by number of frame from 0 to 255 frames. Also, each group can be repeated with repeat counting number (RP[n]) from 1 to 256 times; each AB / CD phases can be repeated with state repeat counting number (SR[nAB]/SR[nCD]) from 1 to 256 times. For the voltage, there is four levels for Source voltage (VSS, VSH1, VSH2, VSL) and three levels for VCOM voltage (DCVCOM, VSH1+DCVCOM, VSL+DCVOM).

The description of each parameter is as follows.

1) TP[nX] represents the phase length set by the number of frame.
- The range of TP[nX] is from 0 to 255.
- n represents the Group number from 0 to 11; X represents the phase number from A to D.
- When TP[nX] = 0, the phase is skipped. When TP[nX] = 1, the phase is 1 frame, and so on. The maximum phase length is 255 frame.

2) RP[n] represents the repeat counting number for the Group.
- The range of RP[n] is from 0 to 255.
- n represents the Group number from 0 to 11.
- RP[n] = 0 indicates that the repeat times =1, RP[n] = 1 indicates that the repeat times = 2, and so on. The maximum repeat times is 256.

3) SR[nAB] and SR[nCD] represent the state repeat counting number for Phase A & B and Phase C & D respectively.
- The range of SR[nXY] is from 0 to 255.
- n represents the Group number from 0 to 11.
- SR[nXY] = 0 indicates that the repeat times =1, SR[nXY] = 1 indicates that the repeat times = 2, and so on. The maximum repeat times is 256.

4) VS[nX-LUTm] represents Source and VCOM voltage level which is used in each phase. Table 6-6 shows the voltage settings for source voltage and VCOM voltage.
- n represents the Group number from 0 to 11.
- m represents the LUT number from 0-4.

Table 6-6 : VS[nX-LUTm] settings for Source voltage and VCOM voltage

VS[nX-LUTm]	Source voltage	VCOM voltage
00	VSS	DCVCOM
01	VSH1	VSH1 + DCVCOM
10	VSL	VSL + DCVCOM
11	VSH2	N/A

5) FR[n] indicates the frame rate of group n
- The range of FR [n] is from 0 to 7.
- n represents the Group number from 0 to 11.

6) XON[nAB] and XON[nCD], indicates the gate scan selection.
- n represents the Group number from 0 to 11.
- XON[nXY] = 0 indicates Normal gate scan in Phase[nX] & Phase[nY].
- XON[nXY] = 1 indicates All gate on, that Gate keeps High until the phase for normal gate scan, in Phase[nX] & Phase[nY].

6.7 WAVEFORM SETTING

As described in Section 6.6, parameters VS[nX-LUTm], TP[nX], RP[n], SR[nXY], FR[n] and XON[nXY] are used to define the driving waveform. In the SSD1680, there are 159 bytes in the waveform setting to store LUT0, LUT1, LUT2, LUT3 and LUT4, gate voltage, source voltage and frame rate. The waveform LUT of a particular temperature range can be loaded from OTP or written by MCU.

- WS byte 0~152, the content of VS[nX-LUTm], TP[nX], RP[n], SR[nXY], FR[n] and XON[nXY] are defined by Register 0x32
- WS byte 153, the content of Option for LUT end, is the parameter belonging to Register 0x3F.
- WS byte 154, the content of gate level, is the parameter defined by Register 0x03.
- WS byte 155~157, the content of source level, is the parameter defined by Register 0x04.
- WS byte 158, the content of VCOM level, is the parameter defined by Register 0x2C.

The SSD1680 waveform setting is shown in Figure 6-6 : Waveform Setting mapping

addr.	D7	D6	D5	D4	D3	D2	D1	D0
0	VS[0A-L0]		VS[0B-L0]		VS[0C-L0]		VS[0D-L0]	
1	VS[1A-L0]		VS[1B-L0]		VS[1C-L0]		VS[1D-L0]	
2	VS[2A-L0]		VS[2B-L0]		VS[2C-L0]		VS[2D-L0]	
3	VS[3A-L0]		VS[3B-L0]		VS[3C-L0]		VS[3D-L0]	
4	VS[4A-L0]		VS[4B-L0]		VS[4C-L0]		VS[4D-L0]	
5	VS[5A-L0]		VS[5B-L0]		VS[5C-L0]		VS[5D-L0]	
6	VS[6A-L0]		VS[6B-L0]		VS[6C-L0]		VS[6D-L0]	
7	VS[7A-L0]		VS[7B-L0]		VS[7C-L0]		VS[7D-L0]	
8	VS[8A-L0]		VS[8B-L0]		VS[8C-L0]		VS[8D-L0]	
9	VS[9A-L0]		VS[9B-L0]		VS[9C-L0]		VS[9D-L0]	
10	VS[10A-L0]		VS[10B-L0]		VS[10C-L0]		VS[10D-L0]	
11	VS[11A-L0]		VS[11B-L0]		VS[11C-L0]		VS[11D-L0]	
12	VS[0A-L1]		VS[0B-L1]		VS[0C-L1]		VS[0D-L1]	
13	VS[1A-L1]		VS[1B-L1]		VS[1C-L1]		VS[1D-L1]	
14	VS[2A-L1]		VS[2B-L1]		VS[2C-L1]		VS[2D-L1]	
15	VS[3A-L1]		VS[3B-L1]		VS[3C-L1]		VS[3D-L1]	
16	VS[4A-L1]		VS[4B-L1]		VS[4C-L1]		VS[4D-L1]	
17	VS[5A-L1]		VS[5B-L1]		VS[5C-L1]		VS[5D-L1]	
18	VS[6A-L1]		VS[6B-L1]		VS[6C-L1]		VS[6D-L1]	
19	VS[7A-L1]		VS[7B-L1]		VS[7C-L1]		VS[7D-L1]	
20	VS[8A-L1]		VS[8B-L1]		VS[8C-L1]		VS[8D-L1]	
21	VS[9A-L1]		VS[9B-L1]		VS[9C-L1]		VS[9D-L1]	
22	VS[10A-L1]		VS[10B-L1]		VS[10C-L1]		VS[10D-L1]	
23	VS[11A-L1]		VS[11B-L1]		VS[11C-L1]		VS[11D-L1]	
24	VS[0A-L2]		VS[0B-L2]		VS[0C-L2]		VS[0D-L2]	
25	VS[1A-L2]		VS[1B-L2]		VS[1C-L2]		VS[1D-L2]	
26	VS[2A-L2]		VS[2B-L2]		VS[2C-L2]		VS[2D-L2]	
27	VS[3A-L2]		VS[3B-L2]		VS[3C-L2]		VS[3D-L2]	
28	VS[4A-L2]		VS[4B-L2]		VS[4C-L2]		VS[4D-L2]	
29	VS[5A-L2]		VS[5B-L2]		VS[5C-L2]		VS[5D-L2]	
30	VS[6A-L2]		VS[6B-L2]		VS[6C-L2]		VS[6D-L2]	
31	VS[7A-L2]		VS[7B-L2]		VS[7C-L2]		VS[7D-L2]	
32	VS[8A-L2]		VS[8B-L2]		VS[8C-L2]		VS[8D-L2]	
33	VS[9A-L2]		VS[9B-L2]		VS[9C-L2]		VS[9D-L2]	
34	VS[10A-L2]		VS[10B-L2]		VS[10C-L2]		VS[10D-L2]	
35	VS[11A-L2]		VS[11B-L2]		VS[11C-L2]		VS[11D-L2]	
36	VS[0A-L3]		VS[0B-L3]		VS[0C-L3]		VS[0D-L3]	
37	VS[1A-L3]		VS[1B-L3]		VS[1C-L3]		VS[1D-L3]	
38	VS[2A-L3]		VS[2B-L3]		VS[2C-L3]		VS[2D-L3]	
39	VS[3A-L3]		VS[3B-L3]		VS[3C-L3]		VS[3D-L3]	
40	VS[4A-L3]		VS[4B-L3]		VS[4C-L3]		VS[4D-L3]	
41	VS[5A-L3]		VS[5B-L3]		VS[5C-L3]		VS[5D-L3]	
42	VS[6A-L3]		VS[6B-L3]		VS[6C-L3]		VS[6D-L3]	
43	VS[7A-L3]		VS[7B-L3]		VS[7C-L3]		VS[7D-L3]	
44	VS[8A-L3]		VS[8B-L3]		VS[8C-L3]		VS[8D-L3]	
45	VS[9A-L3]		VS[9B-L3]		VS[9C-L3]		VS[9D-L3]	
46	VS[10A-L3]		VS[10B-L3]		VS[10C-L3]		VS[10D-L3]	
47	VS[11A-L3]		VS[11B-L3]		VS[11C-L3]		VS[11D-L3]	
48	VS[0A-L4]		VS[0B-L4]		VS[0C-L4]		VS[0D-L4]	
49	VS[1A-L4]		VS[1B-L4]		VS[1C-L4]		VS[1D-L4]	
50	VS[2A-L4]		VS[2B-L4]		VS[2C-L4]		VS[2D-L4]	
51	VS[3A-L4]		VS[3B-L4]		VS[3C-L4]		VS[3D-L4]	
52	VS[4A-L4]		VS[4B-L4]		VS[4C-L4]		VS[4D-L4]	
53	VS[5A-L4]		VS[5B-L4]		VS[5C-L4]		VS[5D-L4]	
54	VS[6A-L4]		VS[6B-L4]		VS[6C-L4]		VS[6D-L4]	
55	VS[7A-L4]		VS[7B-L4]		VS[7C-L4]		VS[7D-L4]	
56	VS[8A-L4]		VS[8B-L4]		VS[8C-L4]		VS[8D-L4]	
57	VS[9A-L4]		VS[9B-L4]		VS[9C-L4]		VS[9D-L4]	
58	VS[10A-L4]		VS[10B-L4]		VS[10C-L4]		VS[10D-L4]	
59	VS[11A-L4]		VS[11B-L4]		VS[11C-L4]		VS[11D-L4]	
60	TP[0A]							
61	TP[0B]							
62	SR[0AB]							
63	TP[0C]							
64	TP[0D]							
65	SR[0CD]							
66	RP[0]							
67	TP[1A]							
68	TP[1B]							
69	SR[1AB]							
70	TP[1C]							
71	TP[1D]							
72	SR[1CD]							
73	RP[1]							
74	TP[2A]							
75	TP[2B]							
76	SR[2AB]							
77	TP[2C]							
78	TP[2D]							
79	SR[2CD]							
80	RP[2]							

addr.	D7	D6	D5	D4	D3	D2	D1	D0
81	TP[3A]							
82	TP[3B]							
83	SR[3AB]							
84	TP[3C]							
85	TP[3D]							
86	SR[3CD]							
87	RP[3]							
88	TP[4A]							
89	TP[4B]							
90	SR[4AB]							
91	TP[4C]							
92	TP[4D]							
93	SR[4CD]							
94	RP[4]							
95	TP[5A]							
96	TP[5B]							
97	SR[5AB]							
98	TP[5C]							
99	TP[5D]							
100	SR[5CD]							
101	RP[5]							
102	TP[6A]							
103	TP[6B]							
104	SR[6AB]							
105	TP[6C]							
106	TP[6D]							
107	SR[6CD]							
108	RP[6]							
109	TP[7A]							
110	TP[7B]							
111	SR[7AB]							
112	TP[7C]							
113	TP[7D]							
114	SR[7CD]							
115	RP[7]							
116	TP[8A]							
117	TP[8B]							
118	SR[8AB]							
119	TP[8C]							
120	TP[8D]							
121	SR[8CD]							
122	RP[8]							
123	TP[9A]							
124	TP[9B]							
125	SR[9AB]							
126	TP[9C]							
127	TP[9D]							
128	SR[9CD]							
129	RP[9]							
130	TP[10A]							
131	TP[10B]							
132	SR[10AB]							
133	TP[10C]							
134	TP[10D]							
135	SR[10CD]							
136	RP[10]							
137	TP[11A]							
138	TP[11B]							
139	SR[11AB]							
140	TP[11C]							
141	TP[11D]							
142	SR[11CD]							
143	RP[11]							
144	FR[0]				FR[1]			
145	FR[2]				FR[3]			
146	FR[4]				FR[5]			
147	FR[6]				FR[7]			
148	FR[8]				FR[9]			
149	FR[10]				FR[11]			
150	XON[0AB]	XON[0CD]	XON[1AB]	XON[1CD]	XON[2AB]	XON[2CD]	XON[3AB]	XON[3CD]
151	XON[4AB]	XON[4CD]	XON[5AB]	XON[5CD]	XON[6AB]	XON[6CD]	XON[7AB]	XON[7CD]
152	XON[8AB]	XON[8CD]	XON[9AB]	XON[9CD]	XON[10AB]	XON[10CD]	XON[11AB]	XON[11CD]
153	EOPT							
154	VGH							
155	VSH1							
156	VSH2							
157	VSL							
158	VCOM							

Figure 6-6 : Waveform Setting mapping

6.8 Temperature Searching

The SSD1680 has internal temperature sensor to detect the environment temperature or can communicate with the external temperature sensor by I2C single master interface or can communicate with the external MCU to get the temperature value through SPI. In the SSD1680, there is a dedicated format for the temperature value so that the driver IC can understand it. The format of temperature value is described in Section 6.8.3.

6.8.1 Internal Temperature Sensor

The internal temperature sensor can be selected by command register. The accuracy of it is ±2degC from -25degC to 50degC.

6.8.2 External Temperature Sensor I2C Single Master Interface

The driver IC can communicate with the external temperature sensor through I2C single master interface (TSDA and TSCL). TSDA will be SDA and TSCL will be SCL. TSDA and TSCL are required to connect with external pull-up resistor. Temperature register value of external temperature sensor can be read by command register.

6.8.3 Format of temperature value

The temperature value is defined by 12-bit binary. The rules are shown as below.

- If the Temperature value MSByte bit D11 = 0, then
  the temperature is positive and value (DegC) = + (Temperature value) / 16
- If the Temperature value MSByte bit D11 = 1, then
  the temperature is negative and value (DegC) = - (2's complement of Temperature value) / 16

Table 6-7 shows some examples of 12-bit binary temperature value:

Table 6-7 : Example of 12-bit binary temperature settings for temperature ranges

12-bit binary (2's complement)	Hexadecimal Value	TR Value [DegC]
0111 1111 1111	7FF	128
0111 1111 1111	7FF	127.9
0110 0100 0000	640	100
0101 0000 0000	500	80
0100 1011 0000	4B0	75
0011 0010 0000	320	50
0001 1001 0000	190	25
0000 0000 0100	004	0.25
0000 0000 0000	000	0
1111 1111 1100	FFC	-0.25
1110 0111 0000	E70	-25
1100 1001 0000	C90	-55

6.9 Waveform Setting searching mechanism

As mentioned in Section 6.7, the SSD1680 OTP can store waveform setting and temperature range. If waveform setting and temperature range are programmed in OTP memory, corresponding waveform LUT can be selected according to the sensed temperature to drive the display. The Waveform Setting searching mechanism by driver IC is as follows.

1) Read temperature value by command register in the format of 12-bit binary.
2) According to read temperature and display mode selection, search LUT in OTP from TR0 to TR35 in sequence. The last match will be selected, then, the corresponding WS will be loaded in the LUT register to drive the display.

Remark: Waveform LUT selection criteria is "Lower temperature bound < Sensed temperature ≤ Upper temperature bound".

Table 6-8 shows an example for the waveform LUT searching from OTP:

- If the read temperature is 25degC, then, WS4 will be selected.
- If the read temperature is 34degC, then, WS7 will be selected. Although 34degC is also in the temperature range TR6, according to searching mechanism, the last match should be selected. Therefore, WS7 is selected.

Table 6-8 : Example of waveform settings selection based on temperature ranges.

Waveform LUT in OTP	Temperature Range in OTP	TR Lower Limit [Hex]	TR Upper Limit [Hex]	Temperature range in OTP
WS0	TR0	800	050	-128 DegC < Temperature ≤ 5 DegC
WS1	TR1	050	0A0	5 DegC < Temperature ≤ 10DegC
WS2	TR2	0A0	0F0	10 DegC < Temperature ≤ 15DegC
WS3	TR3	0F0	140	15 DegC < Temperature ≤ 20DegC
WS4	TR4	140	190	20 DegC < Temperature ≤ 25DegC
WS5	TR5	190	1E0	25 DegC < Temperature ≤ 30DegC
WS6	TR6	1E0	230	30 DegC < Temperature ≤ 35DegC
WS7	TR7	210	7FF	33 DegC < Temperature ≤ 127.9DegC
Others	Others	000	000	

Precaution:
Please ensure the temperature range covers whole range of application temperatures, display will not be updated if no suitable temperature range matches the sensed temperature.

6.10 One Time Programmable (OTP) Memory

In the SSD1680, there is an embedded OTP memory which is designed to store the waveform settings of different temperature range and some variables/parameters. The OTP memory can store 36 sets of waveform LUT settings (WS), 36 sets of temperature range (TR), VCOM value, display mode selection, waveform version and user ID. Figure 6 7 shows the address mapping of the 36 waveform setting (WS0 to WS35) and temperature range (TR0 to TR35).

addr.	D7	D6	D5	D4	D3	D2	D1	D0
0	WS0							
…								
158								
159	WS1							
…								
317								
318	WS2							
…								
476								
477	WS3							
…								
635								
636	WS4							
…								
794								
	…							
5406	WS34							
…								
5564								
5565	WS35							
…								
5723								
5724	TR0							
5725								
5726								
5727	TR1							
5728								
5729								
5730	TR2							
5731								
5732								
5733	TR3							
5734								
5735								
5736	TR4							
5737								
5738								
	…							
5826	TR34							
5827								
5828								
5829	TR35							
5830								
5831								

Figure 6-7 : The Waveform setting mapping in OTP for waveform setting and temperature range

6.11 The Format for Temperature Range (TR)

The format of TR Lower limit and Upper limit as shown in Figure 6-8 which temp_L[11:0] is the lower limit and temp_H[11:0] is the upper limit of the temperature range. There has 36sets of TR for waveform LUT searching.

D7	D6	D5	D4	D3	D2	D1	D0
temp_L[7:0]							
temp_H[3:0]				temp_L[11:8]			
temp_H[11:4]							

Figure 6-8 : Format of Temperature Range (TR) in OTP

6.12 Cascade Mode

SSD1680 has a cascade mode that can cascade 2 chips to achieve the display resolution up to 352 (sources) x 296 (gates). The pin M/S# is used to configure the chip. When M/S# is connected to VDDIO, the chip is configured as a master chip. When M/S# is connected to VSS, the chip is configured as a slave chip.

When the chip is configured as a master chip, it will be the same as a single chip application, ie, all circuit blocks will be worked as usual. When the chip is configured as a slave chip, its oscillator and booster & regulator circuit will be disabled. The oscillator clock and all booster voltages will be come from the master chip. Therefore, the corresponding pins including CL, VDD, VGH, VGL, VSH1, VSH2, VSL, VGL and VCOM must be connected to the master chip.

6.13 VCI Detection

The VCI detection function is used to detect the VCI level when it is lower than Vlow, threshold voltage set by register.

In SSD1680, there is a command to execute the VCI detection function. When the VCI detection command is issued, the VCI detection will be executed. During the detection period, BUSY output is at high level. BUSY output is at low level when the detection is completed. Then, user can issue the Status Bit Read command to check the status bit for the result of VCI, which 0 is normal, 1 is VCI<Vlow.

6.14 HV Ready Detection

The HV Ready detection function is used to detect whether the analog block is ready.

In SSD1680, there is a command to execute the HV Ready detection function. When the HV Ready detection command is issued, the HV Ready will be executed. During the detection period, BUSY output is at high level. BUSY output is at low level when the detection is completed. Then, user can issue the Status Bit Read command to check the status bit for the result of HV Ready, which 0 is normal, 1 indicate HV is not ready.

7 COMMAND TABLE

Table 7-1: Command Table

<table>
<tr><th colspan="12">Command Table</th></tr>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>01</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td rowspan="4">Driver Output control</td><td rowspan="4">Gate setting
A[8:0]= 127h [POR], 296 MUX
MUX Gate lines setting as (A[8:0] + 1).

B[2:0] = 000 [POR].
Gate scanning sequence and direction

B[2]: GD
Selects the 1st output Gate
GD=0 [POR],
G0 is the 1st gate output channel, gate output sequence is G0,G1, G2, G3, …
GD=1,
G1 is the 1st gate output channel, gate output sequence is G1, G0, G3, G2, …

B[1]: SM
Change scanning order of gate driver.
SM=0 [POR],
G0, G1, G2, G3…295 (left and right gate interlaced)
SM=1,
G0, G2, G4 …G294, G1, G3, …G295

B[0]: TB
TB = 0 [POR], scan from G0 to G295
TB = 1, scan from G295 to G0.</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_8</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>B_2</td><td>B_1</td><td>B_0</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>03</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td rowspan="2">Gate Driving voltage Control</td><td rowspan="2">Set Gate driving voltage
A[4:0] = 00h [POR]
VGH setting from 10V to 20V
<table><tr><td>A[4:0]</td><td>VGH</td><td>A[4:0]</td><td>VGH</td></tr><tr><td>00h</td><td>20</td><td>0Dh</td><td>15</td></tr><tr><td>03h</td><td>10</td><td>0Eh</td><td>15.5</td></tr><tr><td>04h</td><td>10.5</td><td>0Fh</td><td>16</td></tr><tr><td>05h</td><td>11</td><td>10h</td><td>16.5</td></tr><tr><td>06h</td><td>11.5</td><td>11h</td><td>17</td></tr><tr><td>07h</td><td>12</td><td>12h</td><td>17.5</td></tr><tr><td>08h</td><td>12.5</td><td>13h</td><td>18</td></tr><tr><td>07h</td><td>12</td><td>14h</td><td>18.5</td></tr><tr><td>08h</td><td>12.5</td><td>15h</td><td>19</td></tr><tr><td>09h</td><td>13</td><td>16h</td><td>19.5</td></tr><tr><td>0Ah</td><td>13.5</td><td>17h</td><td>20</td></tr><tr><td>0Bh</td><td>14</td><td>Other</td><td>NA</td></tr><tr><td>0Ch</td><td>14.5</td><td></td><td></td></tr></table></td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
</table>

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	04	0	0	0	0	0	1	0	0	Source Driving voltage Control	Set Source driving voltage A[7:0] = 41h [POR], VSH1 at 15V B[7:0] = A8h [POR], VSH2 at 5V. C[7:0] = 32h [POR], VSL at -15V Remark: VSH1>=VSH2
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		

A[7]/B[7] = 1,
VSH1/VSH2 voltage setting from 2.4V to 8.8V

A/B[7:0]	VSH1/VSH2	A/B[7:0]	VSH1/VSH2
8Eh	2.4	AFh	5.7
8Fh	2.5	B0h	5.8
90h	2.6	B1h	5.9
91h	2.7	B2h	6
92h	2.8	B3h	6.1
93h	2.9	B4h	6.2
94h	3	B5h	6.3
95h	3.1	B6h	6.4
96h	3.2	B7h	6.5
97h	3.3	B8h	6.6
98h	3.4	B9h	6.7
99h	3.5	BAh	6.8
9Ah	3.6	BBh	6.9
9Bh	3.7	BCh	7
9Ch	3.8	BDh	7.1
9Dh	3.9	BEh	7.2
9Eh	4	BFh	7.3
9Fh	4.1	C0h	7.4
A0h	4.2	C1h	7.5
A1h	4.3	C2h	7.6
A2h	4.4	C3h	7.7
A3h	4.5	C4h	7.8
A4h	4.6	C5h	7.9
A5h	4.7	C6h	8
A6h	4.8	C7h	8.1
A7h	4.9	C8h	8.2
A8h	5	C9h	8.3
A9h	5.1	CAh	8.4
AAh	5.2	CBh	8.5
ABh	5.3	CCh	8.6
ACh	5.4	CDh	8.7
ADh	5.5	CEh	8.8
AEh	5.6	Other	NA

A[7]/B[7] = 0,
VSH1/VSH2 voltage setting from 9V to 17V

A/B[7:0]	VSH1/VSH2	A/B[7:0]	VSH1/VSH2
23h	9	3Ch	14
24h	9.2	3Dh	14.2
25h	9.4	3Eh	14.4
26h	9.6	3Fh	14.6
27h	9.8	40h	14.8
28h	10	41h	15
29h	10.2	42h	15.2
2Ah	10.4	43h	15.4
2Bh	10.6	44h	15.6
2Ch	10.8	45h	15.8
2Dh	11	46h	16
2Eh	11.2	47h	16.2
2Fh	11.4	48h	16.4
30h	11.6	49h	16.6
31h	11.8	4Ah	16.8
32h	12	4Bh	17
33h	12.2	Other	NA
34h	12.4		
35h	12.6		
36h	12.8		
37h	13		
38h	13.2		
39h	13.4		
3Ah	13.6		
3Bh	13.8		

C[7] = 0,
VSL setting from -5V to -17V

C[7:0]	VSL
0Ah	
0Ch	-5.5
0Eh	-6
10h	-6.5
12h	-7
14h	-7.5
16h	-8
18h	-8.5
1Ah	-9
1Ch	-9.5
1Eh	-10
20h	-10.5
22h	-11
24h	-11.5
26h	-12
28h	-12.5
2Ah	-13
2Ch	-13.5
2Eh	-14
30h	-14.5
32h	-15
34h	-15.5
36h	-16
38h	-16.5
3Ah	-17
Other	NA

0	0	08	0	0	0	0	1	0	0	0	Initial Code Setting OTP Program	Program Initial Code Setting The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	09	0	0	0	0	1	0	0	1	Write Register for Initial Code Setting	Write Register for Initial Code Setting Selection A[7:0] ~ D[7:0]: Reserved Details refer to Application Notes of Initial Code Setting
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
0	0	0A	0	0	0	0	1	0	1	0	Read Register for Initial Code Setting	Read Register for Initial Code Setting

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	0C	0	0	0	0	1	1	0	0	Booster Soft start Control	Booster Enable with Phase 1, Phase 2 and Phase 3 for soft start current and duration setting. A[7:0] -> Soft start setting for Phase1 = 8Bh [POR] B[7:0] -> Soft start setting for Phase2 = 9Ch [POR] C[7:0] -> Soft start setting for Phase3 = 96h [POR] D[7:0] -> Duration setting = 0Fh [POR]
0	1		1	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		1	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		1	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	1		0	0	D_5	D_4	D_3	D_2	D_1	D_0		

Bit Description of each byte:
A[6:0] / B[6:0] / C[6:0]:

Bit[6:4]	Driving Strength Selection
000	1(Weakest)
001	2
010	3
011	4
100	5
101	6
110	7
111	8(Strongest)

Bit[3:0]	Min Off Time Setting of GDR [Time unit]
0000 ~ 0011	NA
0100	2.6
0101	3.2
0110	3.9
0111	4.6
1000	5.4
1001	6.3
1010	7.3
1011	8.4
1100	9.8
1101	11.5
1110	13.8
1111	16.5

D[5:0]: duration setting of phase
D[5:4]: duration setting of phase 3
D[3:2]: duration setting of phase 2
D[1:0]: duration setting of phase 1

Bit[1:0]	Duration of Phase [Approximation]
00	10ms
01	20ms
10	30ms
11	40ms

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	10	0	0	0	1	0	0	0	0	Deep Sleep mode	Deep Sleep mode Control: A[1:0] : Description 00 Normal Mode [POR] 01 Enter Deep Sleep Mode 1 11 Enter Deep Sleep Mode 2 After this command initiated, the chip will enter Deep Sleep Mode, BUSY pad will keep output high. Remark: To Exit Deep Sleep mode, User required to send HWRESET to the driver
0	1		0	0	0	0	0	0	A_1	A_0		
0	0	11	0	0	0	1	0	0	0	1	Data Entry mode setting	Define data entry sequence A[2:0] = 011 [POR] A [1:0] = ID[1:0] Address automatic increment / decrement setting The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00 –Y decrement, X decrement, 01 –Y decrement, X increment, 10 –Y increment, X decrement, 11 –Y increment, X increment [POR] A[2] = AM Set the direction in which the address counter is updated automatically after data are written to the RAM. AM= 0, the address counter is updated in the X direction. [POR] AM = 1, the address counter is updated in the Y direction.
0	1		0	0	0	0	0	A_2	A_1	A_0		
0	0	12	0	0	0	1	0	0	1	0	SW RESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode During operation, BUSY pad will output high. Note: RAM are unaffected by this command.

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	14	0	0	0	1	0	1	0	0	HV Ready Detection	HV ready detection A[7:0] = 00h [POR] The command required CLKEN=1 and ANALOGEN=1. Refer to Register 0x22 for detail. After this command initiated, HV Ready detection starts. BUSY pad will output high during detection. The detection result can be read from the Status Bit Read (Command 0x2F).
0	1		0	A_6	A_5	A_4	0	A_2	A_1	A_0		A[6:4]=n for cool down duration: 10ms x (n+1) A[2:0]=m for number of Cool Down Loop to detect. The max HV ready duration is 10ms x (n+1) x (m) HV ready detection will be trigger after each cool down time. The detection will be completed when HV is ready. For 1 shot HV ready detection, A[7:0] can be set as 00h.
0	0	15	0	0	0	1	0	1	0	1	VCI Detection	VCI Detection A[2:0] = 100 [POR] , Detect level at 2.3V A[2:0] : VCI level Detect A[2:0] / VCI level 011 / 2.2V 100 / 2.3V 101 / 2.4V 110 / 2.5V 111 / 2.6V Other / NA The command required CLKEN=1 and ANALOGEN=1 Refer to Register 0x22 for detail. After this command initiated, VCI detection starts. BUSY pad will output high during detection. The detection result can be read from the Status Bit Read (Command 0x2F).
0	1		0	0	0	0	0	A_2	A_1	A_0		
0	0	18	0	0	0	1	1	0	0	0	Temperature Sensor Control	Temperature Sensor Selection A[7:0] = 48h [POR], external temperatrure sensor A[7:0] = 80h Internal temperature sensor
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	1A	0	0	0	1	1	0	1	0	Temperature Sensor Control (Write to temperature register)	Write to temperature register. A[11:0] = 7FFh [POR]
0	1		A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4		
0	1		A_3	A_2	A_1	A_0	0	0	0	0		
0	0	1B	0	0	0	1	1	0	1	1	Temperature Sensor Control (Read from temperature register)	Read from temperature register.
1	1		A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4		
1	1		A_3	A_2	A_1	A_0	0	0	0	0		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	1C	0	0	0	1	1	1	0	0	Temperature Sensor Control (Write Command to External temperature sensor)	Write Command to External temperature sensor. A[7:0] = 00h [POR], B[7:0] = 00h [POR], C[7:0] = 00h [POR], A[7:6] A[7:6] – Select no of byte to be sent 00 – Address + pointer 01 – Address + pointer + 1st parameter 10 – Address + pointer + 1st parameter + 2nd pointer 11 – Address A[5:0] – Pointer Setting B[7:0] – 1st parameter C[7:0] – 2nd parameter The command required CLKEN=1. Refer to Register 0x22 for detail. After this command initiated, Write Command to external temperature sensor starts. BUSY pad will output high during operation.
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	0	20	0	0	1	0	0	0	0	0	Master Activation	Activate Display Update Sequence The Display Update Sequence Option is located at R22h. BUSY pad will output high during operation. User should not interrupt this operation to avoid corruption of panel images.
0	0	21	0	0	1	0	0	0	0	1	Display Update Control 1	RAM content option for Display Update A[7:0] = 00h [POR] B[7:0] = 00h [POR] A[7:4] Red RAM option 0000 – Normal 0100 – Bypass RAM content as 0 1000 – Inverse RAM content A[3:0] BW RAM option 0000 – Normal 0100 – Bypass RAM content as 0 1000 – Inverse RAM content B[7] Source Output Mode 0 – Available Source from S0 to S175 1 – Available Source from S8 to S167
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	0	0	0	0	0	0	0		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	22	0	0	1	0	0	0	1	0	Display Update Control 2	Display Update Sequence Option: Enable the stage for Master Activation A[7:0]= FFh (POR)
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

Operating sequence	Parameter (in Hex)
Enable clock signal	80
Disable clock signal	01
Enable clock signal ➔ Enable Analog	C0
Disable Analog ➔ Disable clock signal	03
Enable clock signal ➔ Load LUT with DISPLAY Mode 1 ➔ Disable clock signal	91
Enable clock signal ➔ Load LUT with DISPLAY Mode 2 ➔ Disable clock signal	99
Enable clock signal ➔ Load temperature value ➔ Load LUT with DISPLAY Mode 1 ➔ Disable clock signal	B1
Enable clock signal ➔ Load temperature value ➔ Load LUT with DISPLAY Mode 2 ➔ Disable clock signal	B9
Enable clock signal ➔ Enable Analog ➔ Display with DISPLAY Mode 1 ➔ Disable Analog ➔ Disable OSC	C7
Enable clock signal ➔ Enable Analog ➔ Display with DISPLAY Mode 2 ➔ Disable Analog ➔Disable OSC	CF
Enable clock signal ➔Enable Analog ➔ Load temperature value ➔ DISPLAY with DISPLAY Mode 1 ➔ Disable Analog ➔ Disable OSC	F7
Enable clock signal ➔Enable Analog ➔ Load temperature value ➔ DISPLAY with DISPLAY Mode 2 ➔ Disable Analog ➔ Disable OSC	FF

0	0	24	0	0	1	0	0	1	0	0	Write RAM (Black White) / RAM 0x24	After this command, data entries will be written into the BW RAM until another command is written. Address pointers will advance accordingly For Write pixel: Content of Write RAM(BW) = 1 For Black pixel: Content of Write RAM(BW) = 0

Command Table												
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	26	0	0	1	0	0	1	1	0	Write RAM (RED) / RAM 0x26	After this command, data entries will be written into the RED RAM until another command is written. Address pointers will advance accordingly. For Red pixel: Content of Write RAM(RED) = 1 For non-Red pixel [Black or White]: Content of Write RAM(RED) = 0
0	0	27	0	0	1	0	0	1	1	1	Read RAM	After this command, data read on the MCU bus will fetch data from RAM. According to parameter of Register 41h to select reading RAM0x24/ RAM0x26, until another command is written. Address pointers will advance accordingly. The 1st byte of data read is dummy data.
0	0	28	0	0	1	0	1	0	0	0	VCOM Sense	Enter VCOM sensing conditions and hold for duration defined in 29h before reading VCOM value. The sensed VCOM voltage is stored in register The command required CLKEN=1 and ANALOGEN=1 Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	29	0	0	1	0	1	0	0	1	VCOM Sense Duration	Stabling time between entering VCOM sensing mode and reading acquired. A[3:0] = 9h, duration = 10s. VCOM sense duration = (A[3:0]+1) sec
0	1		0	1	0	0	A_3	A_2	A_1	A_0		
0	0	2A	0	0	1	0	1	0	1	0	Program VCOM OTP	Program VCOM register into OTP The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	2B	0	0	1	0	1	0	1	1	Write Register for VCOM Control	This command is used to reduce glitch when ACVCOM toggle. Two data bytes D04h and D63h should be set for this command.
0	1		0	0	0	0	0	1	0	0		
0	1		0	1	1	0	0	0	1	1		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	2C	0	0	1	0	1	1	0	0	Write VCOM register	Write VCOM register from MCU interface A[7:0] = 00h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

A[7:0]	VCOM	A[7:0]	VCOM
08h	-0.2	44h	-1.7
0Ch	-0.3	48h	-1.8
10h	-0.4	4Ch	-1.9
14h	-0.5	50h	-2
18h	-0.6	54h	-2.1
1Ch	-0.7	58h	-2.2
20h	-0.8	5Ch	-2.3
24h	-0.9	60h	-2.4
28h	-1	64h	-2.5
2Ch	-1.1	68h	-2.6
30h	-1.2	6Ch	-2.7
34h	-1.3	70h	-2.8
38h	-1.4	74h	-2.9
3Ch	-1.5	78h	-3
40h	-1.6	Other	NA

0	0	2D	0	0	1	0	1	1	0	1	OTP Register Read for Display Option	Read Register for Display Option: A[7:0]: VCOM OTP Selection (Command 0x37, Byte A) B[7:0]: VCOM Register (Command 0x2C) C[7:0]~G[7:0]: Display Mode (Command 0x37, Byte B to Byte F) [5 bytes] H[7:0]~K[7:0]: Waveform Version (Command 0x37, Byte G to Byte J) [4 bytes]
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1	1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1	1		E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
1	1		F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0		
1	1		G_7	G_6	G_5	G_4	G_3	G_2	G_1	G_0		
1	1		H_7	H_6	H_5	H_4	H_3	H_2	H_1	H_0		
1	1		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0		
1	1		J_7	J_6	J_5	J_4	J_3	J_2	J_1	J_0		
1	1		K_7	K_6	K_5	K_4	K_3	K_2	K_1	K_0		

0	0	2E	0	0	1	0	1	1	1	0	User ID Read	Read 10 Byte User ID stored in OTP: A[7:0]]~J[7:0]: UserID (R38, Byte A and Byte J) [10 bytes]
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1	1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1	1		E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
1	1		F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0		
1	1		G_7	G_6	G_5	G_4	G_3	G_2	G_1	G_0		
1	1		H_7	H_6	H_5	H_4	H_3	H_2	H_1	H_0		
1	1		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0		
1	1		J_7	J_6	J_5	J_4	J_3	J_2	J_1	J_0		

Command Table												
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	2F	0	0	1	0	1	1	1	1	Status Bit Read	Read IC status Bit [POR 0x01] A[5]: HV Ready Detection flag [POR=0] 0: Ready 1: Not Ready A[4]: VCI Detection flag [POR=0] 0: Normal 1: VCI lower than the Detect level A[3]: [POR=0] A[2]: Busy flag [POR=0] 0: Normal 1: BUSY A[1:0]: Chip ID [POR=01] Remark: A[5] and A[4] status are not valid after RESET, they need to be initiated by command 0x14 and command 0x15 respectively.
1	1		0	0	A_5	A_4	0	0	A_1	A_0		
0	0	30	0	0	1	1	0	0	0	0	Program WS OTP	Program OTP of Waveform Setting The contents should be written into RAM before sending this command. The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	31	0	0	1	1	0	0	0	1	Load WS OTP	Load OTP of Waveform Setting The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	32	0	0	1	1	0	0	1	0	Write LUT register	Write LUT register from MCU interface [153 bytes], which contains the content of VS[nX-LUTm], TP[nX], RP[n], SR[nXY], FR[n] and XON[nXY] Refer to Session 6.7 WAVEFORM SETTING
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		:	:	:	:	:	:	:	:		
0	1		.	..	.	.	.	.	.	.		
0	0	34	0	0	1	1	0	1	0	0	CRC calculation	CRC calculation command For details, please refer to SSD1680 application note. BUSY pad will output high during operation.
0	0	35	0	0	1	1	0	1	0	1	CRC Status Read	CRC Status Read A[15:0] is the CRC read out value
1	1		A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8		
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

Command Table												
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	36	0	0	1	1	0	1	1	0	Program OTP selection	Program OTP Selection according to the OTP Selection Control [R37h and R38h] The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	37	0	0	1	1	0	1	1	1	Write Register for Display Option	Write Register for Display Option A[7] Spare VCOM OTP selection 0: Default [POR] 1: Spare B[7:0] Display Mode for WS[7:0] C[7:0] Display Mode for WS[15:8] D[7:0] Display Mode for WS[23:16] E[7:0] Display Mode for WS[31:24] F[3:0 Display Mode for WS[35:32] 0: Display Mode 1 1: Display Mode 2 F[6]: PingPong for Display Mode 2 0: RAM Ping-Pong disable [POR] 1: RAM Ping-Pong enable G[7:0]~J[7:0] module ID /waveform version. Remarks: 1) A[7:0]~J[7:0] can be stored in OTP 2) RAM Ping-Pong function is not support for Display Mode 1
0	1		A_7	0	0	0	0	0	0	0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
0	1		E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
0	1		0	F_6	0	0	F_3	F_2	F_1	F_0		
0	1		G_7	G_6	G_5	G_4	G_3	G_2	G_1	G_0		
0	1		H_7	H_6	H_5	H_4	H_3	H_2	H_1	H_0		
0	1		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0		
0	1		J_7	J_6	J_5	J_4	J_3	J_2	J_1	J_0		
0	0	38	0	0	1	1	1	0	0	0	Write Register for User ID	Write Register for User ID A[7:0]]~J[7:0]: UserID [10 bytes] Remarks: A[7:0]~J[7:0] can be stored in OTP
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
0	1		E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
0	1		F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0		
0	1		G_7	G_6	G_5	G_4	G_3	G_2	G_1	G_0		
0	1		H_7	H_6	H_5	H_4	H_3	H_2	H_1	H_0		
0	1		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0		
0	1		J_7	J_6	J_5	J_4	J_3	J_2	J_1	J_0		
0	0	39	0	0	1	1	1	0	0	1	OTP program mode	OTP program mode A[1:0] = 00: Normal Mode [POR] A[1:0] = 11: Internal generated OTP programming voltage Remark: User is required to EXACTLY follow the reference code sequences
0	1		0	0	0	0	0	0	A_1	A_0		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	3C	0	0	1	1	1	1	0	0	Border Waveform Control	Select border waveform for VBD A[7:0] = C0h [POR], set VBD as HIZ. A [7:6] :Select VBD option
0	1		A_7	A_6	A_5	A_4	0	A_2	A_1	A_0		

A[7:6]	Select VBD as
00	GS Transition, Defined in A[2] and A[1:0]
01	Fix Level, Defined in A[5:4]
10	VCOM
11[POR]	HiZ

A [5:4] Fix Level Setting for VBD

A[5:4]	VBD level
00	VSS
01	VSH1
10	VSL
11	VSH2

A[2] GS Transition control

A[2]	GS Transition control
0	Follow LUT (Output VCOM @ RED)
1	Follow LUT

A [1:0] GS Transition setting for VBD

A[1:0]	VBD Transition
00	LUT0
01	LUT1
10	LUT2
11	LUT3

0	0	3F	0	0	1	1	1	1	1	1	End Option (EOPT)	Option for LUT end A[7:0]= 02h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

22h	Normal.
07h	Source output level keep previous output before power off

0	0	41	0	1	0	0	0	0	0	1	Read RAM Option	Read RAM Option A[0]= 0 [POR] 0 : Read RAM corresponding to RAM0x24 1 : Read RAM corresponding to RAM0x26
0	1		0	0	0	0	0	0	0	A_0		
0	0	44	0	1	0	0	0	1	0	0	Set RAM X - address Start / End position	Specify the start/end positions of the window address in the X direction by an address unit for RAM A[5:0]: XSA[5:0], XStart, POR = 00h B[5:0]: XEA[5:0], XEnd, POR = 15h
0	1		0	0	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	B_5	B_4	B_3	B_2	B_1	B_0		
0	0	45	0	1	0	0	0	1	0	1	Set Ram Y- address Start / End position	Specify the start/end positions of the window address in the Y direction by an address unit for RAM A[8:0]: YSA[8:0], YStart, POR = 000h B[8:0]: YEA[8:0], YEnd, POR = 127h
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	A_8		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		0	0	0	0	0	0	0	B_8		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	46	0	1	0	0	0	1	1	0	Auto Write RED RAM for Regular Pattern	Auto Write RED RAM for Regular Pattern A[7:0] = 00h [POR] A[7]: The 1st step value, POR = 0 A[6:4]: Step Height, POR= 000 Step of alter RAM in Y-direction according to Gate
0	1		A_7	A_6	A_5	A_4	0	A_2	A_1	A_0		

A[6:4]	Height	A[6:4]	Height
000	8	100	128
001	16	101	256
010	32	110	296
011	64	111	NA

A[2:0]: Step Width, POR= 000
Step of alter RAM in X-direction according to Source

A[2:0]	Width	A[2:0]	Width
000	8	100	128
001	16	101	176
010	32	110	NA
011	64	111	NA

BUSY pad will output high during operation.

0	0	47	0	1	0	0	0	1	1	1	Auto Write B/W RAM for Regular Pattern	Auto Write B/W RAM for Regular Pattern A[7:0] = 00h [POR] A[7]: The 1st step value, POR = 0 A[6:4]: Step Height, POR= 000 Step of alter RAM in Y-direction according to Gate
0	1		A_7	A_6	A_5	A_4	0	A_2	A_1	A_0		

A[6:4]	Height	A[6:4]	Height
000	8	100	128
001	16	101	256
010	32	110	296
011	64	111	NA

A[2:0]: Step Width, POR= 000
Step of alter RAM in X-direction according to Source

A[2:0]	Width	A[2:0]	Width
000	8	100	128
001	16	101	176
010	32	110	NA
011	64	111	NA

During operation, BUSY pad will output high.

Command Table												
R/W#	**D/C#**	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	0	4E	0	1	0	0	1	1	1	0	Set RAM X address counter	Make initial settings for the RAM X address in the address counter (AC) A[5:0]: 00h [POR].
0	1		0	0	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	4F	0	1	0	0	1	1	1	1	Set RAM Y address counter	Make initial settings for the RAM Y address in the address counter (AC) A[8:0]: 000h [POR].
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	A_8		
0	0	7F	0	1	1	1	1	1	1	1	NOP	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read Commands.

8 COMMAND DESCRIPTION

8.1 Driver Output Control (01h)

This triple byte command has multiple configurations and each bit setting is described as follows:

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	MUX7	MUX6	MUX5	MUX4	MUX3	MUX2	MUX1	MUX0
POR		0	0	1	1	1	1	1	1
W	1								MUX8
POR									1
W	1						GD	SM	TB
POR							0	0	0

MUX[8:0]: Specify number of lines for the driver: MUX[8:0] + 1. Multiplex ratio (MUX ratio) from 16 MUX to 296MUX.

GD: Selects the 1st output Gate
This bit is made to match the GATE layout connection on the panel. It defines the first scanning line.

SM: Change scanning order of gate driver.
When SM is set to 0, left and right interlaced is performed.
When SM is set to 1, no splitting odd / even of the GATE signal is performed,
Output pin assignment sequence is shown as below (for 296 MUX ratio):

	SM=0	SM=0	SM=1	SM=1
Driver	GD=0	GD=1	GD=0	GD=1
G0	ROW0	ROW1	ROW0	ROW148
G1	ROW1	ROW0	ROW148	ROW0
G2	ROW2	ROW3	ROW1	ROW149
G3	ROW3	ROW2	ROW149	ROW1
:	:	:	:	:
G146	ROW146	ROW147	ROW73	ROW222
G147	ROW147	ROW146	ROW222	ROW73
G148	ROW148	ROW149	ROW74	ROW223
G149	ROW149	ROW148	ROW223	ROW74
:	:	:	:	:
G292	ROW292	ROW293	ROW146	ROW294
G293	ROW293	ROW292	ROW294	ROW146
G294	ROW294	ROW295	ROW147	ROW295
G295	ROW295	ROW294	ROW295	ROW147

See “Scan Mode Setting” on next page.

TB: Change scanning direction of gate driver.
This bit defines the scanning direction of the gate for flexible layout of signals in module either from up to down (TB = 0) or from bottom to up (TB = 1).

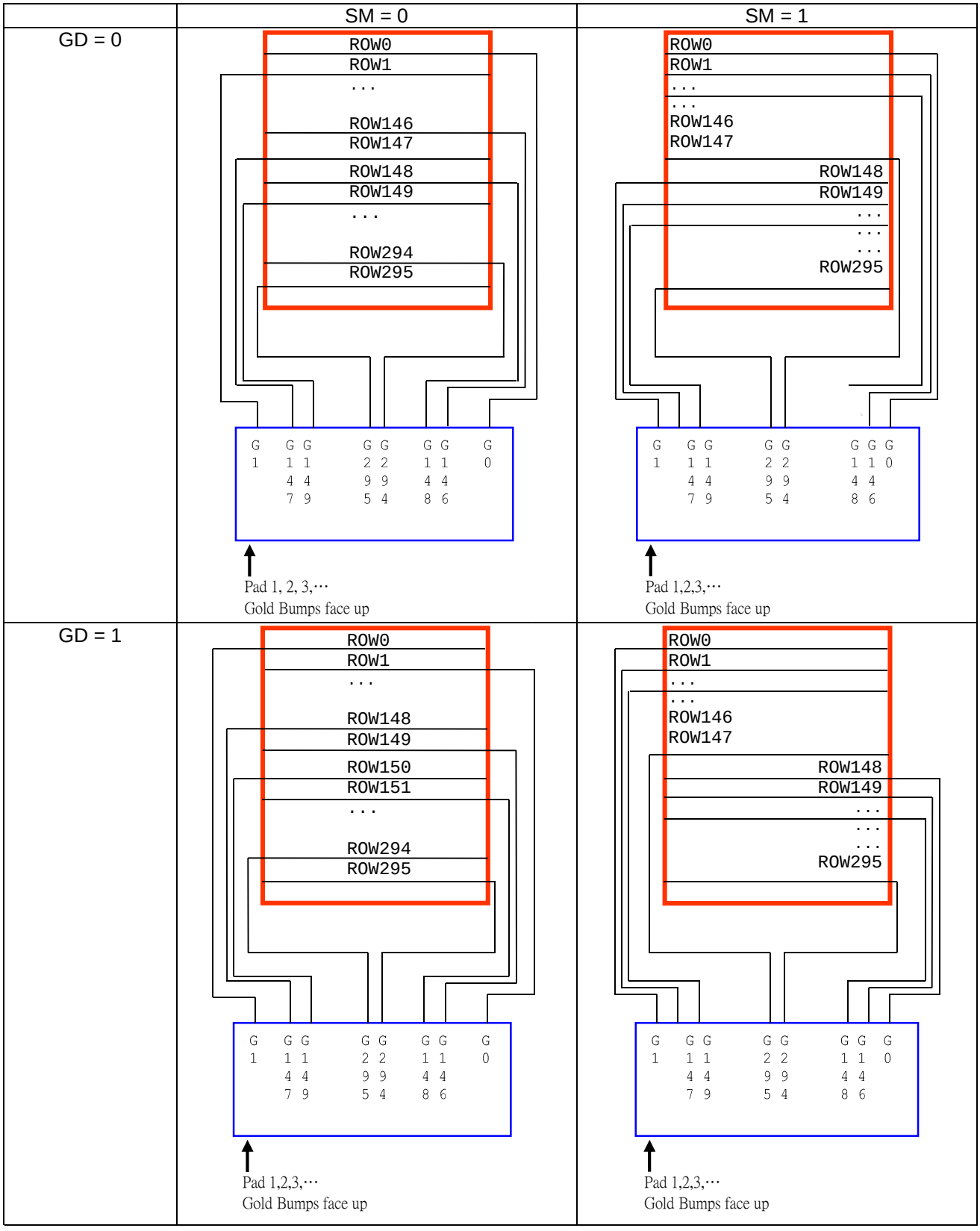


Figure 8-1: Output pin assignment on different Scan Mode Setting

8.2 Gate Scan Start Position (0Fh)

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
POR		0	0	0	0	0	0	0	0
W	1	0	0	0	0	0	0	0	SCN8
POR		0	0	0	0	0	0	0	0

This command is to set Gate Start Position for determining the starting gate of display RAM by selecting a value from 0 to 295. Figure 8-2 shows an example using this command of this command when MUX ratio= 295 and MUX ratio= 148. “ROW” means the graphic display data RAM row.

Figure 8-2: Example of Set Display Start Line with no Remapping

	MUX ratio (01h) = 127h	MUX ratio (01h) = 093h	MUX ratio (01h) = 095h
GATE Pin	Gate Start Position (0Fh) = 000h	Gate Start Position (0Fh) = 000h	Gate Start Position (0Fh) = 04Ah
G0	ROW0	ROW0	-
G1	ROW1	ROW1	-
G2	ROW2	ROW2	-
G3	ROW3	ROW3	-
:	:	:	:
:	:	:	:
G72	:	:	-
G73	:	:	-
G74	:	:	ROW74
G75	:	:	ROW75
:	:	:	:
:	:	:	:
G146	ROW146	ROW146	:
G147	ROW147	ROW147	:
G148	ROW148	-	:
G149	ROW149	-	:
:	:	:	:
	:	:	:
G220	:	:	:
G221	:	:	:
G222	:	:	ROW222
G223	:	:	ROW223
	:	:	:
:	:	:	:
G292	ROW292	-	-
G293	ROW293	-	-
G294	ROW294	-	-
G295	ROW295	-	-
Display Example			

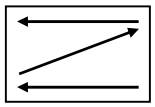
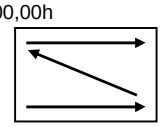
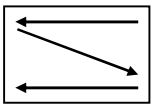
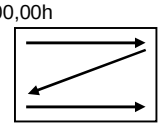
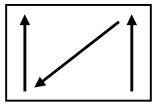
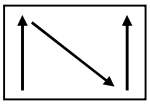
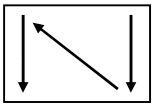
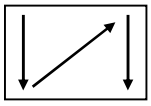
8.3 Data Entry Mode Setting (11h)

This command has multiple configurations and each bit setting is described as follows:

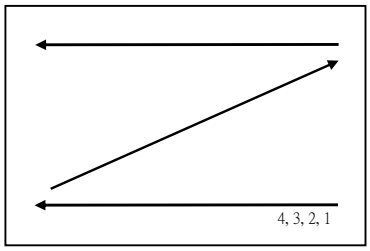
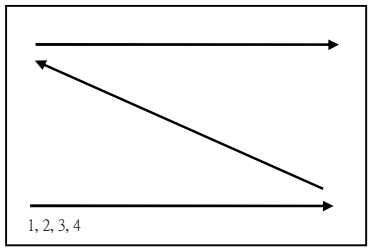
R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1						AM	ID1	ID0
POR		0	0	0	0	0	0	1	1

ID[1:0]: The address counter is automatically incremented by 1, after data is written to the RAM when ID[1:0] = “01”. The address counter is automatically decremented by 1, after data is written to the RAM when ID[1:0] = “00”. The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. The direction of the address when data is written to the RAM is set by AM bits.

AM: Set the direction in which the address counter is updated automatically after data are written to the RAM. When AM = “0”, the address counter is updated in the X direction. When AM = “1”, the address counter is updated in the Y direction. When window addresses are selected, data are written to the RAM area specified by the window addresses in the manner specified with ID[1:0] and AM bits.

	ID [1:0]="00” X: decrement Y: decrement	ID [1:0]="01” X: increment Y: decrement	ID [1:0]="10” X: decrement Y: increment	ID [1:0]="11” X: increment Y: increment
AM="0” X-mode	00,00h  15,127h	00,00h  15, 127h	00,00h  15, 127h	00,00h  15, 127h
AM="1” Y-mode	00,00h  15, 127h	00,00h  15, 127h	00,00h  15, 127h	00,00h  15, 127h

The pixel sequence is defined by the ID [0],

	ID[1:0]="00” X: decrement Y: decrement	ID[1:0]="01” X: increment Y: decrement
AM="0” X-mode	00,00h  4, 3, 2, 1 15,127h	00,00h  1, 2, 3, 4 15,127h

8.4 Set RAM X - Address Start / End Position (44h)

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1				XSA4	XSA3	XSA2	XSA1	XSA0
POR		0	0	0	0	0	0	0	0
W	1				XEA4	XEA3	XEA2	XEA1	XEA0
POR		0	0	0	1	0	1	0	1

XSA[4:0]/XEA[4:0]: Specify the start/end positions of the window address in the X direction by 8 times address unit. Data is written to the RAM within the area determined by the addresses specified by XSA [4:0] and XEA [4:0]. These addresses must be set before the RAM write.
It allows on XEA [4:0] ≤ XSA [4:0]. The settings follow the condition on 00h ≤ XSA [4:0], XEA [4:0] ≤ 15h. The windows is followed by the control setting of Data Entry Setting (R11h)

8.5 Set RAM Y - Address Start / End Position (45h)

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	YSA7	YSA6	YSA5	YSA4	YSA3	YSA2	YSA1	YSA0
POR		0	0	0	0	0	0	0	0
W	1	0	0	0	0	0	0	0	YSA8
POR		0	0	0	0	0	0	0	0
W	1	YEA7	YEA6	YEA5	YEA4	YEA3	YEA2	YEA1	YEA0
POR		0	0	1	0	0	1	1	1
W	1	0	0	0	0	0	0	0	YEA8
POR		0	0	0	0	0	0	0	1

YSA[8:0]/YEA[8:0]: Specify the start/end positions of the window address in the Y direction by an address unit. Data is written to the RAM within the area determined by the addresses specified by YSA [8:0] and YEA [8:0]. These addresses must be set before the RAM write.
It allows YEA [8:0] ≤ YSA [8:0]. The settings follow the condition on 00h ≤ YSA [8:0], YEA [8:0] ≤ 127h. The windows is followed by the control setting of Data Entry Setting (R11h)

8.6 Set RAM Address Counter (4Eh-4Fh)

Reg#	R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
4Eh	W	1				XAD4	XAD3	XAD2	XAD1	XAD0
	POR		0	0	0	0	0	0	0	0
4Fh	W	1	YAD7	YAD6	YAD5	YAD4	YAD3	YAD2	YAD1	YAD0
	POR		0	0	0	0	0	0	0	0
	W	1								YAD8
	POR									0

XAD[4:0]: Make initial settings for the RAM X address in the address counter (AC).
YAD[8:0]: Make initial settings for the RAM Y address in the address counter (AC).

After RAM data is written, the address counter is automatically updated according to the settings with AM, ID bits and setting for a new RAM address is not required in the address counter. Therefore, data is written consecutively without setting an address. The address counter is not automatically updated when data is read out from the RAM. RAM address setting cannot be made during the standby mode. The address setting should be made within the area designated with window addresses which is controlled by the Data Entry Setting (R11h) {AM, ID[1:0]} ; RAM Address XStart / XEnd Position (R44h) and RAM Address Ystart /Yend Position (R45h). Otherwise undesirable image will be displayed on the Panel.

9 Operation Flow and Code Sequence

9.1 General operation flow to drive display panel

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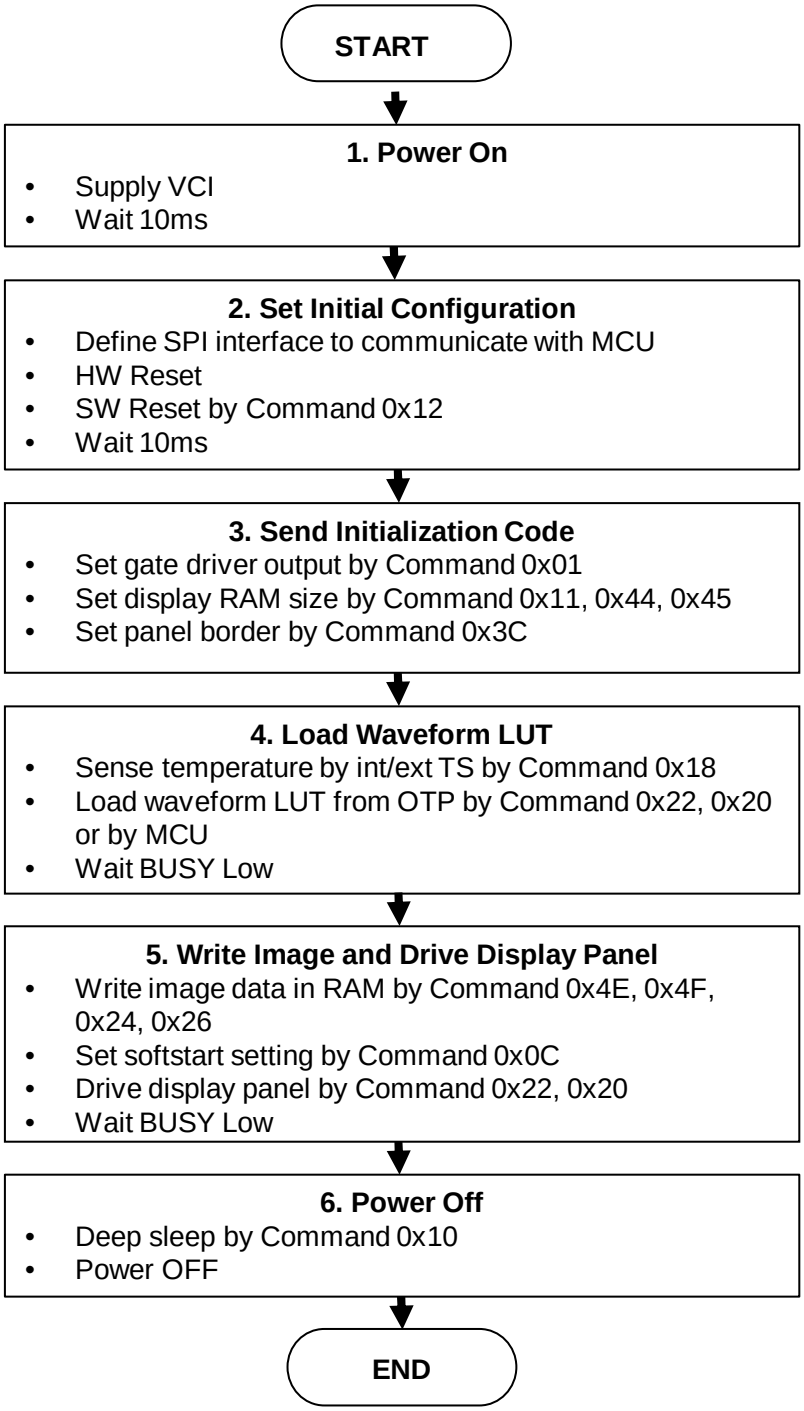


Figure 9-1: Operation flow to drive display panel

10 Absolute Maximum Rating

Table 10-1 : Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CI}	Logic supply voltage	-0.5 to +6.0	V
V_{IN}	Logic Input voltage	-0.5 to V_{DDIO}+0.5	V
V_{OUT}	Logic Output voltage	-0.5 to V_{DDIO}+0.5	V
T_{OPR}	Operation temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-65 to +150	°C

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{CI} be constrained to the range $V_{SS} < V_{CI}$. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DDIO}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

11 Electrical Characteristics

The following specifications apply for: VSS=0V, VCI=3.0V, VDD=1.8V, T_{OPR}=25ºC.

Table 11-1: DC Characteristics

Symbol	Parameter	Applicable pin	Test Condition	Min.	Typ.	Max.	Unit
V_{CI}	VCI operation voltage	VCI		2.2	3.0	3.7	V
V_{DD}	VDD operation voltage	VDD		1.7	1.8	1.9	V
V_{COM_DC}	VCOM_DC output voltage	VCOM		-3.0		-0.2	V
dV_{COM_DC}	VCOM_DC output voltage deviation	VCOM		-200		200	mV
V_{COM_AC}	VCOM_AC output voltage	VCOM		V_{SL} + V_{COM_DC}	V_{COM_DC}	V_{SH1}+ V_{COM_DC}	V
V_{GATE}	Gate output voltage	G0~G295		-20		+20	V
$V_{GATE(p-p)}$	Gate output peak to peak voltage	G0~G295				40	V
V_{SH1}	Positive Source output voltage	VSH1		+2.4	+15	+17	V
dV_{SH1}	VSH1 output voltage deviation	VSH1	From 2.4V to 8.8V	-100		100	mV
			From 9.0V to 17V	-200		200	mV
V_{SH2}	Positive Source output voltage	VSH2		+2.4	+5	+17	V
dV_{SH2}	VSH2 output voltage deviation	VSH2	From 2.4V to 8.8V	-100		100	mV
			From 9.0V to 17V	-200		200	mV
V_{SL}	Negative Source output voltage	VSL		-17	-15	-9	V
dV_{SL}	VSL output voltage deviation	VSL		-200		200	mV
V_{IH}	High level input voltage	SDA, SCL, CS#, D/C#, RES#, BS1, M/S#, CL		0.8V_{DDIO}			V
V_{IL}	Low level input voltage					0.2V_{DDIO}	V
V_{OH}	High level output voltage	SDA, BUSY, CL	IOH = -100uA	0.9V_{DDIO}			V
V_{OL}	Low level output voltage		IOL = 100uA			0.1V_{DDIO}	V
V_{PP}	OTP Program voltage	VPP		7.25	7.5	7.75	V

Symbol	Parameter	Applicable pin	Test Condition	Min.	Typ.	Max.	Unit
Islp_VCI	Sleep mode current	VCI	- DC/DC off - No clock - No output load - MCU interface access - RAM data access		20	35	uA
Idslp_VCI1	Current of deep sleep mode 1	VCI	- DC/DC off - No clock - No output load - No MCU interface access - Retain RAM data but cannot access the RAM		1	3	uA
Idslp_VCI2	Current of deep sleep mode 2	VCI	- DC/DC off - No clock - No output load - No MCU interface access - Cannot retain RAM data		0.7	3	uA
Iopr_VCI	Operating Mode current	VCI	VCI=3.0V		1000		uA
V_{GH}	Operating Mode Output Voltage	VGH	Enable Clock and Analog by Master Activation Command VGH=20V VGL=-VGH VSH1=15V VSH2=5V VSL=-15V VCOM = -2V No waveform transitions. No loading. No RAM read/write No OTP read /write	19.5	20	20.5	V
V_{SH1}		VSH1		14.8	15	15.2	V
V_{SH2}		VSH2		4.9	5	5.1	V
V_{SL}		VSL		-15.2	-15	-14.8	V
V_{COM}		VCOM		-2.2	-2	-1.8	V

Table 11-2: Regulators Characteristics

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
IVSH	VSH1 current	VSH1 = +15V	VSH1			800	uA
IVSH1	VSH2 current	VSH2 = +5V	VSH2			800	uA
IVSL	VSL current	VSL = -15V	VSL			800	uA
IVCOM	VCOM current	VCOM = -2V	VCOM			100	uA

12 AC Characteristics

12.1 Serial Peripheral Interface

The following specifications apply for: VDDIO - VSS = 2.2V to 3.7V, T_{OPR} = 25°C, CL=20pF

Table 12-1 : Serial Peripheral Interface Timing Characteristics

Write mode

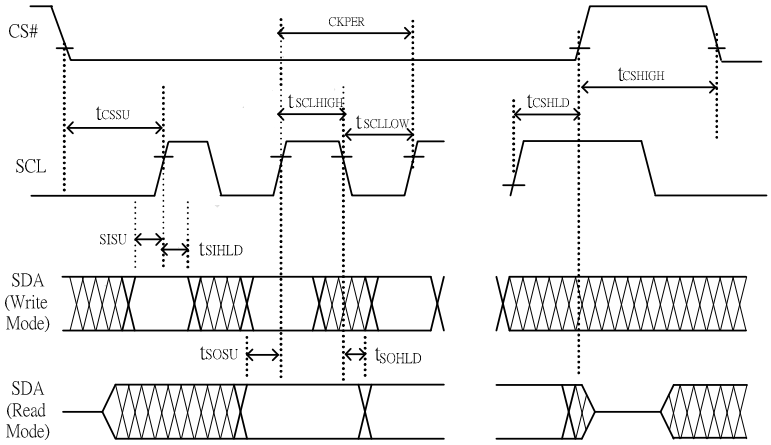
Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL frequency (Write Mode)			20	MHz
t_{CSSU}	Time CS# has to be low before the first rising edge of SCLK	60			ns
t_{CSHLD}	Time CS# has to remain low after the last falling edge of SCLK	65			ns
t_{CSHIGH}	Time CS# has to remain high between two transfers	100			ns
$t_{SCLHIGH}$	Part of the clock period where SCL has to remain high	25			ns
t_{SCLLOW}	Part of the clock period where SCL has to remain low	25			ns
t_{SISU}	Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL	10			ns
t_{SIHLD}	Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL	40			ns

Read mode

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL frequency (Read Mode)			2.5	MHz
t_{CSSU}	Time CS# has to be low before the first rising edge of SCLK	100			ns
t_{CSHLD}	Time CS# has to remain low after the last falling edge of SCLK	50			ns
t_{CSHIGH}	Time CS# has to remain high between two transfers	250			ns
$t_{SCLHIGH}$	Part of the clock period where SCL has to remain high	180			ns
t_{SCLLOW}	Part of the clock period where SCL has to remain low	180			ns
t_{SOSU}	Time SO(SDA Read Mode) will be stable before the next rising edge of SCL		50		ns
t_{SOHLD}	Time SO (SDA Read Mode) will remain stable after the falling edge of SCL		0		ns

Note: All timings are based on 20% to 80% of VDDIO-VSS

Figure 12-1: SPI timing diagram



13 Application Circuit

Figure 13-1: Schematic of SSD1680 application circuit

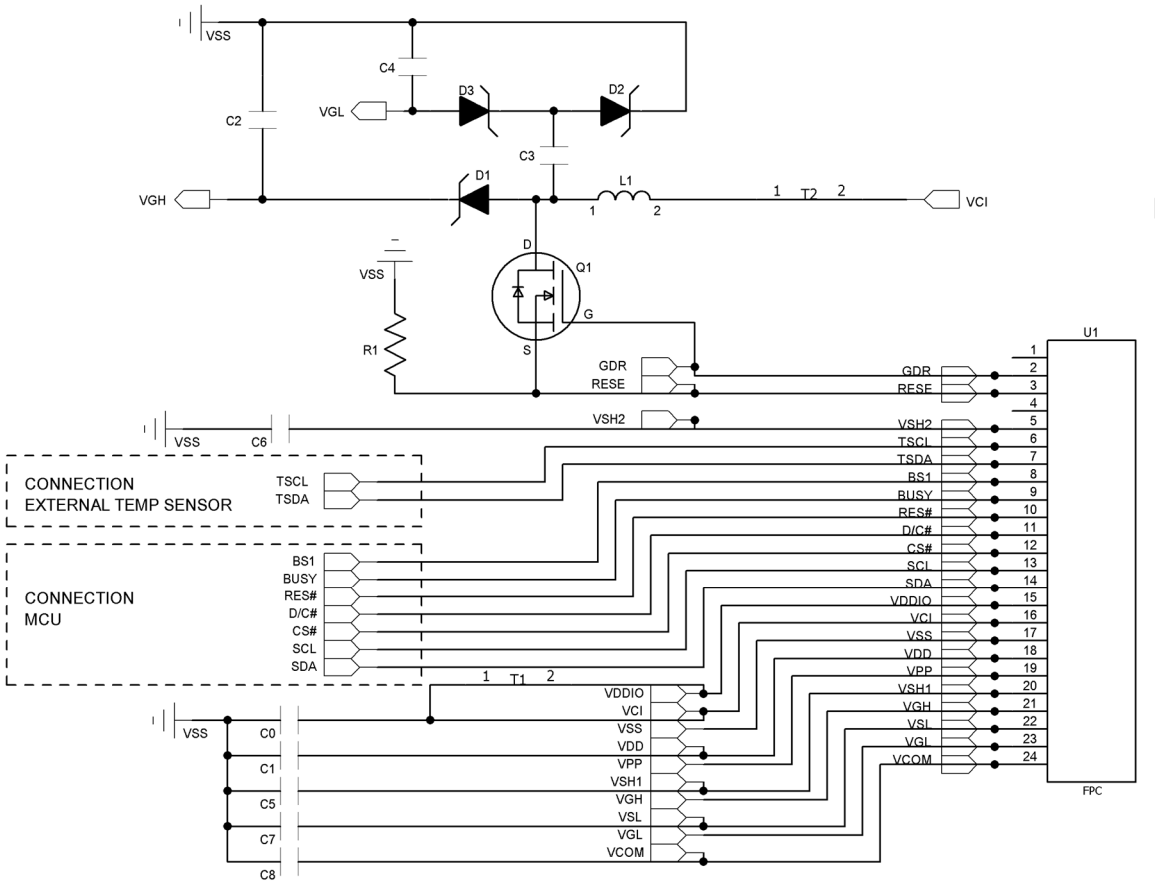


Table 13-1: Component list for SSD1680 application circuit

Part Name	Value	Requirements/Reference Part
C0-C1	1uF	X5R/X7R; Voltage Rating : 6V or 25V
C2-C7	1uF	0402/0603/0805; X5R/X7R; Voltage Rating : 25V
C8	0.47uF, 1uF	0603/0805; X7R; Voltage Rating : 25V Note: Effective capacitance > 0.25uF @ 18V DC bias
R1	2.2 ohm	0402, 0603, 0805; 1% variation, ≥ 0.05W
D1-D3	Diode	MBR0530 1) Reverse DC voltage ≥ 30V 2) Io ≥ 500mA 3) Forward voltage ≤ 430mV
Q1	NMOS	Si1304BDL/NX3008NBK 1) Drain-Source breakdown voltage ≥ 30V 2) Vgs(th) = 0.9V (Typ), 1.3V (Max) 3) Rds on ≤ 2.1Ω @ Vgs = 2.5V
L1	47uH	CDRH2D18 / LDNP-470NC Io= 500mA (Max)
U1	0.5mm ZIF socket	24pins, 0.5mm pitch

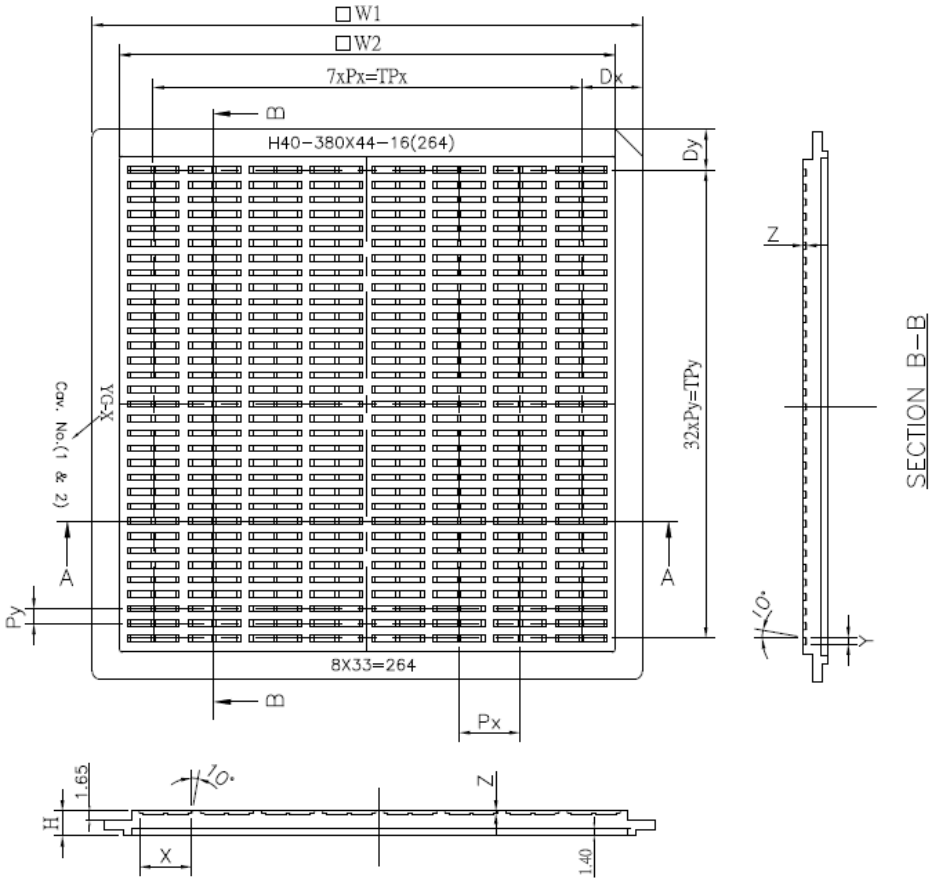
Remarks:

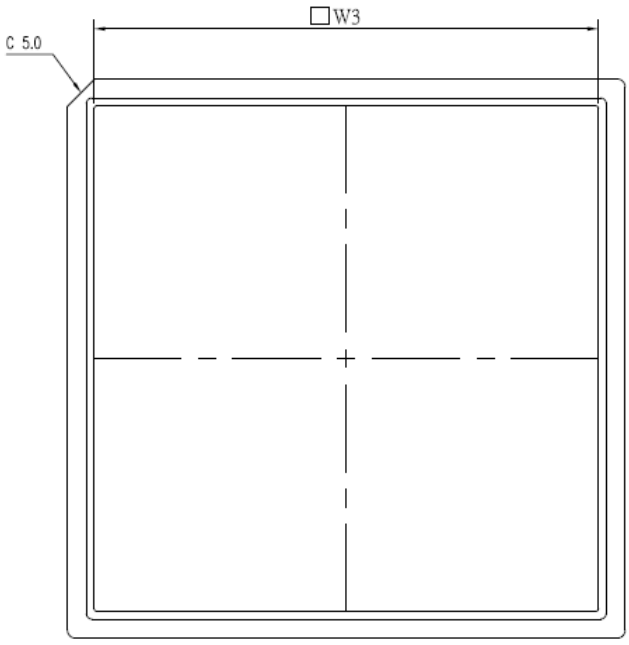
1) The recommended component value and reference part in Table 13-1 is subject to change depending on panel loading.
2) Customer is required to review if the selected component value and part is suitable for their application.

14 Package Information

14.1 Die Tray Dimensions for SSD1680Z

Figure 14-1 : SSD1680Z die tray information (unit: mm)

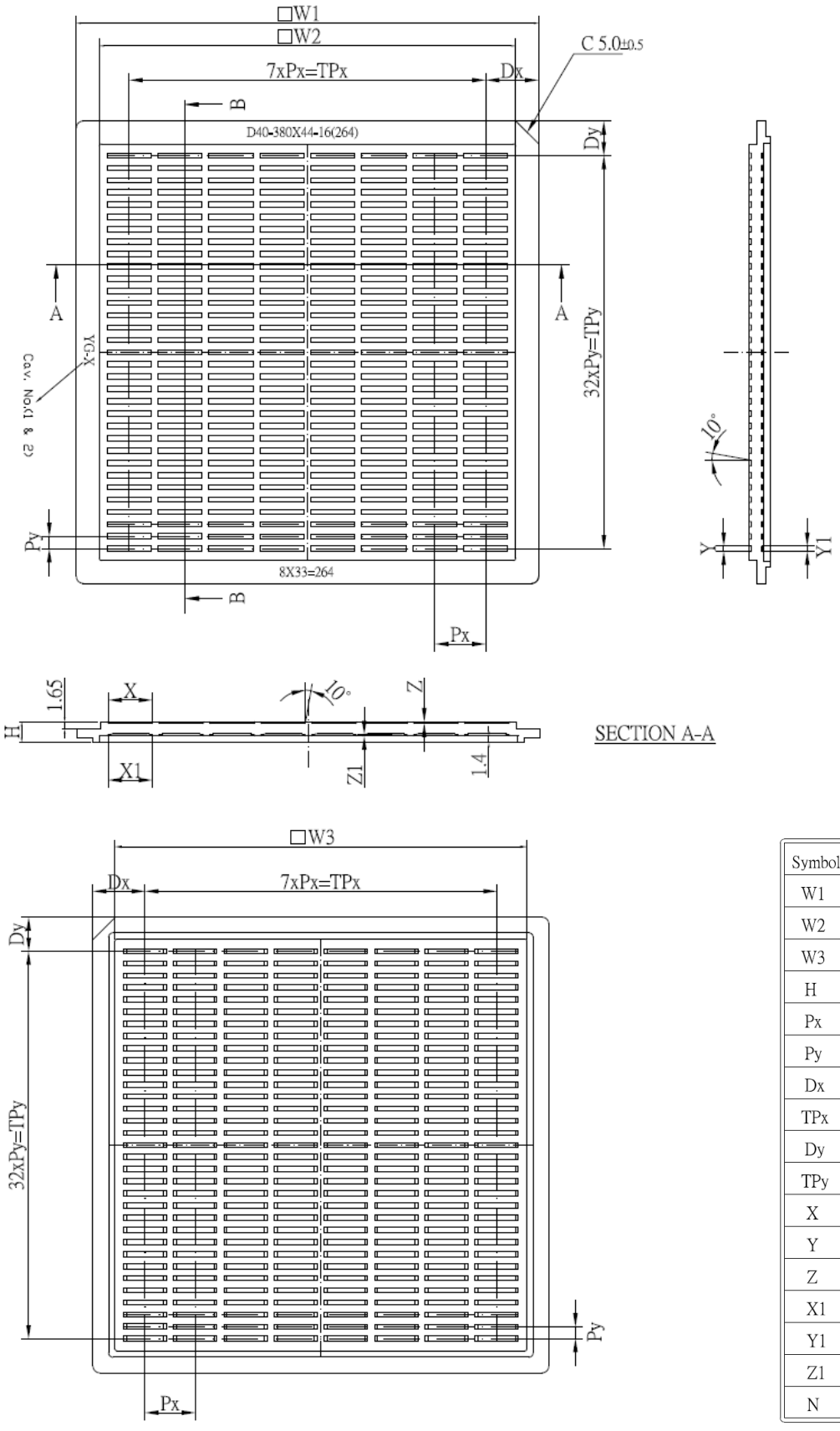




Symbol	Spec(mm)
W1	101.60±0.10
W2	91.55±0.10
W3	91.85±0.10
H	4.55±0.10
Dx	11.25±0.10
TPx	79.10±0.10
Dy	7.60±0.10
TPy	86.40±0.10
Px	11.30±0.05
Py	2.70±0.05
X	9.661±0.05
Y	1.125±0.05
Z	0.40±0.05
N	264(pocket number)

14.2 Die Tray Dimensions for SSD1680Z8

Figure 14-2 : SSD1680Z8 die tray information (unit: mm)



Symbol	Spec (mm)
W1	101.60±0.10
W2	91.55±0.10
W3	91.75±0.10
H	4.55±0.10
Px	11.20±0.05
Py	2.70±0.05
Dx	11.60±0.05
TPx	78.40±0.10
Dy	7.60±0.05
TPy	86.40±0.10
X	9.661±0.05
Y	1.125±0.05
Z	0.40±0.05
X1	9.661±0.05
Y1	1.125±0.05
Z1	0.35±0.05
N	8x33=264 (pocket number)

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