HIGH-VOLTAGE MIXED-SIGNAL IC

UC8159

All-in-one driver IC w/ Timing Controller for
Color Application

Preliminary Specifications
Datasheet Revision: 0.1

IC Version: c_A
July 21, 2014

ULTRACHIP

The Coolest EPD Driver, Ever!

Table of Content

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INTRODUCTION

The UC8159 is an all-in-one gate source driver with an integrated timing controller for ESL application. The source is capable of 3-bit outputs per pixel to support white/black/color. The timing controller provides control signals for the source driver and gate drivers.

The integrated DC-DC converter generates all the necessary source and gate output voltages for VDPS_LV/VDNS_LV (+/-3V~+/- 15V), VDPS/VDNS(+/- 15V) and VDPG/VDNG (+/- 17V ~ +/- 20V). The chip also includes an output buffer for the supply of the common electrode (VCOMAC or VCOMDC). The system is configurable through a 3-wire/4-wire (SPI) serial.

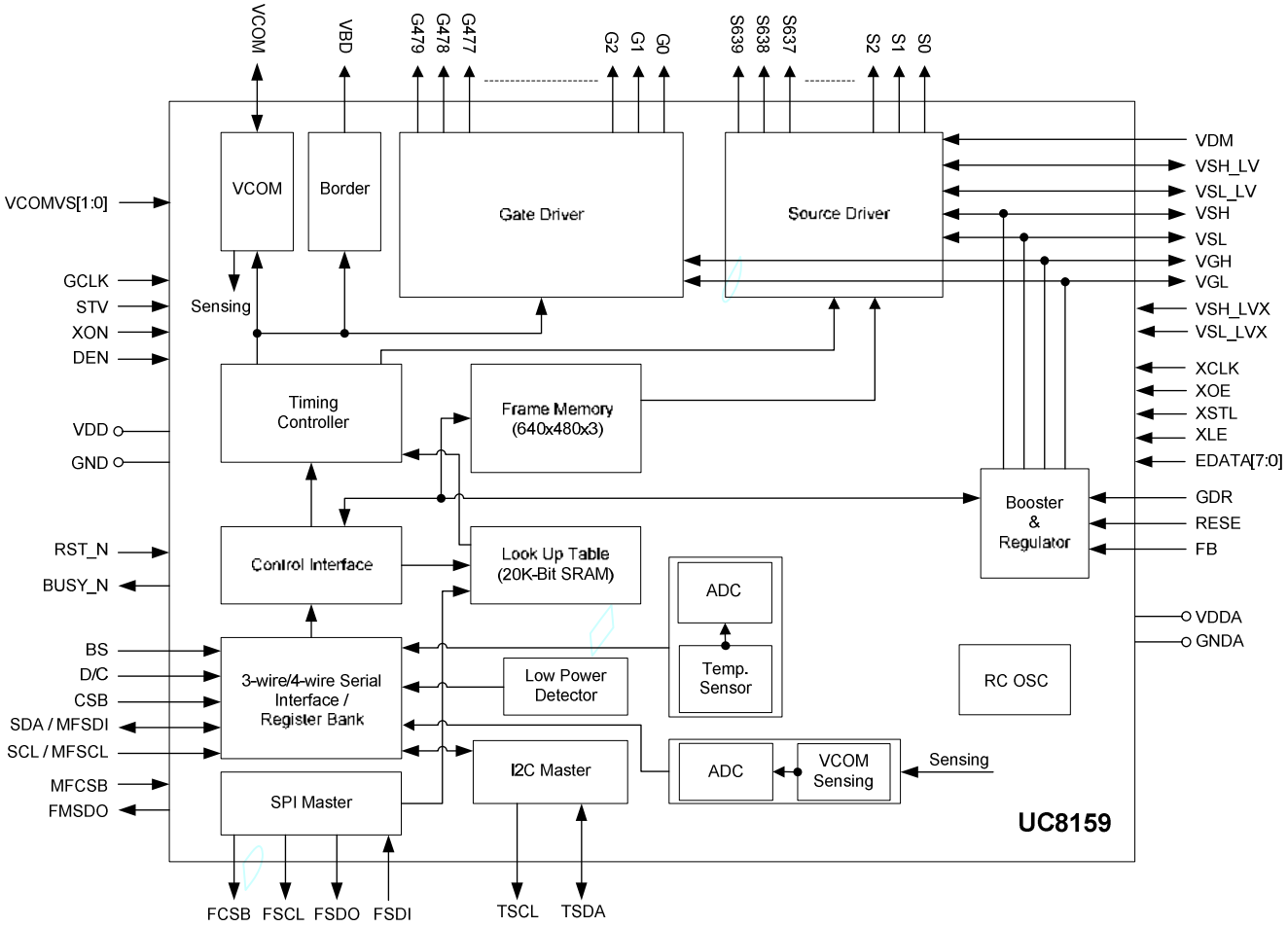
MAIN APPLICATIONS

- E-tag application

FEATURE HIGHLIGHTS

- System-on-chip (SOC) for ESL, including:
- Timing controller support of several resolutions
- Preselect res (640x480, 600x450, 640x448, 600x448)
- Built in Frame memory maximum (640x480x3bit)
- Support LUT
- 640 outputs source driver with 3-bit white/black/red resolution
  - Output dynamic range: VDNS, 0, VDPS, VDNS_LV, VDPS_LV
  - Output deviation: 0.2V
  - 640 channels outputs
  - Left and Right shift capability
- 480 outputs gate driver:
  - 480 channels outputs
  - Up and Down shift capability
  - Output voltage VDNG+40
- 3-wire/4-wire (SPI) serial interface for system configuration
- DC-DC controller for generating the analog power supply
- Common electrode (VCOM AC) level
- External SPI flash/eeprom
- Built-in temperature sensor
- Support I^2C interface for external temperature sensor
- Support low power detection
- Digital supply voltage: 2.3~ 3.6V
- Support frame rate: 200 Hz (max)
- Support pure source & gate driver function
- COG Package

BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	I^2C	Description
UC8159cGAA-M0P3-3	No	with 3” Tray
UC8159cGAA-M0P3-4	No	with 4” Tray

General Notes

APPLICATION INFORMATION

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

BARE DIE DISCLAIMER

All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing. There is no post waffle saw/pack testing performed on individual die. Although the latest modern processes are utilized for wafer sawing and die pick-&-place into waffle pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and qualify their application in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

LIFE SUPPORT APPLICATIONS

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

CONTENT DISCLAIMER

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PIN DESCRIPTION

Type: C: Capacitor pin, I: Input, I/O: Input/Output, M: Mark, O: Output,
PWR: Power, PI: Power Input, PO: Power Output, PS: Power Setting, S: Shorted line

Pin (Pad) Name	Pin Count	Type	Description
SERIAL INTERFACE			
CSB	1	I, Type2	Serial communication chip select.
SDA / MFSDI*	1	I/O, Type5	Serial communication data input. It would bypass to MFSDI by R61H command.
SCL / MFSCL*	1	I, Type2	Serial communication clock input. It would bypass to MFSCL by R61H command.
D/C	1	I, Type2	Serial communication command/parameter input. L: command H: parameter
FMSDO*	1	O, Type1	Serial communication data output. It would bypass to FMSDO by R61H command.
MFCSB*	1	I, Type2	Serial communication chip select. It would bypass to MFCSB by R61H command.
FCSB	1	O, Type1	Serial communication chip select for External Flash/EEPROM.
FSCL	1	O, Type1	Serial communication clock input for External Flash/EEPROM.
FSDI	1	I, Type2	Serial communication clock input for External Flash/EEPROM.
FSDO	1	O, Type1	Serial communication clock output for External Flash/EEPROM.
CONTROL INTERFACE			
BS	1	I, Type2	Input interface setting. Select 3 wire/ 4 wire SPI interface L: 4-wire IF **H: 3-wire IF (Default)**
RST_N	1	I (Pull-up), Type3	Global reset pin. Low reset. When RST_N become low, driver will reset. All register will reset to default value. All driver functions will be disabled. SD output and VCOM will remain previous condition. It may have two conditions: 0v or floating.
BUSY_N	1	O, Type1	This pin indicates the driver status. L: Driver is busy, data/VCOM is transforming. H: non-busy. Host side can send command/data to driver.
TSCL	2	O	I^2C clock for external temperature sensor.
TSDA	2	I/O	I^2C data for external temperature sensor.

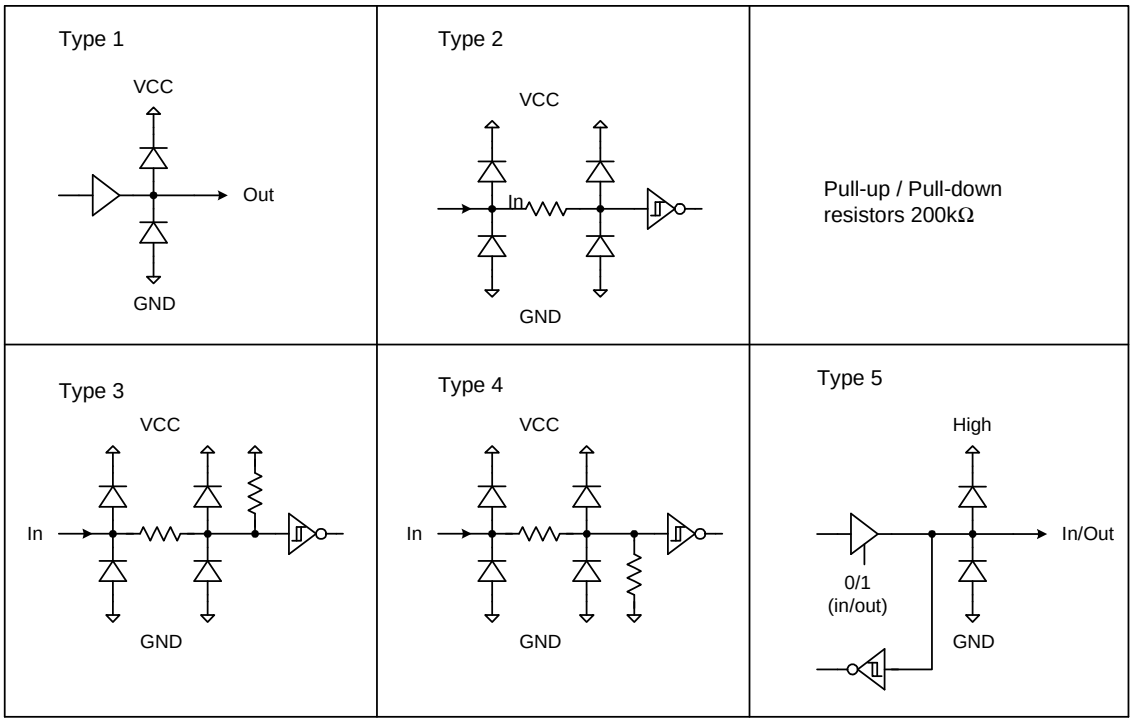
Pin (Pad) Name	Pin Count	Type	Description
SOURCE / GATE DRIVER			
S[0..639]	640	O	Source driver output signals.
G[0..479]	480	O	Gate driver output signals.
VBD	2	O	Border output pin. It will output black
VCOM	16	O	VCOM output. VCOM has four voltage states: 1. (VDPS+VCM_DC) V 2. (VCM_DC) V 3. (VDNS+VCM_DC) V 4. Floating
POWER CIRCUIT			
GDR	6	O	This pin is N-MOS gate control.
RESE	2	PWR	Current sense input for control loop.
FB	2	PWR	Keep open
VGH	20	C	Positive gate voltage
VGL	23	C	Negative gate voltage.
VSH	10	C	Positive source voltage
VSL	10	C	Negative source voltage.
VSH_LV	10	C	Positive source voltage
VSL_LV	10	C	Negative source voltage.
DRIVER INTERFACE			
DEN	1	I	Pure driver mode pin. L: Disable pure driver mode. H: Enable pure driver mode.
XCLK	1	I	Source driver clock input. Data inputs are captured on the rising edge of clock signal.
XOE	1	I	Source driver outputs enabled when OE is logic “H”, Outputs forced to GND when OE is logic “L”. It is asynchronous to clock CLK.
XSTL	1	I	Source driver data shift start pulse
XLE	1	I	Source driver parallel latch enable, transparent when high. It is asynchronous to clock CLK
EDATA[7:0]	8	I	Source driver 8-bit data
GCLK	1	I	Gate driver shift clock pin. The shift register data are shifted synchronously with each rising edge of GCLK.
STV	1	I	Gate driver start pulse
XON	1	I	Driver XON pin

Pin (Pad) Name	Pin Count	Type	Description
POWER SUPPLY			
VDD		PWR	Digital voltage supply
VSS		PWR	Digital ground.
AVDD		PWR	Analog voltage supply
AVSS		PWR	Analog ground.
COMA		S	Internal link together.

Remark:

(1) Pull-up / Pull-down resistors 200KΩ

(2) I/O Pin Structure:



COMMAND TABLE

W/R: 0: Write Cycle 1: Read Cycle C/D: 0: Command / 1: Data D7~D0: –: Don't Care #: Valid Data

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
1	Panel Setting (PSR)	0	0	0	0	0	0	0	0	0	0		00h
		0	1	#	#	#	--	#	#	#	#	RES[1], RES[0], LUT_EN, UD, SHL, SHD_N, RST_N	07h
2	Power Setting (PWR)	0	0	0	0	0	0	0	0	0	1		01h
		0	1	--	--	--	--	#	#	#	#	EDATA_SEL, EDATA_SET, VGate_EN, VSource_EN	0Fh
		0	1	--	--	--	--	--	#	#	#	VGHL_LV[1:0]	01h
		0	1	--	--	#	#	#	#	#	#	VDPS_LV[5:0]	07h
		0	1	--	--	#	#	#	#	#	#	VDNS_LV[5:0]	07h
3	Power OFF (POF)	0	0	0	0	0	0	0	0	1	0		02h
4	Power OFF Sequence Setting (PFS)	0	0	0	0	0	0	0	0	1	1		03h
		0	1	--	--	#	#	--	--	--	--	T_VDS_OFF[1:0]	00h
5	Power ON (PON)	0	0	0	0	0	0	0	1	0	0		04h
6	Data Start Transmission 1 (DTM1) (x-byte command)	0	0	0	0	0	1	0	0	0	0		10h
		0	1	#	#	#	--	#	#	#	--	KPixel1[2:0], KPixel2[2:0]	00h
		0	1	:	:	:	:	:	:	:	:	:	:
		0	1	#	#	#	--	#	#	#	--	Kpixel[2M-1][2:0], Kpixel[2M][2:0]	00h
7	Data Stop (DSP)	0	0	0	0	0	1	0	0	0	1		11h
		1	1	#	--	--	--	--	--	--	--	Data_flag	--
8	Display Refresh (DRF)	0	0	0	0	0	1	0	0	1	0		12h
9	PLL control (PLL)	0	0	0	0	1	1	0	0	0	0		30h
		0	1	--	--	#	#	#	#	#	#	M[2:0], N[2:0]	3Ch
10	Temperature Sensor Command (TSC)	0	0	0	1	0	0	0	0	0	0		40h
		1	1	#	#	#	#	#	#	#	#	D[10:3] / TS[7:0]	00h
		1	1	#	#	#	--	--	--	--	--	D[2:0] / -	00h
11	Temperature Sensor Calibration (TSE)	0	0	0	1	0	0	0	0	0	1		41h
		0	1	#	--	--	#	#	#	#	#	TSE,TO[4:0]	00h
12	Vcom and data interval setting (CDI)	0	0	0	1	0	1	0	0	0	0		50h
		0	1	#	#	#	#	#	#	#	#	VBD[2:0], DDX, CDI[3:0]	17h
13	Lower Power Detection (LPD)	0	0	0	1	0	1	0	0	0	1		51h
		1	1	--	--	--	--	--	--	--	#	LPD	01h
14	TCON setting (TCON)	0	0	0	1	1	0	0	0	0	0		60h
		0	1	#	#	#	#	#	#	#	#	S2G[3:0], G2S[3:0]	22h
15	TCON resolution (TRES)	0	0	0	1	1	0	0	0	0	1		61h
		0	1	--	--	--	--	--	#	#	#	HRES[9:0]	00h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	--	--	--	--	--	#	#	#	VRES[9:0]	00h
		0	1	#	#	#	#	#	#	#	#		00h
16	SPI flash control (DAM)	0	0	0	1	1	0	0	1	0	1		65h
		0	1	--	--	--	--	--	--	--	#	DAM	00h
17	Revision (REV)	0	0	0	1	1	1	0	0	0	0		70h
		0	1	--	--	#	#	#	#	#	#	MAN, SHRK, LUT_REV[3:0]	00h
18	Get Status (FLG)	0	0	0	1	1	1	0	0	0	1		71h
		1	1	--	--	#	#	#	#	#	#	I^2C_ERR, I^2C_BUSYN, DATA_FLAG, PON, POF, BUSY_N	--
19	Auto Measurement Vcom (AMV)	0	0	1	0	0	0	0	0	0	0		80h

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
		0	1	--	#	#	#	#	#	#	#	VCM_EN, AMVT[1:0], AMVX, AMVS, AMV, AMVE	50h
20	Read Vcom Value(VV)	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**		**81h**
		1	1	--	#	#	#	#	#	#	#	VV[6:0]	00h
21	VCM_DC Setting (VDCS)	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**1**	**0**		**82h**
		0	1	--	#	#	#	#	#	#	#	VDCS[6:0]	0Ch

Note: (1) All other register addresses are invalid or reserved by UltraChip, and should NOT be used.

(2) Any bits shown here as 0 must be written with a 0. All unused bits should also be set to zero. Device malfunction may occur if this is not done.

(3) Commands are processed on the 'stop' condition of the interface.

(4) Registers marked 'W/R' can be read, but the contents are written when the SPI command completes – so the contents can be read and altered. The user can subsequently write the register to restore the contents following an SPI read.

(5) All commands are "USABLE" either when BUSY_N=0 or 1, except DSP (R11h) and DRF (R12h), which are only "USABLE" either when BUSY_N=1, ("USELESS" when BUSY_N=0).

* USABLE means that Host can send command/parameter to driver.
* USELESS means that Host cannot send command/parameter to driver.

COMMAND DESCRIPTION

W/R: 0: Write Cycle / 1: Read Cycle C/D: 0: Command / 1: Data D7-D0: –: Don't Care

(1) PANEL SETTING (PSR) (R00H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Setting the panel	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	00h
	0	1	RES1	RES0	LUT_EN	**-**	UD	SHL	SHD_N	RST_N	07h

RES[1:0]: Display Resolution setting (source x gate)
00b: 640x480 (Default)
01b: 600x450
10b: 640x448
11b: 600x448

LUT_EN: LUT selection
0: Using LUT from external Flash.
1: Using LUT from register.

UD: Gate Scan Direction
0: Scan down. First line to Last line: Gn → … … → G1
1: Scan up. (Default) First line to Last line: G1 → … … . → Gn

SHL: Source Shift Direction
0: Shift left. First data to Last data: Sn → … … → S1
1: Shift right. (Default) First data to Last data: S1 → … … . → Sn

SHD_N: Booster Switch
0: DC-DC converter OFF.
1: DC-DC converter ON (Default)
When SHD_N become low, DC-DC will turn OFF. Register and SRAM data will keep until VDD OFF. SD output and VCOM will remain previous condition. It may have two conditions: 0v or floating.

RST_N: Soft Reset
0: The controller is reset. Reset all registers to their default value.
1: Noormal operation (Default). Booster OFF, Register data are set to their default values, and SEG/BG/VCOM: 0V
When RST_N become low, driver will reset. All register will reset to default value. Driver all function will disable. SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.

(2) POWER SETTING (PWR) (R01H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Selecting Internal/External Power	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	01h
	0	1	-	-	-	-	EDATA_SEL	EDATA_SET	VGate_EN	VSource_EN	0Fh
	0	1	-	-	-	-	-	-	VGHL_LVL[1:0]		01h
	0	1	-	-	VDPS_LV[5:0]						07h
	0	1	-	-	VDNS_LV[5:0]						07h

EDATA_SEL: EDATA selection for pure driver mode
0 : When EDATA_SET=1, pixel bit =2`b11 output VDPS_L level
1 : When EDATA_SET=1, pixel bit =2`b11 output VDNS_L level (default)

EDATA_SET: EDATA setting for pure driver mode
0 : 3-bit data mode for pure driver
1 : 2-bit data mode for pure driver (default)

VGate_EN: VGate power selection.
0 : External gate power from VDPG and VDNG pin.
1 : Internal DCDC function for generate gate power. (default)

VSource_EN: VSource power selection.
0 : External source power from VDPS and VDNS pin.
1 : Internal DCDC function for generate source power. (default)

VGHL_LVL[1:0]: VGH / VGL Voltage Level selection.

VDPS_LV[5:0]: Internal VDHpower selection for B/W LUT.

VDNS_LV[5:0]: Internal VDL power selection for B/W LUT.

(3) POWER OFF (POF) (R02H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Turning OFF the power	0	0	0	0	0	0	0	0	1	0	02h

After power off command, driver will power off based on the Power OFF Sequence, BUSY_N signal will become “0”.

The Power OFF command will turn off DCDC, T-con, source driver, gate driver, VCOM, temperature sensor, but register and SRAM data will keep until VDD off.

SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.

(4) POWER OFF SEQUENCE SETTING (PFS) (R03H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Setting Power OFF sequence	0	0	0	0	0	0	0	0	1	1	03h
	0	1	-	-	T_VDS_OFF[1:0]		-	-	-	-	00h

T_VDS_OFF[1:0]: Power OFF Sequence of VDH and VDL.

00b: 1 frame (Default) 01b: 2 frames 10b: 3 frames 11b: 4 frame

(5) POWER ON (PON) (REGISTER: R04H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Turning ON the power	0	0	0	0	0	0	0	1	0	0	04h

After the Power ON command, driver will power on based on the Power ON Sequence.

After power on command and all power sequence are ready, then BUSY_N signal will become “1”.

(6) DATA START TRANSMISSION 1 (DTM1) (R10H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	0	0	0	1	0	0	0	0	10h
	0	1	KPixel12	KPixel11	KPixel10	Dummy	KPixel22	Kpixel21	Kpixel20	Dummy	00h
	0	1	:	:	:	:	:	:	:	:	00h
	0	1	Kpixel (2M-1)2	Kpixel (2M-1)1	Kpixel (2M-1)0	Dummy	Kpixel (2M)2	Kpixel (2M)1	Kpixel (2M)0	Dummy	00h

This command indicates that user starts to transmit data. Then write to SRAM. While complete data transmission, user must send a DataStop command (R11H). Then the chip will start to send data/VCOM for panel.

Kpixel[1~2M][2:0] :

KPixel[2:0]	Look Up Table
000	LUTB
001	LUTG1
010	LUTG2
011	LUTW
100	LUTR0
101	LUTR1
110	LUTR2
111	LUTR3

(7) DATA STOP (DSP) (R11H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Stopping data transmission	0	0	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**1**	11h
	1	1	data_flag	-	-	-	-	-	-	-	--

To stop data transmission, this command must be issued to check the data_flag.

Data_flag: Data flag of receiving user data.

0: Driver didn't receive all the data.
1: Driver has already received all the one-frame data (DTM1 and DTM2).

After "Data Start" (10h) or "Data Stop" (11h) commands, BUSY_N signal will become "0".

This command only active when BUSY_N = "1".

(8) DISPLAY REFRESH (DRF) (R12H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Refreshing the display	0	0	**0**	**0**	**0**	**1**	**0**	**0**	**1**	**0**	12h

After this command is issued, driver will refresh display (data/VCOM) according to SRAM data and LUT.

After Display Refresh command, BUSY_N signal will become "0".

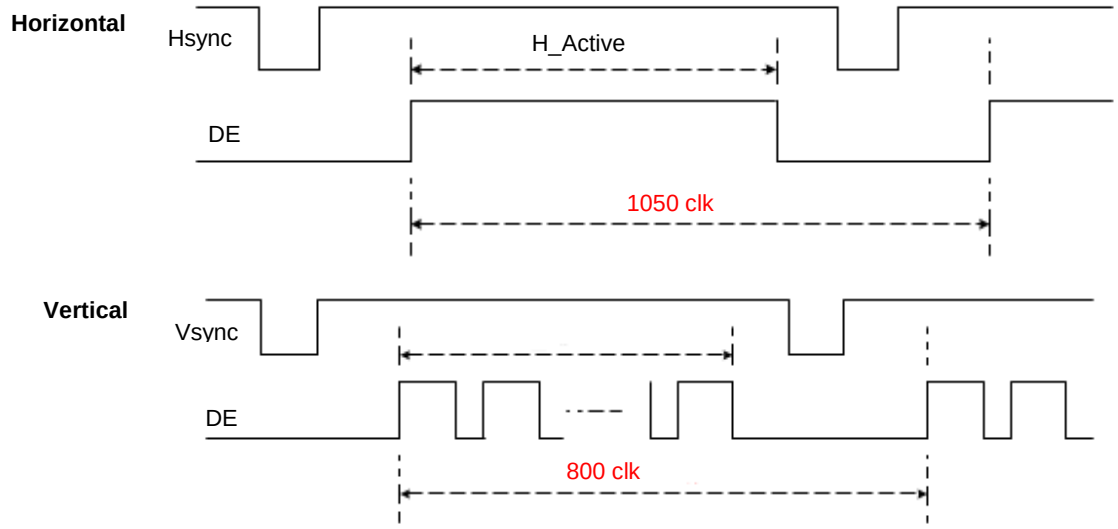
This command only active when BUSY_N = "1".

(19) PLL CONTROL (PLL) (R30H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Controlling PLL	0	0	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**0**	30h
	0	1	-	-	M[2:0]			N[2:0]			3Ch

The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

Frame rate (Hz)	
10	Oscclk = 2MHz PLL clock = Oscclk x (M / N)
20	
30	
40	
50 (Default)	
60	
70	
85	
100	
200	



(20) TEMPERATURE SENSOR CALIBRATION (TSC) (R40H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Sensing Temperature	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	40h
	1	1	D10	D9/TS6	D8/TS5	D7/TS4	D6 / TS3	D5 / TS2	D4 / TS1	D3 / TS0	00h
	1	1	D2	D1	D0	-	-	-	-	-	00h

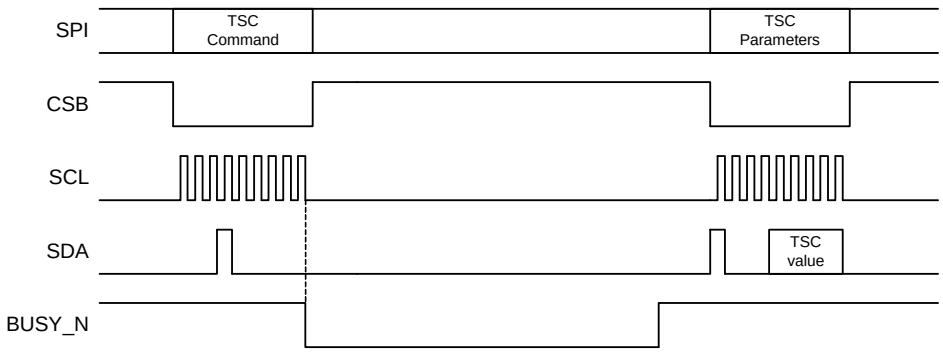
This command reads the temperature sensed by the temperature sensor.

TS[7:0]: When TSE (R41h) is set to 0, this command reads internal temperature sensor value.

D[10:0]: When TSE (R41h) is set to 1, this command reads external LM75 temperature sensor value.

Bit 7~0	Temperature (^{o}C)
0000 0000b	0
0000 0001b	0.5
0000 0010b	1
:	:
0101 1010b	45
:	:
0110 0100b	50
:	:
1100 1110b	-25
:	:
1111 1110b	-1
1111 1111b	-0.5

BUSY_N become low after TSC command. When BUSYN become high, Parameter can be read.



(21) TEMPERATURE SENSOR CALIBRATION (TSE) (R41H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Calibrate Temperature Sensor	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**1**	41h
	0	1	TSE	**-**	**-**	TO[4:0]					00h

This command selects Internal or External temperature sensor.

TSE: Internal temperature sensor switch

0: Enable (default) 1: Disable; using external sensor.

TO[4:0]: Temperature offset.

TO[4]: sign bit 0b: + 1b: -
TO[3:0]: offset value

(22) VCOM AND DATA INTERVAL SETTING (CDI) (R50H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Interval between Vcom and Data	0	0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	50h
	0	1	VBD[2:0]			DDX	CDI[3:0]				17h

This command indicates the interval of Vcom and data output. When setting the vertical back porch, the total blanking will be kept (20 Hsync).

VBD[2:0]: **V**border control, border output selection

VBD	Border output voltage
000 b	Border floating (Default)
001	Border output LUTB voltage
010	Border output LUTG1 voltage
011	Border output LUTG2 voltage
100	Border output LUTW voltage
101	Border output LUTR1 voltage
110	Border output LUTR2 voltage
111	Border output LUTR3 voltage

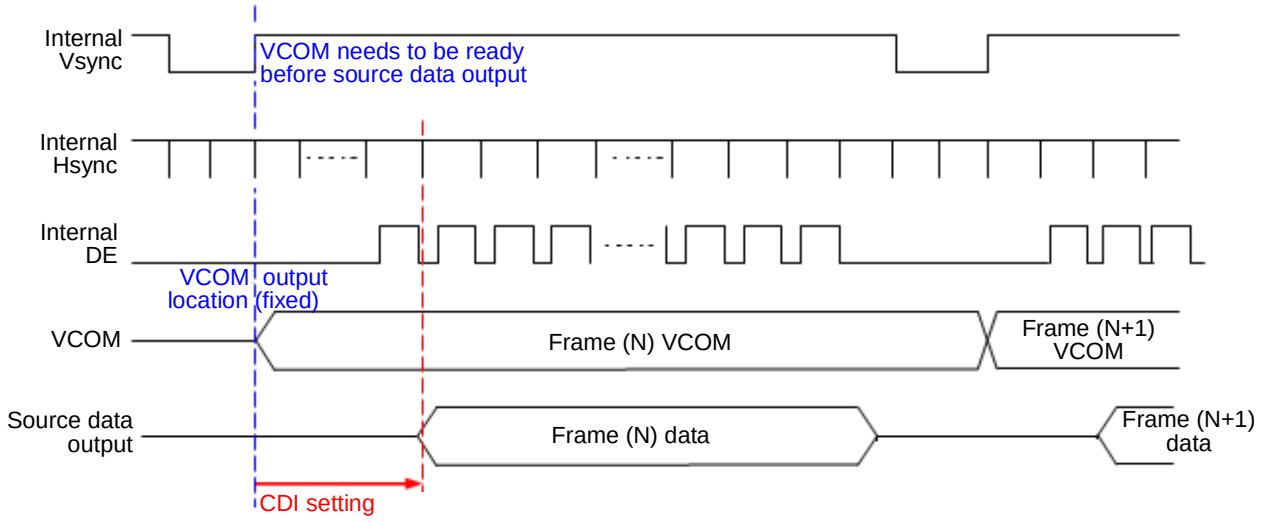
DDX[1:0]: Data polality.

DDX[1] for RED data, DDX[0] for BW data in the B/W/Red mode.
DDX[0] for B/W mode.

CDI[3:0]: Vcom and data interval

CDI[3:0]	Vcom and Data Interval
0000 b	17 hsync
0001	16
0010	15
0011	14
0100	13
0101	12
0110	11
0111	10 (Default)

CDI[3:0]	Vcom and Data Interval
1000	9
1001	8
1010	7
1011	6
1100	5
1101	4
1110	3
1111	2



(23) LOW POWER DETECTION (LPD) (R51H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Detect Low Power	0	0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**1**	51h
	1	1	-	-	-	-	-	-	-	LPD	01h

This command indicates the input power condition. Host can read this flag to learn the battery condition.

LPD: Internal temperature sensor switch

0: Low power input (V_{DD}<2.5V) **1: Normal status (default)**

(24) TCON SETTING (TCON) (R60H)

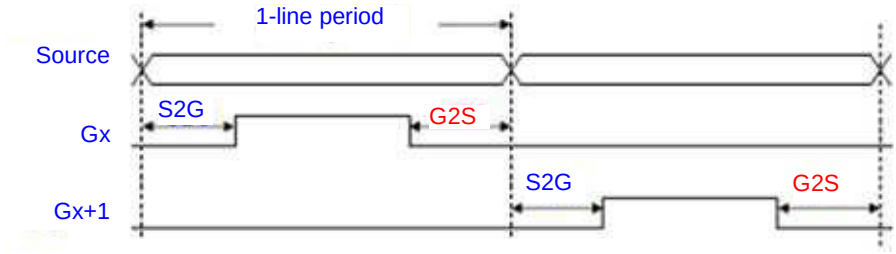
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Sensing Temperature	0	0	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	60h
	0	1	S2G[3:0]				G2S[3:0]				22h

This command defines non-overlap period of Gate and Source.

S2G[3:0] or G2S[3:0]: Source to Gate / Gate to Source Non-overlap period

S2G[3:0] or G2S[3:0]	Period
0000 b	4
0001	8
0010	**12 (Default)**
0011	16
0100	20
0101	24
0110	28
0111	32
1000	36
1001	40
1010	44
1011	48
1100	52
1101	56
1110	60
1111	64

Period = 660 nS.



(25) RESOLUTION SETTING (TRES) (R61H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Display Resolution	0	0	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**1**	61h
	0	1	HRES[7:0]								00h
	0	1	-	-	-	-	-	-	HRES[9:8]		00h
	0	1	VRES[7:0]								00h
	0	1	-	-	-	-	-	-	-	VRES[8]	00h

This command defines alternative resolution and this setting is of higher priority than the RES[1:0] in R00H (PSR).

HRES[9:0]: Horizontal Display Resolution

VRES[8:0]: Vertical Display Resolution

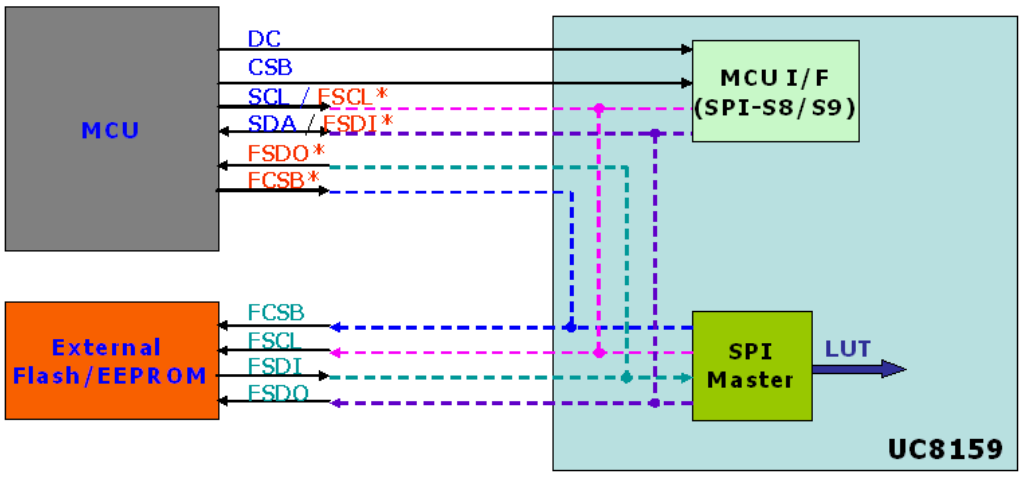
Resolution setting (R61H) has higher priority than RES[1:0] (R00H). Resolution should be even number.

(26) SPI FLASH CONTROL (DAM) (R65H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Sensing Temperature	0	0	**0**	**1**	**1**	**0**	**0**	**1**	**0**	**1**	65h
	0	1	-	-	-	-	-	-	-	DAM	22h

This command defines MCU host direct access external memory mode.

DAM: 0: Disable (Default)
1: Enable. By pass FSCL*, FSDI*, FSDO*, AND FCSB* to external flash.



(27) REVISION (REV) (R70H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Chip Revision	0	0	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	70h
	1	1	-	-	MAN	SHRK	REV[3:0]				00h

The REV is read from OTP address = 0x001.

MAN:

SHRK: Shrink revision or not. **0: Non-shrink revision (default)** 1: Shrink revision

REV[3:0]: Chip Revision.

(28) GET STATUS (FLG) (R71H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read Flags	0	0	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**1**	71h
	1	1	-	-	I2C_ ERR	I2C_ BUSYN	Data_ flag	PON	POF	BUSY_N	

This command reads the IC status.

I2C_ERR: I^2C master error status

I2C_BUSYN: I^2C master busy status (low active)

Data_flag: Driver has already received all the one frame data

PON: Power ON status

POF: Power OFF status

BUSY_N: Driver busy status (low active)

(29) AUTO MEASURE VCOM (AMV) (R80H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Automatically measure Vcom	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	80h
	0	1	-	VCM_EN	AMVT[1:0]		AMVX	AMVS	AMV	AMVE	50h

This command reads the IC status.

VCM_EN: VCOM output Enable

0: VCOM floating. **1: VCOM output.** (default)

AMVT[1:0]: Auto Measure Vcom Time

00b: 3s **01b: 5s (default)**
10b: 8s 11b: 10s

AMVX: Auto Measure VCOM without XON function

0: Measure VCOM without XON function. (Gate scanning) (default)
1: Measure VCOM without XON function. (All Gate ON)

AMVS: Source output of AMV

0: Set Source output to 0V during Auto Measure VCOM period. (default)
1: Set Source output to 3V (or VDPS_L) during Auto Measure VCOM period.

AMV: Analog signal

0: Get Vcom value with the VV command (R81h) (default)
1: Get Vcom value in analog signal.

AMVE: Auto Measure Vcom Enable (/Disable)

0: Disabled 1: Enabled

(30) VCOM VALUE (VV) (R81H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Automatically measure Vcom	0	0	1	0	0	0	0	0	0	1	81h
	1	1	-	VV[6:0]							00h

This command gets the Vcom value.

VV[6:0]: Vcom Value Output

VV[6:0]	Vcom value
000 0000b	(Reserved)
000 0001b	(Reserved)
000 0010b	-0.10 V
000 0011b	-0.15 V
000 0100b	-0.20 V
:	:
101 0000b	-4.0 V
(others)	-4.0 V

(31) VCM_DC SETTING (VDCS) (R82H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set VCM_DC	0	0	1	0	0	0	0	0	1	0	82h
	0	1	-	VDCS[6:0]							0Ch

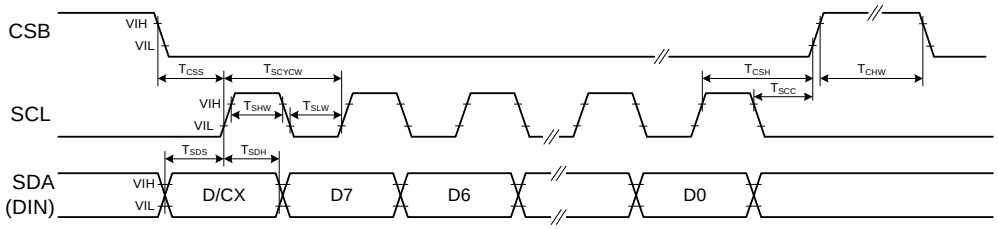
This command sets VCOM_DC value.

VDCS[6:0]: VCOM_DC Setting

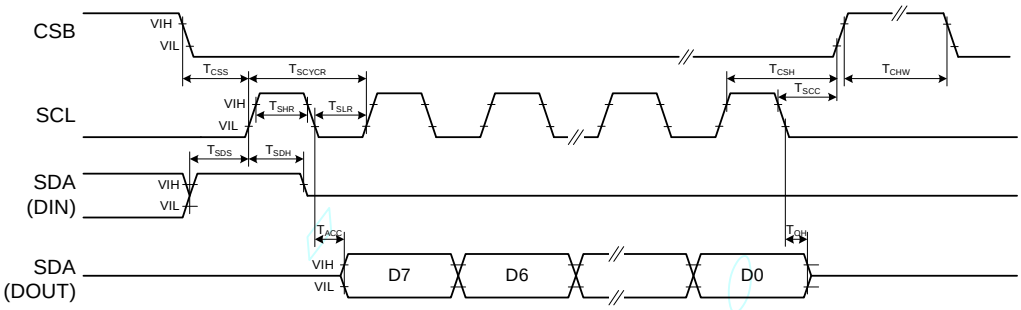
VDCS[6:0]	Vcom_DC value
000 0000b	(Reserved)
000 0001b	(Reserved)
000 0010b	-0.2 V
000 0011b	-0.3 V
000 0100b	-0.4 V
:	:
101 0000b	-4.0 V
(others)	-4.0 V

HOST INTERFACES

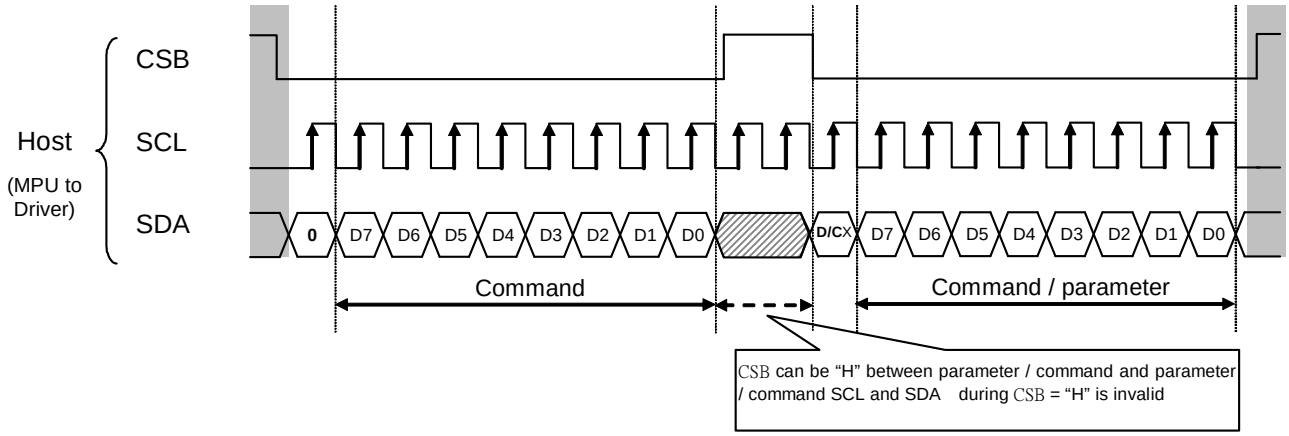
3-WIRE SPI



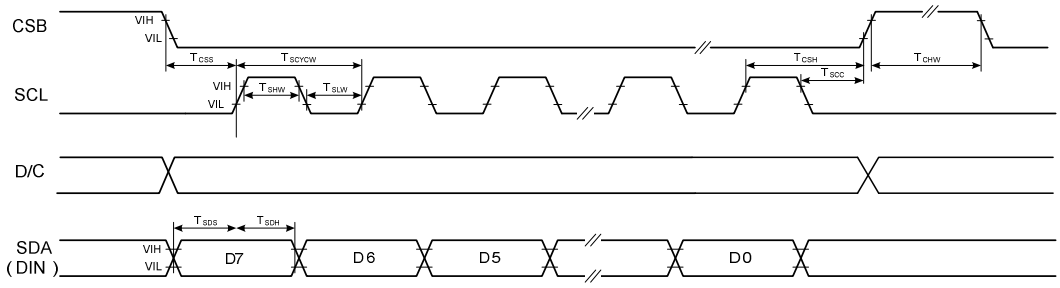
3 pin serial interface characteristics (write mode)



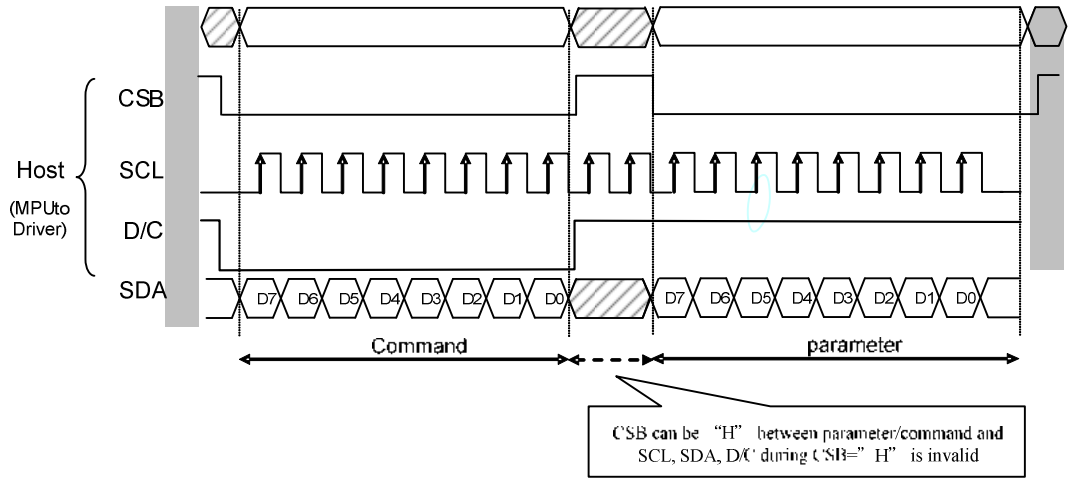
3 pin serial interface characteristics (read mode)



4-WIRE SPI

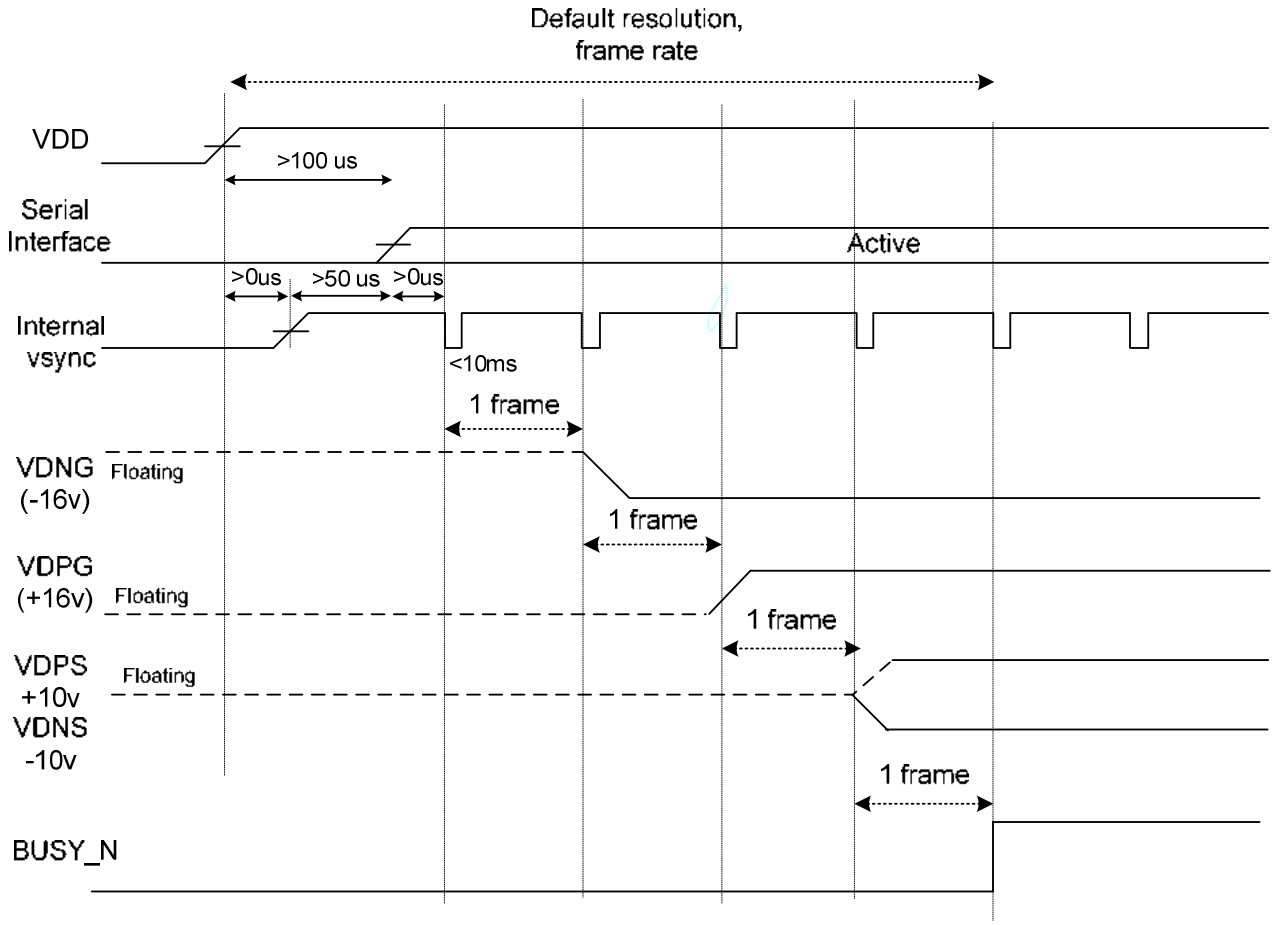


4 pin serial interface characteristics

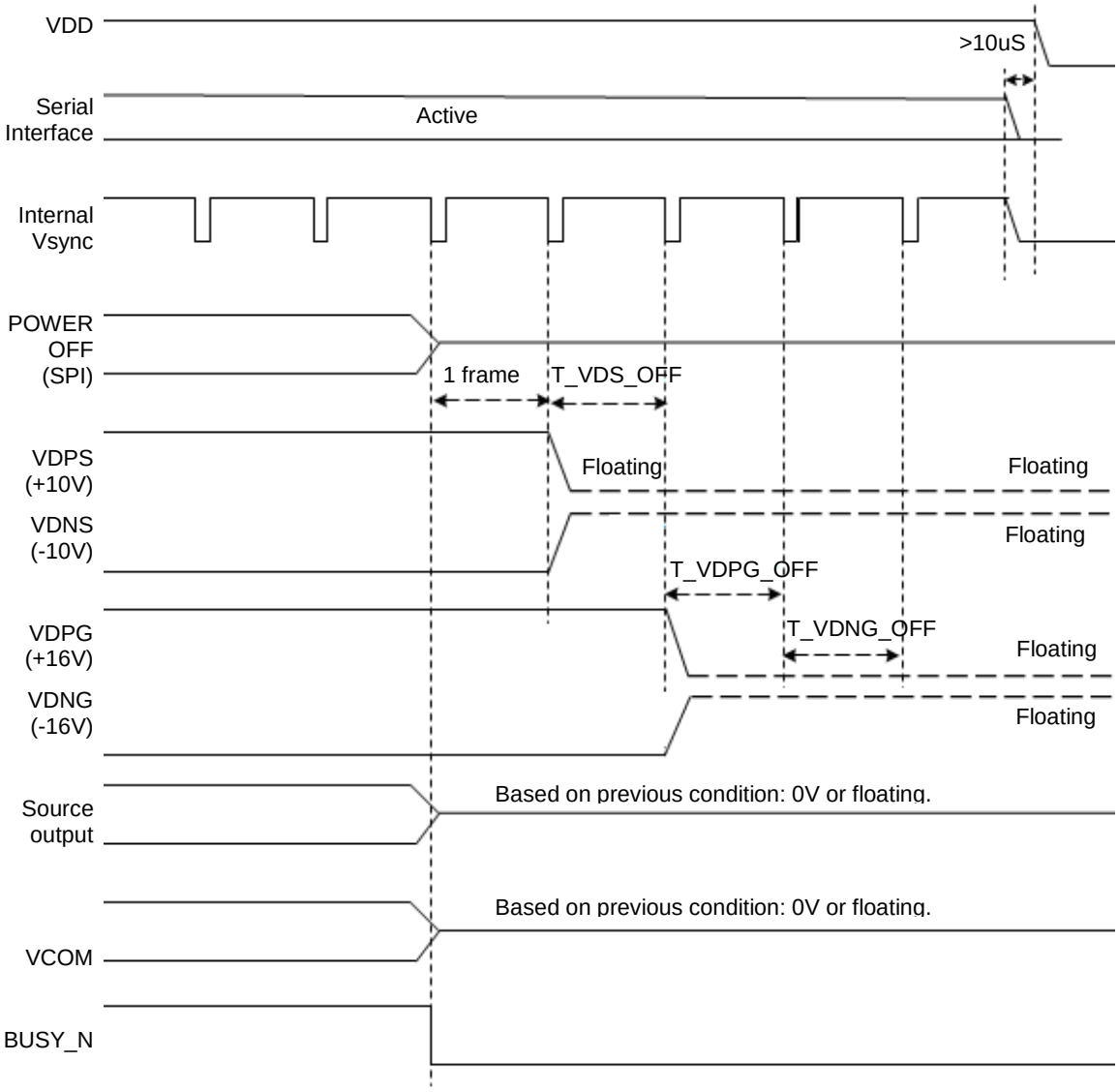


POWER MANAGEMENT

Power ON Sequence



Power OFF Sequence

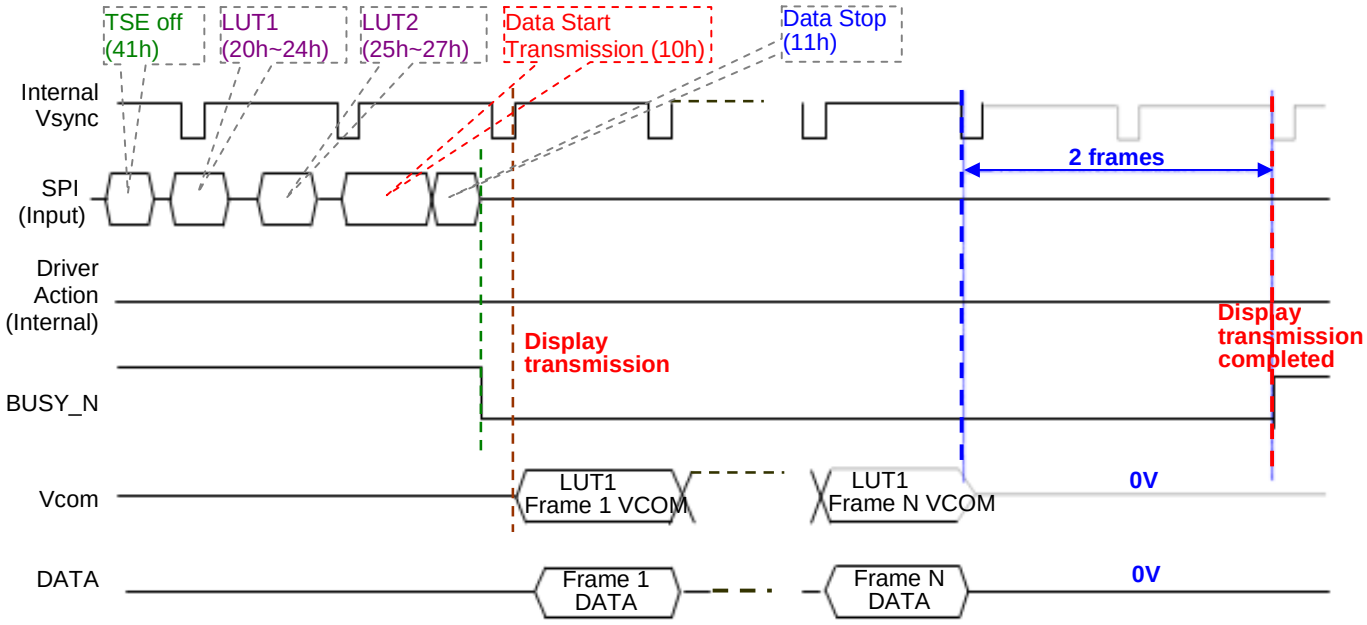


LUT (Lookup Table) Definition

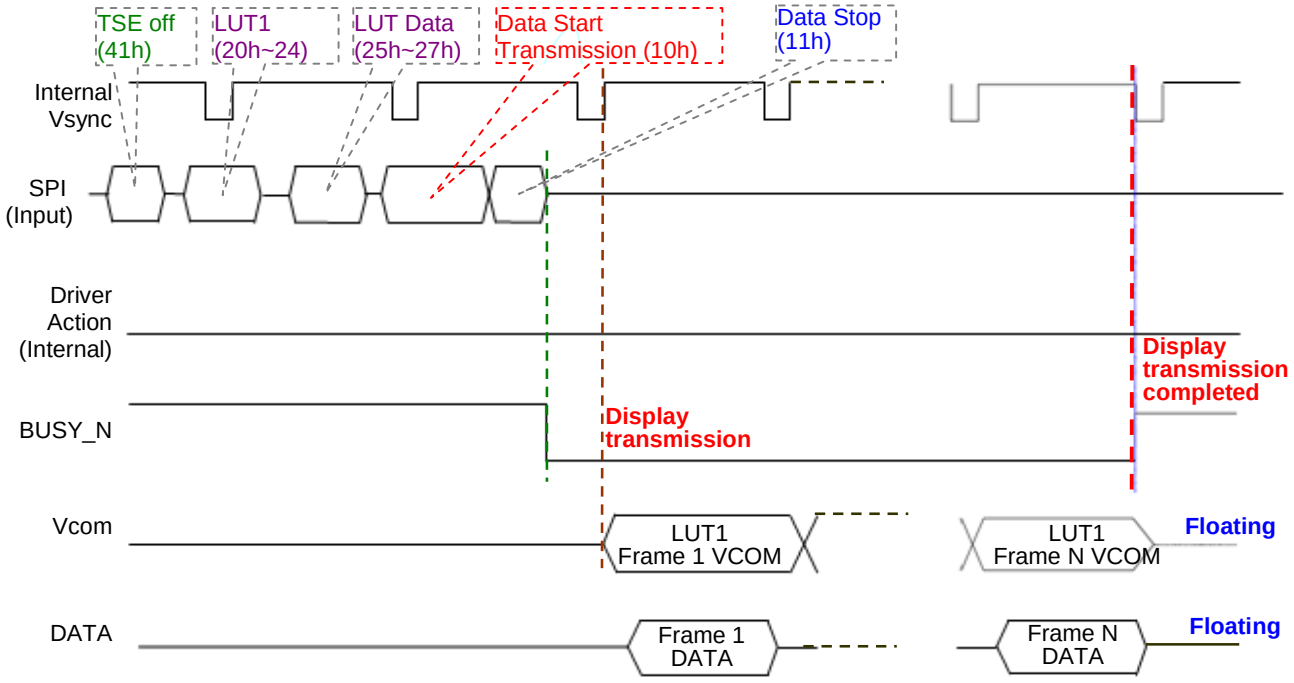
The LUT contains 10 temperature segments for application. And there are waveform, VCOM, XON, VDPS_L, VDNS_L, etc.
The total size of LUT is 25031 bytes.

Data Transmission Waveform

Example 1: LUT all states (10 states) complete or phase number=0, the driver will send 2 frames VCOM and data to 0 V.

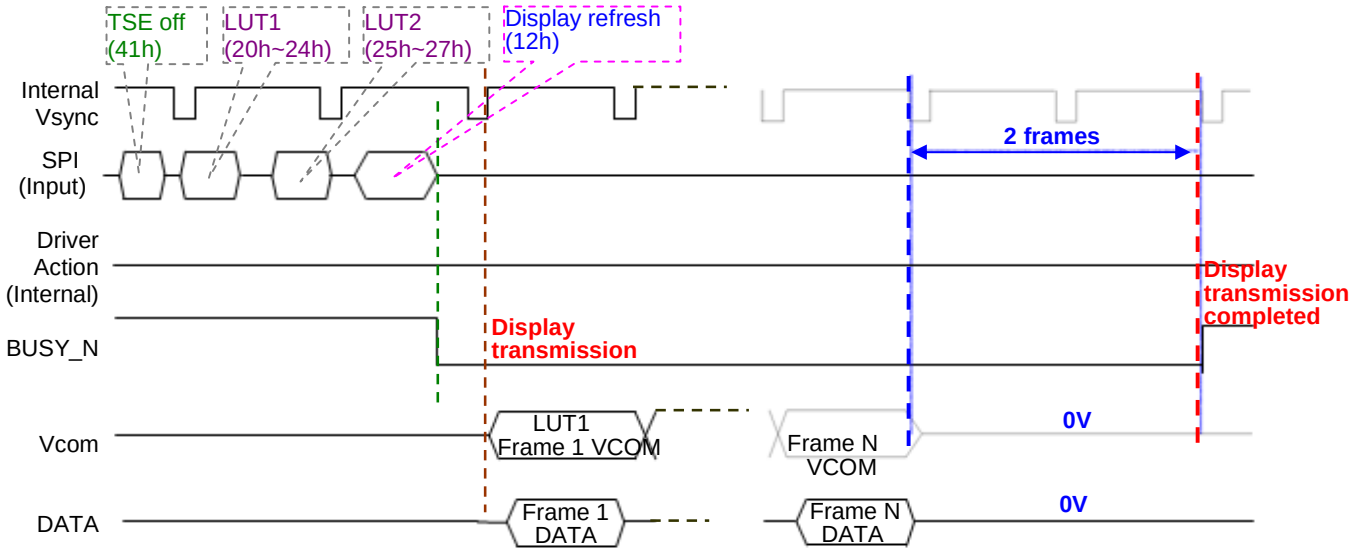


Example 2: While level selection in LUT is "11", the driver will float VCOM and data.

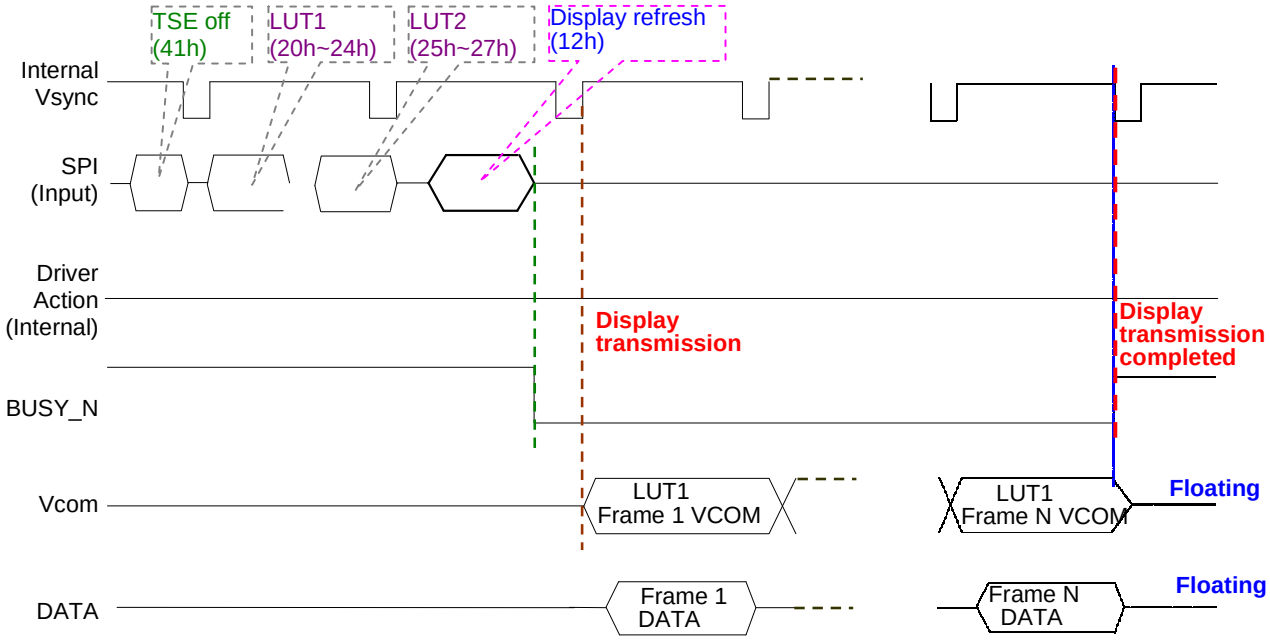


Display Refresh Waveform

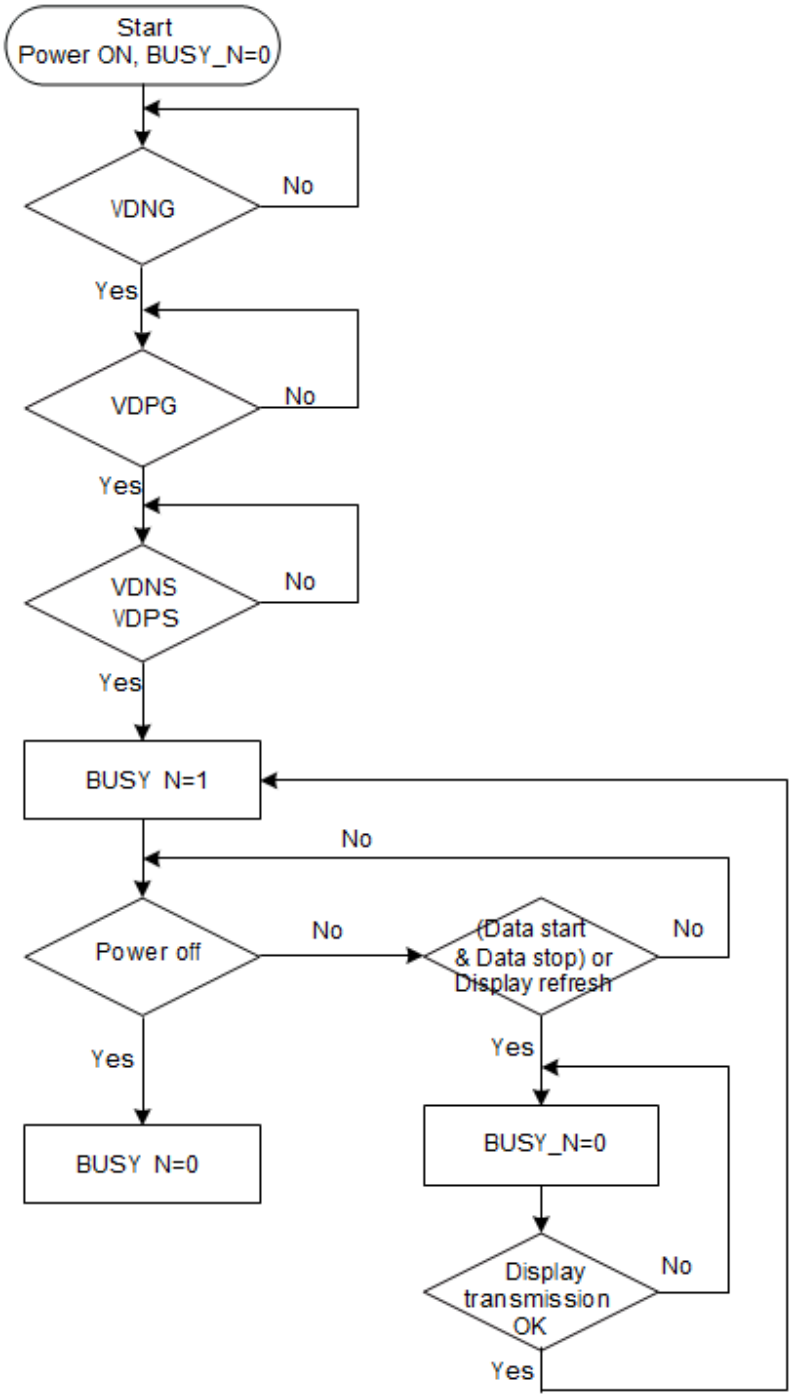
Example 1: LUT all states (10 states) complete or phase number=0, the driver will send 2 frames VCOM and data to 0 V.



Example2: While level selection in LUT is "11", the driver will float VCOM and data.



BUSY_N Signal Flow Chart



BUSY_N Signal Flow Chart

ABSOLUTE MAXIMUM RATINGS

Signal	Item	Min	Max.	Unit
V_{DD}, V_{IO}, V_{DD1}, V_{PP}	Logic Supply voltage	- 0.3	+6.0	V
V_I	Digital input range	-0.3	V_{DDIO}+0.3	V
VDPG-VDNG	Supply range	VDNG-0.3	VDPG+0.3	V
Source				
VDPS	Analog supply voltage – positive	+16		V
VDNS	Analog supply voltage -- nagetive	-16		V
Gate				
V_{DPG}	Analog supply voltage – positive	-0.3	VDNG+42	V
V_{DNG}	Analog supply voltage -- nagetive	VDPG-42	0.3	V
I_{VDPG}	Input rush current for VDH	(TBD)	(TBD)	mA
I_{VDNG}	Input rush current for VDL	(TBD)	(TBD)	mA
T_{STG}	Storage temperature range	-55	+125	^{o}C

Warning:

If ICs are stressed beyond those listed above “absolute maximum ratings”, they may be permanently destroyed. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

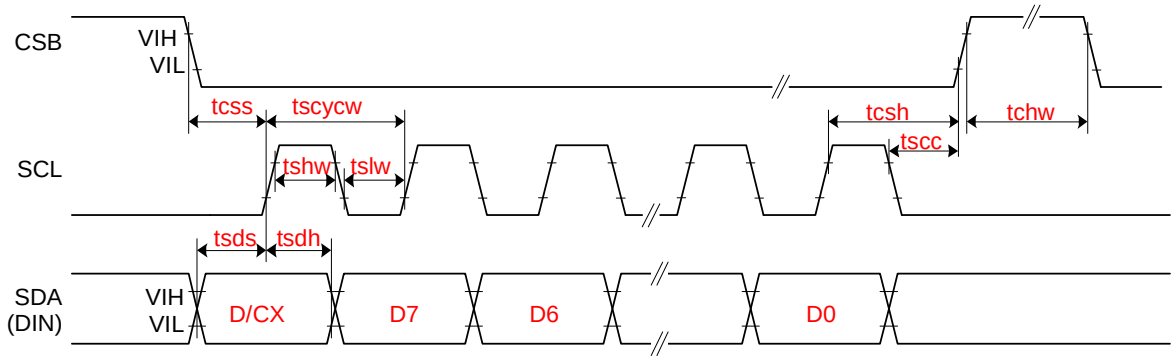
DC CHARACTERISTICS

DIGITAL DC CHARACTERISTICS						
Symbol	**Parameter**	**Conditions**	**MIN.**	**TYP.**	**MAX.**	**Unit**
VIO	IO supply voltage		2.3	3.3	3.6	V
VDD	Supply voltage		2.3	3.3	3.6	V
VDD1	DCDC driver supply voltage	DRVU, DRVD	2.3	3.3	3.6	V
VIL	LOW Level input voltage	Digital input pins	GND	--	0.3xVDD	V
VIH	HIGH Level input voltage	Digital input pins	0.7xVIO	--	VIO	V
VOH	HIGH Level output voltage	Digital input pins, IOH=400UA	VIO-0.4	--	--	V
VOHD	HIGH Level output voltage	Digital input pins, IOH=400UA, DRVD, DRVU	VDD1-0.4	--	--	V
VOL	LOW Level Output voltage	Digital input pins, IOL=-400UA	GND	--	GND+0.4	V
IIN	Input leakage current	Digital input pins except pull-up, pull-down pin	0	--	±1.0	uA
RIN	Pull-up/down impedance			200		KΩ
ISTVDD	Digital stand-by current	all stopped (power off mode)	--	0	0.1	uV
IVDD	Digital operating current		--	0.5	2.0	mV
ISTVIO	IO stand-by current	all stopped (power off mode)		0.4	1.0	uV
IVIO	IO operating current	No load		--	0.2	mA
ISTVDD1	DCDC stand-by current	all stopped (power off mode)		0	0.01	uA
IVDD1	DCDC operating current	fdcdc=250kHz, No load		--	0.05	mA
		fdcdc=250kHz, External cap: 415pF, NMOS=340pF		0.5	1.0	
Top	Operating temperature		-30		85	°C

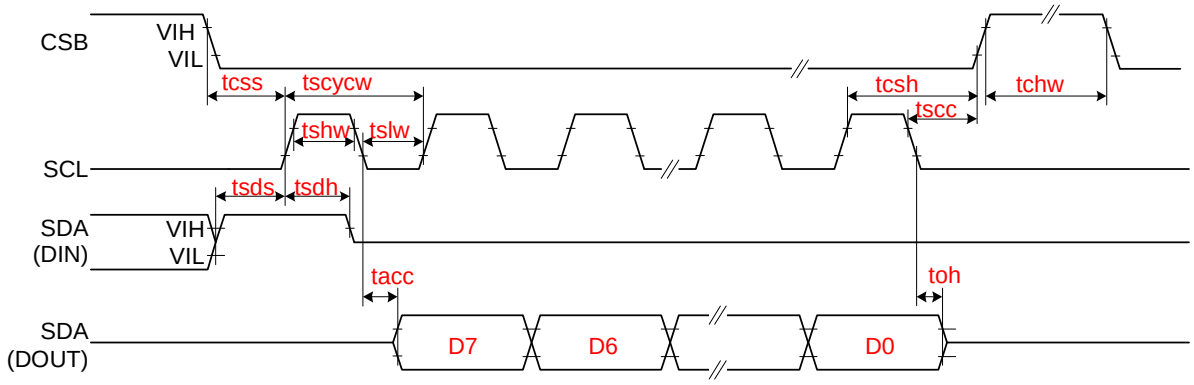
Note: TYP. and MAX. values are to be confirmed by design.

ANALOG DC CHARACTERISTICS						
Symbol	**Parameter**	**Conditions**	**MIN.**	**TYP.**	**MAX.**	**Unit**
VDPS	Supply Voltage	For source driver/VCOM		15		V
dVDPS	Supply voltage dev		-300	0	+300	mV
VDNS	Supply Voltage	For source driver/VCOM		-15		V
dVDNS	Supply voltage dev		-300	0	+300	mV
Idd	Analog Operating Current	No load,		TBD		mA
Vvd	Voltage Deviation of Outputs		--	±16	±35	mV
Vdr	Dynamic Range of Output		0.1	--	VDPS-0.1	V
VDPG-VDPG	Voltage Range of VGH - VGL		12		42	V
VDNG	VGL voltage Range	For gate driver	-20		-18	V
dVDNG	VGL Supply voltage dev		-400	0	+400	mV
VDPG	VGH voltage Range	For gate driver	20		22	V
dVDPG	VGH Supply voltage dev		-400	0	+400	mV
IstVDPG*	Positve HV Stand-by Current (power off mode)	Include VDH power With load	-	0	0.01	µA
IVDPG*	Positve HV Operating Current	Include VDH power With load all SD=L VCOM external resistor divider not included	-	0.7	1.1	mA
		Include VDH power With load all SD=H VCOM external resistor divider not included	-	0.8	1.2	mA
IstVDNG*	Negative HV Stand-by Current (power off mode)	Include VDPNS power With load	-	0	0.01	µA
IVDNG*	Negative HV Operating Current	Include VDL power With load all SD=L	-	0.8	1.2	mA
		Include VDL power With load all SD=H	-	0.9	1.3	mA
IstVINT1*	VINT1 Stand-by Current (power off mode)		-	0	0.01	µA
IVINT1*	VINT1 Operating Current		-	--	0.3	mA
Note: TYP. and MAX. values are to be confirmed by design.						

AC CHARACTERISTICS



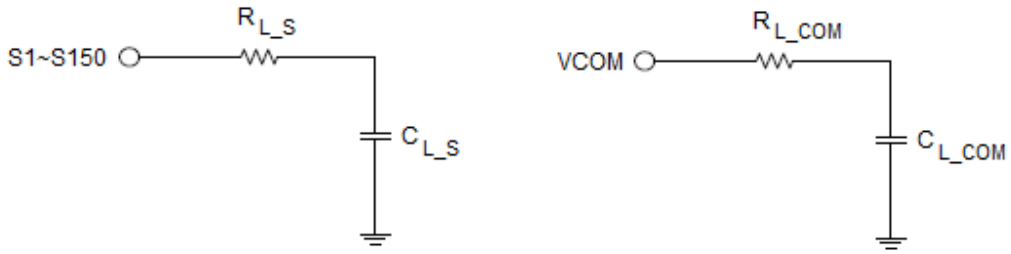
3-wire Serial Interface – Write



3-wire Serial Interface – Read

SYMBOL	SIGNAL			MIN.	TYP.	MAX.	UNIT
SERIAL COMMUNICATION							
tCSS	CSB	Chip select setup time		60			ns
tCSH		Chip select hold time		65			ns
tSCC		Chip select setup time		20			ns
tCHW		Chip select setup time		40			ns
tSCYCW	SCL	Serial clock cycle (Write)		100			ns
tSHW		SCL “H” pulse width (Write)		35			ns
tSLW		SCL “L” pulse width (Write)		35			ns
tSCYCR		Serial clock cycle (Read)		150			ns
tSHR		SCL “H” pulse width (Read)		60			ns
tSLR		SCL “L” pulse width (Read)		60			ns
tSDS	SDA (DIN) (DOUT)	Data setup time		30			ns
tSDH		Data hold time		30			ns
tACC		Access time		10			ns
tOH		Output disable time		15			ns

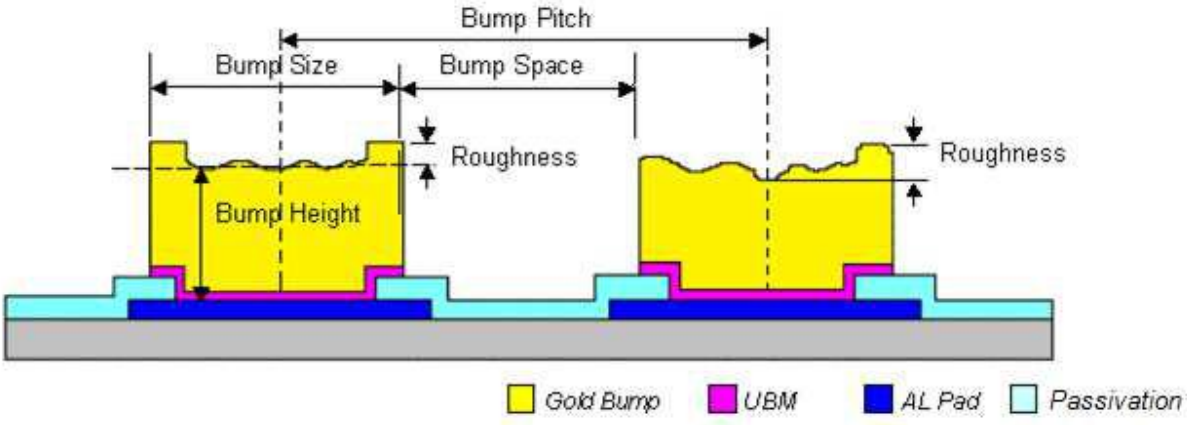
SYMBOL	SIGNAL			MIN.	TYP.	MAX.	UNIT
DRIVER							
trS		Source driver rise time	99% final value		5		uS
tFS		Source driver fall time			5		uS
trG		Gate driver rise time	99% final value		5		uS
tFG		Gate driver fall time			5		uS
trCOM		VCOM rise time	99% final value		1		mS
tFCOM		VCOM fall time			1		mS
RC LOADING							
RS_F	Source driver	Source driver output loading (Fan-out)	Based on 6” panel		1962		Ω
CS_F					5.7		pf
RS_A		Source driver output loading (Active area)			1962		Ω
CS_A					145.2		pf
RS_F	Gate driver	Gate driver output loading (Fan-out)			7533		Ω
CS_F					25.4		pf
RS_A		Gate driver output loading (Active area)			2601		Ω
CS_A					375.4		pf
RC_F	VCOM	VCOM output loading (Fan-out)			5		Ω
CC_F					0.6		pf
RC_A		VCOM output loading (Active area)			83		Ω
CC_A					30888		pf

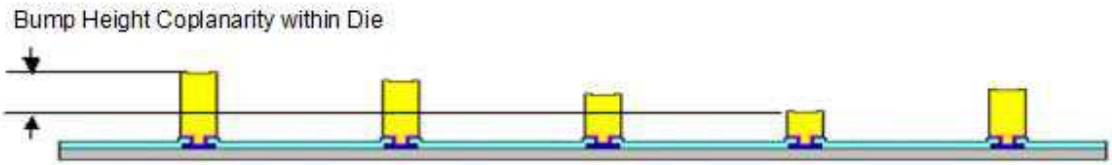


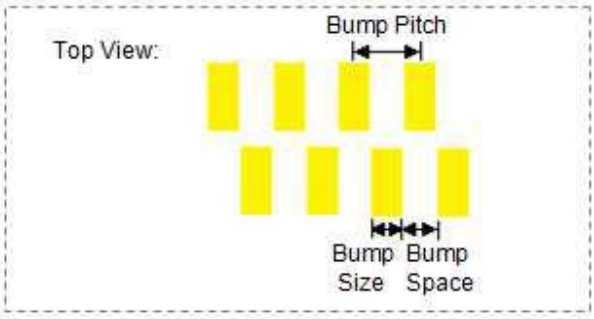
RC Loading

PHYSICAL DIMENSIONS

Die Size:	(17630 μM ± 40μM) x (1680 μM ± 40μM)
Die Thickness:	300 μM ± 20μM
Die TTV:	(D_{MAX} – D_{MIN}) within die ⩽ 2μM
Bump Height:	12 μM ± 3μM
	(H_{MAX} – H_{MIN}) within die ⩽ 2μM
Hardness:	65 Hv ± 15Hv
Bump Size:	12 μM x 100 μM ± 2μM
Bump Area:	1200 μM^2
Bump Pitch:	18 μM
Bump Gap:	15 μM ± 3μM
Shear:	⩾ 5g/Mil^2
Coordinate origin:	Chip center
Pad reference:	Pad center

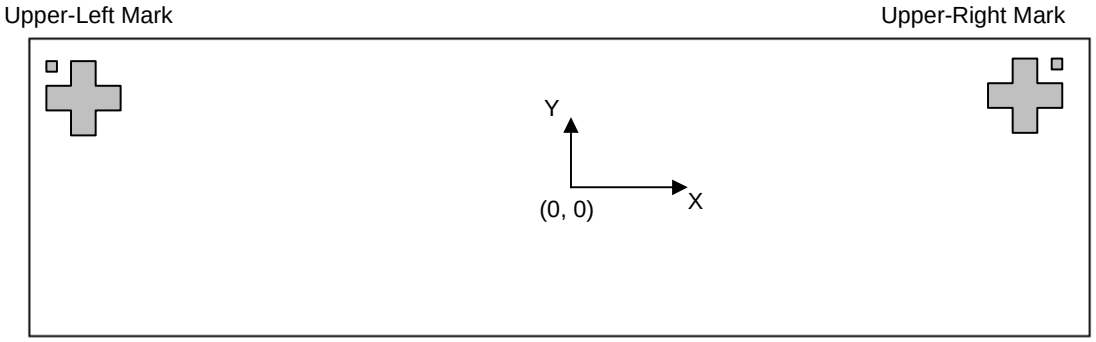




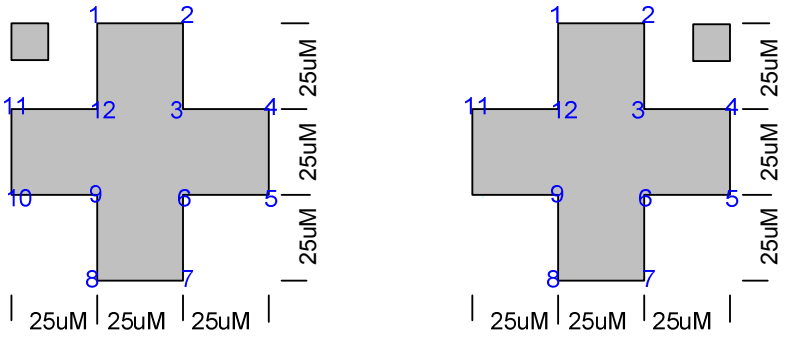


ALIGNMENT MARK INFORMATION

Location:



Shapes and Points:



Point Coordinates:

Point	Upper-Left Mark		Upper-Right Mark	
	X	Y	X	Y
Center	-8700	725	8700	725
1	-8712.5	762.5	8687.5	762.5
2	-8687.5	762.5	8712.5	762.5
3	-8687.5	737.5	8712.5	737.5
4	-8662.5	737.5	8737.5	737.5
5	-8662.5	712.5	8737.5	712.5
6	-8687.5	712.5	8712.5	712.5
7	-8687.5	687.5	8712.5	687.5
8	-8712.5	687.5	8687.5	687.5
9	-8712.5	712.5	8687.5	712.5
10	-8737.5	712.5	8662.5	712.5
11	-8737.5	737.5	8662.5	737.5
12	-8712.5	737.5	8687.5	737.5

PAD COORDINATES

No.	Name	X	Y	W	H
1	DUMMY	-8610	-755	40	50
2	VCOM	-8550	-755	40	50
3	VCOM	-8490	-755	40	50
4	VCOM	-8430	-755	40	50
5	VCOM	-8370	-755	40	50
6	VCOM	-8310	-755	40	50
7	VCOM	-8250	-755	40	50
8	VCOM	-8190	-755	40	50
9	VCOM	-8130	-755	40	50
10	PATH1	-8070	-755	40	50
11	VDM	-8010	-755	40	50
12	VDM	-7950	-755	40	50
13	VGL	-7890	-755	40	50
14	VGL	-7830	-755	40	50
15	VGL	-7770	-755	40	50
16	VGL	-7710	-755	40	50
17	VGL	-7650	-755	40	50
18	VGL	-7590	-755	40	50
19	VGL	-7530	-755	40	50
20	VGL	-7470	-755	40	50
21	VGL	-7410	-755	40	50
22	VGL	-7350	-755	40	50
23	VGL	-7290	-755	40	50
24	VGL	-7230	-755	40	50
25	VGL	-7170	-755	40	50
26	VGL	-7110	-755	40	50
27	VGL	-7050	-755	40	50
28	VGL	-6990	-755	40	50
29	GNDA	-6930	-755	40	50
30	VSL	-6870	-755	40	50
31	VSL	-6810	-755	40	50
32	VSL	-6750	-755	40	50
33	VSL	-6690	-755	40	50
34	VSL	-6630	-755	40	50
35	VSL	-6570	-755	40	50
36	VSL	-6510	-755	40	50
37	VSL	-6450	-755	40	50
38	VSL	-6390	-755	40	50
39	VSL	-6330	-755	40	50
40	GNDA	-6270	-755	40	50
42	VSL_LV	-6210	-755	40	50
41	VSL_LV	-6150	-755	40	50
43	VSL_LV	-6090	-755	40	50
44	VSL_LV	-6030	-755	40	50
45	VSL_LV	-5970	-755	40	50
46	VSL_LV	-5910	-755	40	50
47	VSL_LV	-5850	-755	40	50
48	VSL_LV	-5790	-755	40	50
49	VSL_LV	-5730	-755	40	50
50	VSL_LV	-5670	-755	40	50
51	GNDA	-5610	-755	40	50
52	VSL_LVX	-5550	-755	40	50
53	VSL_LVX	-5490	-755	40	50
54	VSL_LVX	-5430	-755	40	50
55	VSL_LVX	-5370	-755	40	50
56	VSL_LVX	-5310	-755	40	50
57	VSL_LVX	-5250	-755	40	50
58	VSL_LVX	-5190	-755	40	50

No.	Name	X	Y	W	H
59	VSL_LVX	-5130	-755	40	50
60	GNDA	-5070	-755	40	50
61	VGH	-5010	-755	40	50
62	VGH	-4950	-755	40	50
63	VGH	-4890	-755	40	50
64	VGH	-4830	-755	40	50
65	VGH	-4770	-755	40	50
66	VGH	-4710	-755	40	50
67	VGH	-4650	-755	40	50
68	VGH	-4590	-755	40	50
69	VGH	-4530	-755	40	50
70	VGH	-4470	-755	40	50
71	VGH	-4410	-755	40	50
72	VGH	-4350	-755	40	50
73	GNDA	-4290	-755	40	50
74	VSH	-4230	-755	40	50
75	VSH	-4170	-755	40	50
76	VSH	-4110	-755	40	50
77	VSH	-4050	-755	40	50
78	VSH	-3990	-755	40	50
79	VSH	-3930	-755	40	50
80	VSH	-3870	-755	40	50
81	VSH	-3810	-755	40	50
82	VSH	-3750	-755	40	50
83	VSH	-3690	-755	40	50
84	GNDA	-3630	-755	40	50
85	VSH_LV	-3570	-755	40	50
86	VSH_LV	-3510	-755	40	50
87	VSH_LV	-3450	-755	40	50
88	VSH_LV	-3390	-755	40	50
89	VSH_LV	-3330	-755	40	50
90	VSH_LV	-3270	-755	40	50
91	VSH_LV	-3210	-755	40	50
92	VSH_LV	-3150	-755	40	50
93	VSH_LV	-3090	-755	40	50
94	VSH_LV	-3030	-755	40	50
95	GNDA	-2970	-755	40	50
96	VSH_LVX	-2910	-755	40	50
97	VSH_LVX	-2850	-755	40	50
98	VSH_LVX	-2790	-755	40	50
99	VSH_LVX	-2730	-755	40	50
100	VSH_LVX	-2670	-755	40	50
101	VSH_LVX	-2610	-755	40	50
102	VSH_LVX	-2550	-755	40	50
103	VSH_LVX	-2490	-755	40	50
104	GNDA	-2430	-755	40	50
105	VDDD	-2370	-755	40	50
106	VDDD	-2310	-755	40	50
107	VDDD	-2250	-755	40	50
108	VDDD	-2190	-755	40	50
109	VDDD	-2130	-755	40	50
110	VDDD	-2070	-755	40	50
111	VDDDO	-2010	-755	40	50
112	VDDDO	-1950	-755	40	50
113	VDDDO	-1890	-755	40	50
114	VDDDO	-1830	-755	40	50
115	VDDDO	-1770	-755	40	50
116	VDDDO	-1710	-755	40	50

No.	Name	X	Y	W	H
117	GND	-1650	-755	40	50
118	VDM	-1590	-755	40	50
119	VDM	-1530	-755	40	50
120	GND	-1470	-755	40	50
121	GND	-1410	-755	40	50
122	GND	-1350	-755	40	50
123	GND	-1290	-755	40	50
124	GND	-1230	-755	40	50
125	GND	-1170	-755	40	50
126	GND	-1110	-755	40	50
127	GND	-1050	-755	40	50
128	GND	-990	-755	40	50
129	GND	-930	-755	40	50
130	GNDA	-870	-755	40	50
131	GNDA	-810	-755	40	50
132	GNDA	-750	-755	40	50
133	GNDA	-690	-755	40	50
134	GNDA	-630	-755	40	50
135	GNDA	-570	-755	40	50
136	GNDA	-510	-755	40	50
137	GNDA	-450	-755	40	50
138	GNDA	-390	-755	40	50
139	GNDA	-330	-755	40	50
140	GNDA	-270	-755	40	50
141	VDDA	-210	-755	40	50
142	VDDA	-150	-755	40	50
143	VDDA	-90	-755	40	50
144	VDDA	-30	-755	40	50
145	VDDA	30	-755	40	50
146	VDDA	90	-755	40	50
147	VDDA	150	-755	40	50
148	VDDA	210	-755	40	50
149	VDDA	270	-755	40	50
150	VDDA	330	-755	40	50
151	VDD	390	-755	40	50
152	VDD	450	-755	40	50
153	VDD	510	-755	40	50
154	VDD	570	-755	40	50
155	VDD	630	-755	40	50
156	VDD	690	-755	40	50
157	VDD	750	-755	40	50
158	VDD	810	-755	40	50
159	VDD	870	-755	40	50
160	VDD	930	-755	40	50
161	TEST1	990	-755	40	50
162	TEST2	1050	-755	40	50
163	VDDIO	1110	-755	40	50
164	VDDIO	1170	-755	40	50
165	VDDIO	1230	-755	40	50
166	VDDIO	1290	-755	40	50
167	TEST3	1350	-755	40	50
168	XCLK	1410	-755	40	50
169	XSTL	1470	-755	40	50
170	XOE	1530	-755	40	50
171	XLE	1590	-755	40	50
172	EDATA<0>	1650	-755	40	50
173	EDATA<1>	1710	-755	40	50
174	EDATA<2>	1770	-755	40	50
175	EDATA<3>	1830	-755	40	50
176	EDATA<4>	1890	-755	40	50

No.	Name	X	Y	W	H
177	EDATA<5>	1950	-755	40	50
178	EDATA<6>	2010	-755	40	50
179	EDATA<7>	2070	-755	40	50
180	GND	2130	-755	40	50
181	GCLK	2190	-755	40	50
182	STV	2250	-755	40	50
183	VDDIO	2310	-755	40	50
184	XON	2370	-755	40	50
185	DEN	2430	-755	40	50
186	GND	2490	-755	40	50
187	GND	2550	-755	40	50
188	FCSB	2610	-755	40	50
189	GND	2670	-755	40	50
190	FSCL	2730	-755	40	50
191	GND	2790	-755	40	50
192	FSDO	2850	-755	40	50
193	FSDI	2910	-755	40	50
194	SCL	2970	-755	40	50
195	SDA	3030	-755	40	50
196	GND	3090	-755	40	50
197	CSB	3150	-755	40	50
198	VDDIO	3210	-755	40	50
199	MFCSB	3270	-755	40	50
200	GND	3330	-755	40	50
201	DC	3390	-755	40	50
202	VDDIO	3450	-755	40	50
203	FMSDO	3510	-755	40	50
204	BUSY_N	3570	-755	40	50
205	GND	3630	-755	40	50
206	RST_N	3690	-755	40	50
207	TESTVDD	3750	-755	40	50
208	DUMMY	3810	-755	40	50
209	DUMMY	3870	-755	40	50
210	VDDIO	3930	-755	40	50
211	BS	3990	-755	40	50
212	GND	4050	-755	40	50
213	GND	4110	-755	40	50
214	VDD	4170	-755	40	50
215	VDD	4230	-755	40	50
216	VDDA	4290	-755	40	50
217	VDDA	4350	-755	40	50
218	TSDA	4410	-755	40	50
219	TSDA	4470	-755	40	50
220	TSCL	4530	-755	40	50
221	TSCL	4590	-755	40	50
222	GND	4650	-755	40	50
223	TEST4	4710	-755	40	50
224	GND	4770	-755	40	50
225	TEST5	4830	-755	40	50
226	GND	4890	-755	40	50
227	TEST6	4950	-755	40	50
228	GND	5010	-755	40	50
229	TEST7	5070	-755	40	50
230	TEST8	5130	-755	40	50
231	TEST9	5190	-755	40	50
232	TEST10	5250	-755	40	50
233	TEST11	5310	-755	40	50
234	TEST12	5370	-755	40	50
235	TEST13	5430	-755	40	50
236	TEST14	5490	-755	40	50

No.	Name	X	Y	W	H
237	TEST15	5550	-755	40	50
238	VCOMVS<0>	5610	-755	40	50
239	VCOMVS<1>	5670	-755	40	50
240	FSOURCE	5730	-755	40	50
241	FSOURCE	5790	-755	40	50
242	FSOURCE	5850	-755	40	50
243	VPPM	5910	-755	40	50
244	VPPM	5970	-755	40	50
245	VPPM	6030	-755	40	50
246	VPPM	6090	-755	40	50
247	VPPM	6150	-755	40	50
248	VPPM	6210	-755	40	50
249	VGH	6270	-755	40	50
250	VGH	6330	-755	40	50
251	VGH	6390	-755	40	50
252	VGH	6450	-755	40	50
253	VGH	6510	-755	40	50
254	VGH	6570	-755	40	50
255	VGH	6630	-755	40	50
256	VGH	6690	-755	40	50
257	VGL	6750	-755	40	50
258	VGL	6810	-755	40	50
259	VGL	6870	-755	40	50
260	VGL	6930	-755	40	50
261	VGL	6990	-755	40	50
262	VGL	7050	-755	40	50
263	VGL	7110	-755	40	50
264	GNDA	7170	-755	40	50
265	FB	7230	-755	40	50
266	FB	7290	-755	40	50
267	GNDA	7350	-755	40	50
268	RESE	7410	-755	40	50
269	RESE	7470	-755	40	50
270	GNDA	7530	-755	40	50
271	GDR	7590	-755	40	50
272	GDR	7650	-755	40	50
273	GDR	7710	-755	40	50
274	GDR	7770	-755	40	50
275	GDR	7830	-755	40	50
276	GDR	7890	-755	40	50
277	VDM	7950	-755	40	50
278	VDM	8010	-755	40	50
279	PATH1	8070	-755	40	50
280	VCOM	8130	-755	40	50
281	VCOM	8190	-755	40	50
282	VCOM	8250	-755	40	50
283	VCOM	8310	-755	40	50
284	VCOM	8370	-755	40	50
285	VCOM	8430	-755	40	50
286	VCOM	8490	-755	40	50
287	VCOM	8550	-755	40	50
288	DUMMY	8610	-755	40	50
289	DUMMY	8617	626	12	100
290	DUMMY	8602	751	12	100
291	G<0>	8587	626	12	100
292	G<2>	8572	751	12	100
293	G<4>	8557	626	12	100
294	G<6>	8542	751	12	100
295	G<8>	8527	626	12	100
296	G<10>	8512	751	12	100

No.	Name	X	Y	W	H
297	G<12>	8497	626	12	100
298	G<14>	8482	751	12	100
299	G<16>	8467	626	12	100
300	G<18>	8452	751	12	100
301	G<20>	8437	626	12	100
302	G<22>	8422	751	12	100
303	G<24>	8407	626	12	100
304	G<26>	8392	751	12	100
305	G<28>	8377	626	12	100
306	G<30>	8362	751	12	100
307	G<32>	8347	626	12	100
308	G<34>	8332	751	12	100
309	G<36>	8317	626	12	100
310	G<38>	8302	751	12	100
311	G<40>	8287	626	12	100
312	G<42>	8272	751	12	100
313	G<44>	8257	626	12	100
314	G<46>	8242	751	12	100
315	G<48>	8227	626	12	100
316	G<50>	8212	751	12	100
317	G<52>	8197	626	12	100
318	G<54>	8182	751	12	100
319	G<56>	8167	626	12	100
320	G<58>	8152	751	12	100
321	G<60>	8137	626	12	100
322	G<62>	8122	751	12	100
323	G<64>	8107	626	12	100
324	G<66>	8092	751	12	100
325	G<68>	8077	626	12	100
326	G<70>	8062	751	12	100
327	G<72>	8047	626	12	100
328	G<74>	8032	751	12	100
329	G<76>	8017	626	12	100
330	G<78>	8002	751	12	100
331	G<80>	7987	626	12	100
332	G<82>	7972	751	12	100
333	G<84>	7957	626	12	100
334	G<86>	7942	751	12	100
335	G<88>	7927	626	12	100
336	G<90>	7912	751	12	100
337	G<92>	7897	626	12	100
338	G<94>	7882	751	12	100
339	G<96>	7867	626	12	100
340	G<98>	7852	751	12	100
341	G<100>	7837	626	12	100
342	G<102>	7822	751	12	100
343	G<104>	7807	626	12	100
344	G<106>	7792	751	12	100
345	G<108>	7777	626	12	100
346	G<110>	7762	751	12	100
347	G<112>	7747	626	12	100
348	G<114>	7732	751	12	100
349	G<116>	7717	626	12	100
350	G<118>	7702	751	12	100
351	G<120>	7687	626	12	100
352	G<122>	7672	751	12	100
353	G<124>	7657	626	12	100
354	G<126>	7642	751	12	100
355	G<128>	7627	626	12	100
356	G<130>	7612	751	12	100

No.	Name	X	Y	W	H
357	G<132>	7597	626	12	100
358	G<134>	7582	751	12	100
359	G<136>	7567	626	12	100
360	G<138>	7552	751	12	100
361	G<140>	7537	626	12	100
362	G<142>	7522	751	12	100
363	G<144>	7507	626	12	100
364	G<146>	7492	751	12	100
365	G<148>	7477	626	12	100
366	G<150>	7462	751	12	100
367	G<152>	7447	626	12	100
368	G<154>	7432	751	12	100
369	G<156>	7417	626	12	100
370	G<158>	7402	751	12	100
371	G<160>	7387	626	12	100
372	G<162>	7372	751	12	100
373	G<164>	7357	626	12	100
374	G<166>	7342	751	12	100
375	G<168>	7327	626	12	100
376	G<170>	7312	751	12	100
377	G<172>	7297	626	12	100
378	G<174>	7282	751	12	100
379	G<176>	7267	626	12	100
380	G<178>	7252	751	12	100
381	G<180>	7237	626	12	100
382	G<182>	7222	751	12	100
383	G<184>	7207	626	12	100
384	G<186>	7192	751	12	100
385	G<188>	7177	626	12	100
386	G<190>	7162	751	12	100
387	G<192>	7147	626	12	100
388	G<194>	7132	751	12	100
389	G<196>	7117	626	12	100
390	G<198>	7102	751	12	100
391	G<200>	7087	626	12	100
392	G<202>	7072	751	12	100
393	G<204>	7057	626	12	100
394	G<206>	7042	751	12	100
395	G<208>	7027	626	12	100
396	G<210>	7012	751	12	100
397	G<212>	6997	626	12	100
398	G<214>	6982	751	12	100
399	G<216>	6967	626	12	100
400	G<218>	6952	751	12	100
401	G<220>	6937	626	12	100
402	G<222>	6922	751	12	100
403	G<224>	6907	626	12	100
404	G<226>	6892	751	12	100
405	G<228>	6877	626	12	100
406	G<230>	6862	751	12	100
407	G<232>	6847	626	12	100
408	G<234>	6832	751	12	100
409	G<236>	6817	626	12	100
410	G<238>	6802	751	12	100
411	G<240>	6787	626	12	100
412	G<242>	6772	751	12	100
413	G<244>	6757	626	12	100
414	G<246>	6742	751	12	100
415	G<248>	6727	626	12	100
416	G<250>	6712	751	12	100

No.	Name	X	Y	W	H
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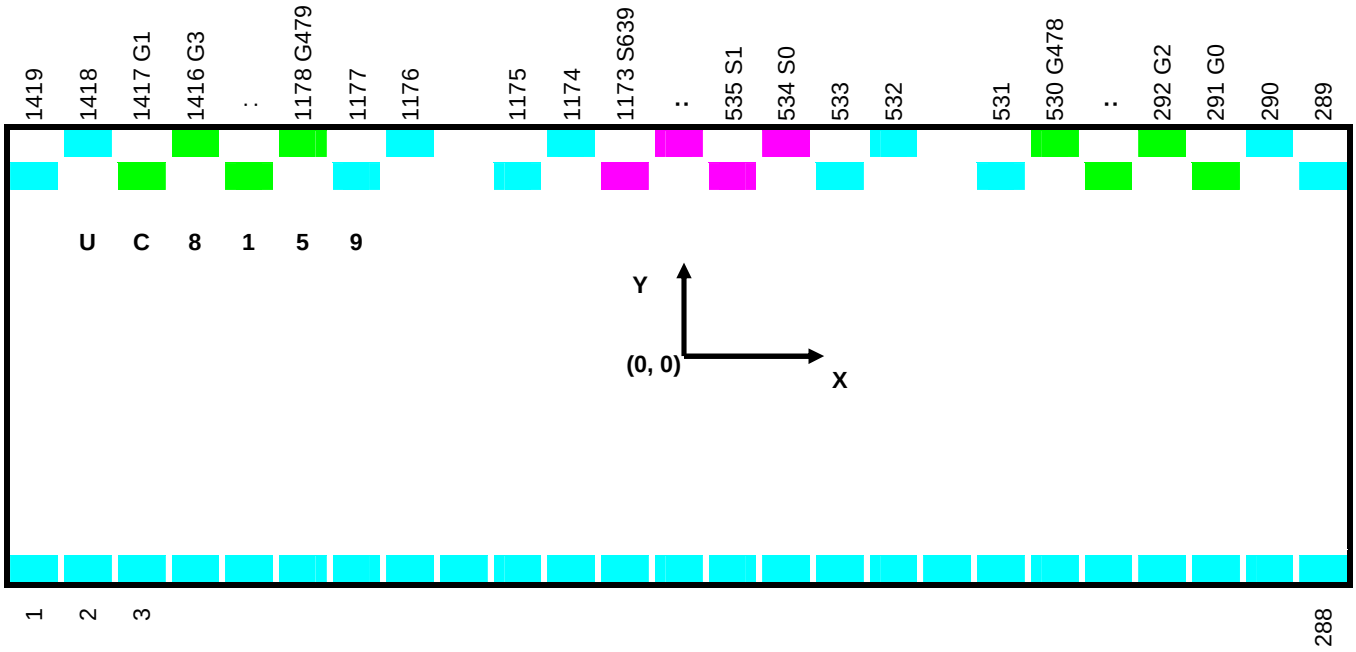
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TRAY INFORMATION

(TBD)

REVISION HISTORY

Revision	• Contents	• Date
	(N/A)	