Formal Verification of AHB-to-APB Bridge

Yelin Mao, Yuxiang Xia,
Hongkuan Yu

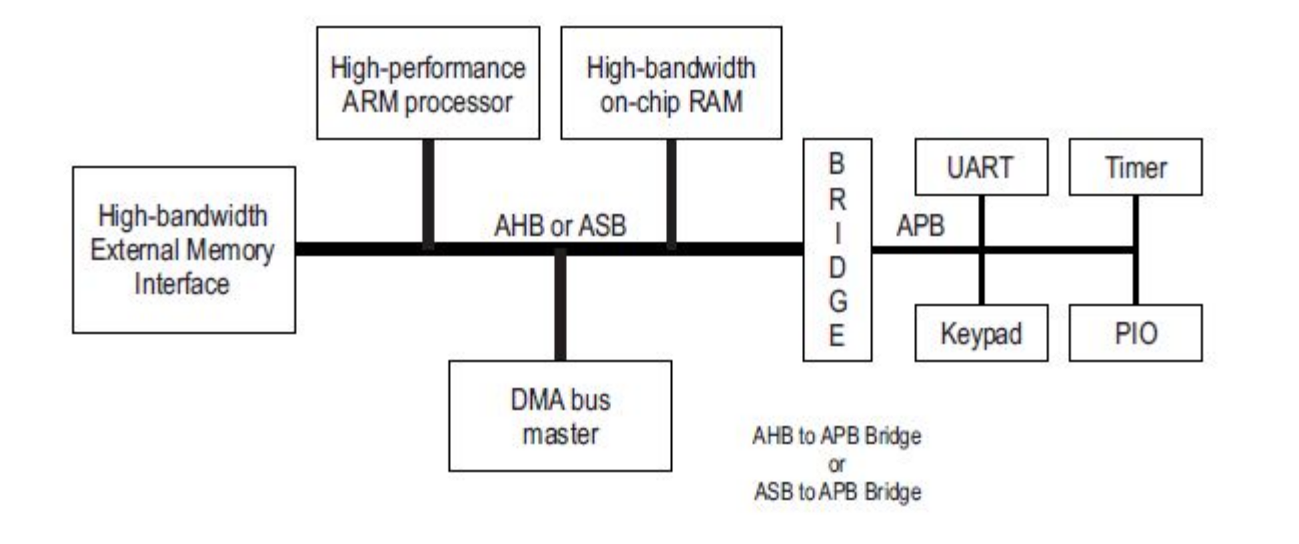
UNI: ym3000, yx2821, hy2819

Fall 2024

Introduction

Project Overview:

- Formal verification of the AHB-to-APB bridge
- Communication between the high-performance AHB and low-power APB buses



High-performance ARM processor
High-bandwidth on-chip RAM
High-bandwidth External Memory Interface
AHB or ASB
B R I D G E
UART
Timer
APB
Keypad
PIO
DMA bus master
AHB to APB Bridge or ASB to APB Bridge

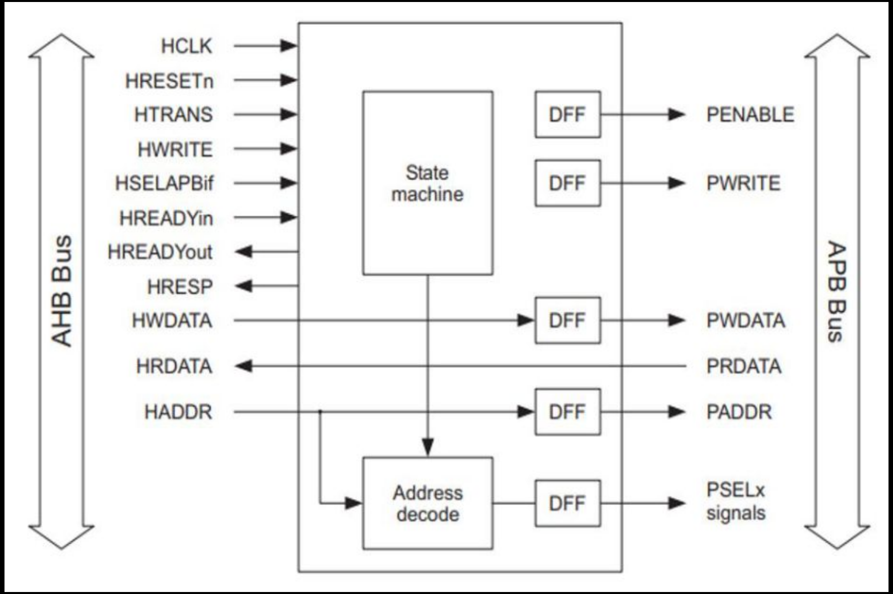
Verification Tools:

- Using SystemVerilog Assertions (SVA)
- Cadence Jasper Gold
- Siemens Modelsim

Structure

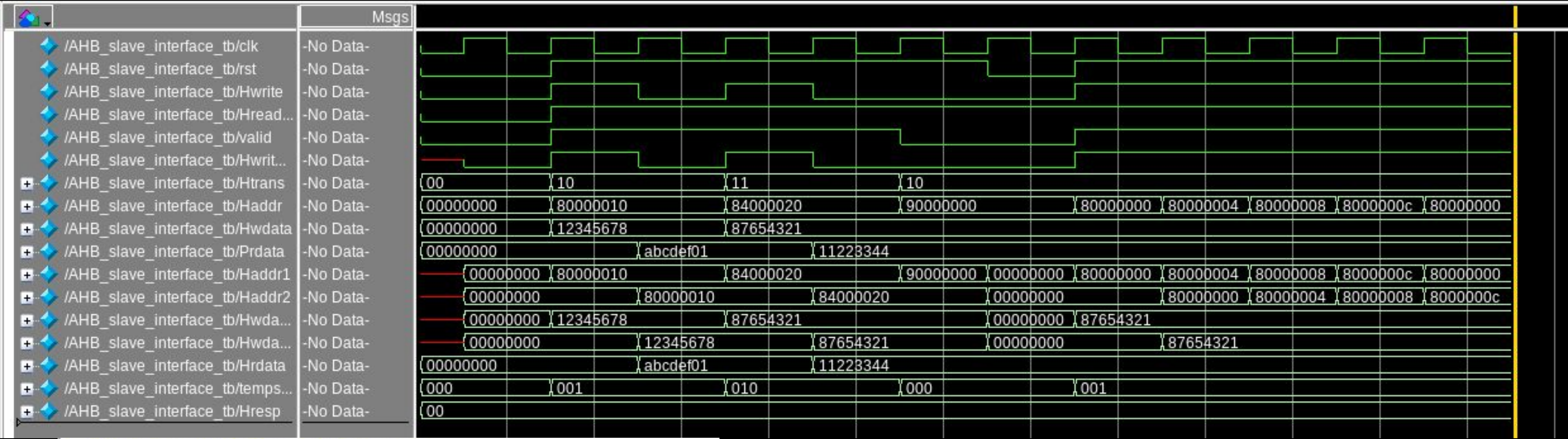
Three components:

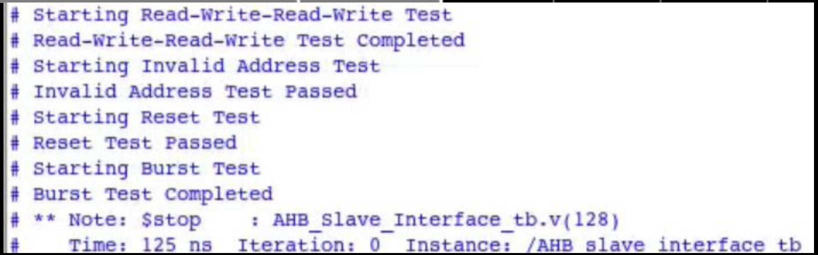
- AHB_Interface
  - Manages AHB bus communication
- APB_FSM
  - Controls APB data transfer via an independent finite state machine
- TOP
  - Integrates AHB and APB components for seamless communication



I/O Ports

Stimulation - AHB Interface

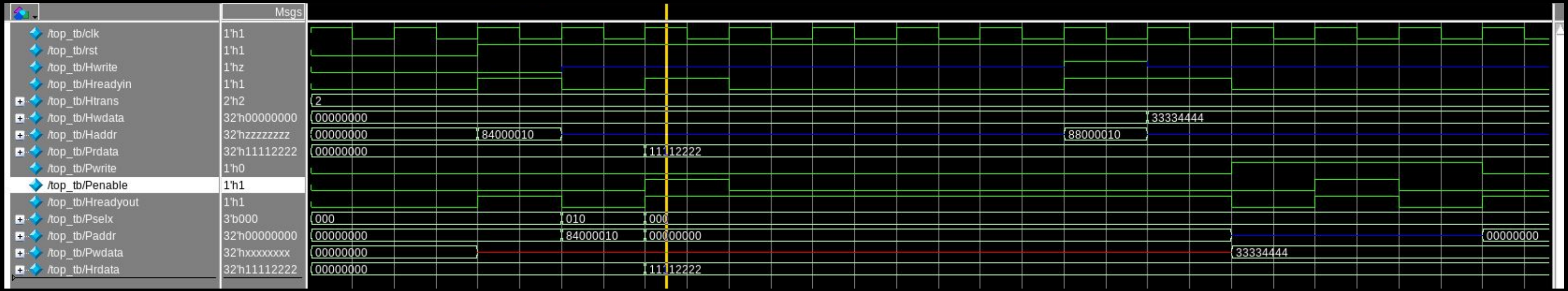

Msgs
/AHB_slave_interface_tb/clk -No Data-
/AHB_slave_interface_tb/rst -No Data-
/AHB_slave_interface_tb/Hwrite -No Data-
/AHB_slave_interface_tb/Hread... -No Data-
/AHB_slave_interface_tb/valid -No Data-
/AHB_slave_interface_tb/Hwrit... -No Data-
/AHB_slave_interface_tb/Htrans -No Data- 00 10 11 10
/AHB_slave_interface_tb/Haddr -No Data- 00000000 80000010 84000020 90000000 80000000 80000004 80000008 8000000c 80000000
/AHB_slave_interface_tb/Hwdata -No Data- 00000000 12345678 87654321
/AHB_slave_interface_tb/Prdata -No Data- 00000000 abcdef01 11223344
/AHB_slave_interface_tb/Haddr1 -No Data- 00000000 80000010 84000020 90000000 00000000 80000000 80000004 80000008 8000000c 80000000
/AHB_slave_interface_tb/Haddr2 -No Data- 00000000 80000010 84000020 00000000 80000000 80000004 80000008 8000000c
/AHB_slave_interface_tb/Hwda... -No Data- 00000000 12345678 87654321 00000000 87654321
/AHB_slave_interface_tb/Hwda... -No Data- 00000000 12345678 87654321 00000000 87654321
/AHB_slave_interface_tb/Hrdata -No Data- 00000000 abcdef01 11223344
/AHB_slave_interface_tb/temps... -No Data- 000 001 010 000 001
/AHB_slave_interface_tb/Hresp -No Data- 00



```
# Starting Read-Write-Read-Write Test
# Read-Write-Read-Write Test Completed
# Starting Invalid Address Test
# Invalid Address Test Passed
# Starting Reset Test
# Reset Test Passed
# Starting Burst Test
# Burst Test Completed
# ** Note: $stop    : AHB_Slave_Interface_tb.v(128)
#    Time: 125 ns  Iteration: 0  Instance: /AHB_slave_interface_tb
```

- Read-Write-Read-Write
- Invalid Address
- Reset
- Burst Write
- Expected outputs

Stimulation - TOP



	Msgs
/top_tb/clk	1'h1
/top_tb/rst	1'h1
/top_tb/Hwrite	1'hz
/top_tb/Hreadyin	1'h1
/top_tb/Htrans	2'h2
/top_tb/Hwdata	32'h00000000
/top_tb/Haddr	32'hzzzzzzzz
/top_tb/Prdata	32'h11112222
/top_tb/Pwrite	1'h0
/top_tb/Penable	1'h1
/top_tb/Hreadyout	1'h1
/top_tb/Pselx	3'b000
/top_tb/Paddr	32'h00000000
/top_tb/Pwdata	32'hxxxxxxxx
/top_tb/Hrdata	32'h11112222

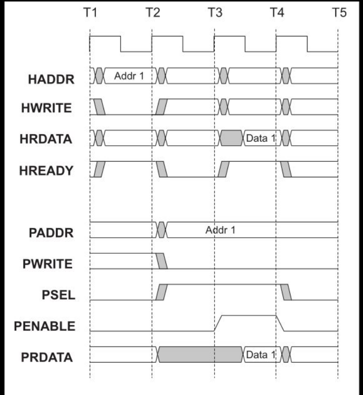


Figure 5-9 Read transfer to AHB

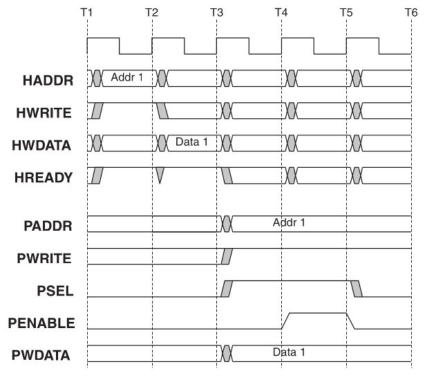
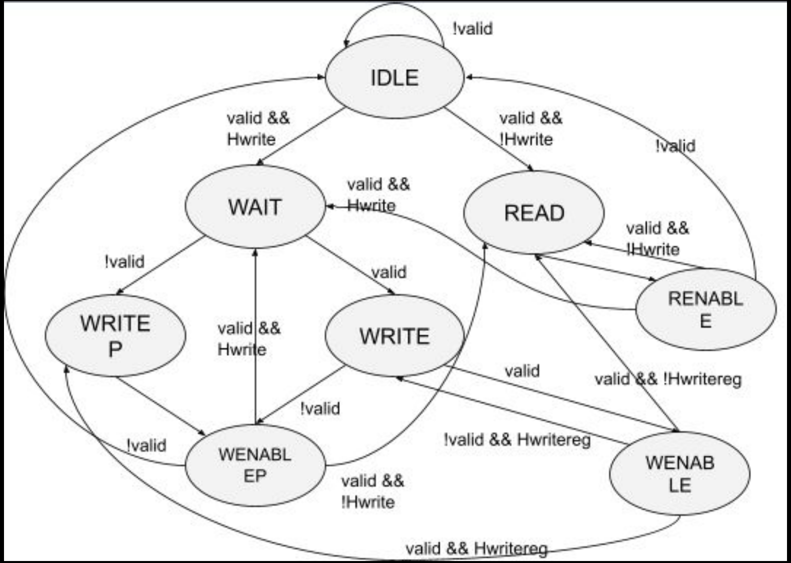
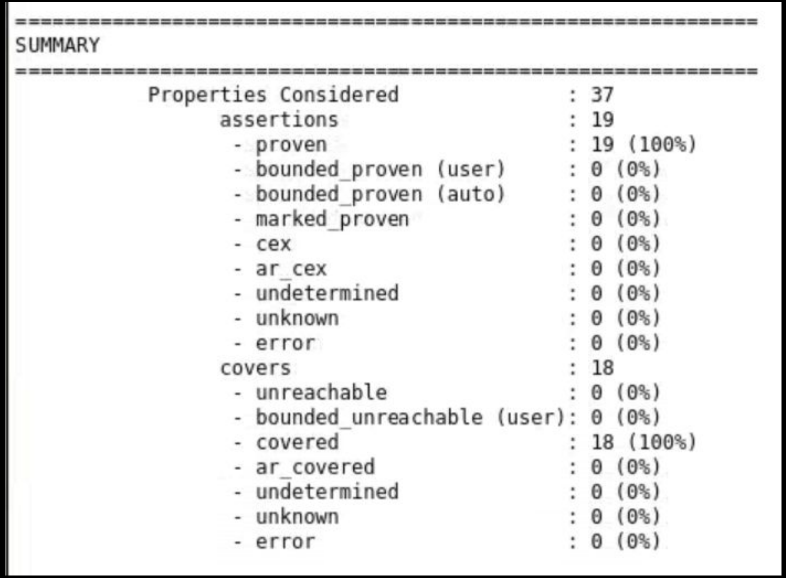


Figure 5-11 Write transfer from AHB

- Single read & write
- Expected outputs except Pslex

SVA - FSM





```
=================================================================
SUMMARY
=================================================================
          Properties Considered               : 37
                assertions                    : 19
                 - proven                     : 19 (100%)
                 - bounded_proven (user)      : 0 (0%)
                 - bounded_proven (auto)      : 0 (0%)
                 - marked_proven              : 0 (0%)
                 - cex                        : 0 (0%)
                 - ar_cex                     : 0 (0%)
                 - undetermined               : 0 (0%)
                 - unknown                    : 0 (0%)
                 - error                      : 0 (0%)
                covers                        : 18
                 - unreachable                : 0 (0%)
                 - bounded_unreachable (user): 0 (0%)
                 - covered                    : 18 (100%)
                 - ar_covered                 : 0 (0%)
                 - undetermined               : 0 (0%)
                 - unknown                    : 0 (0%)
                 - error                      : 0 (0%)
```

- States: IDLE, WAIT, READ, WRITE, WRITEP, WENABLE, WENABLEP, RENALE
- Transitions based on inputs (valid, Hwrite, Hwritereg)

Property Verification

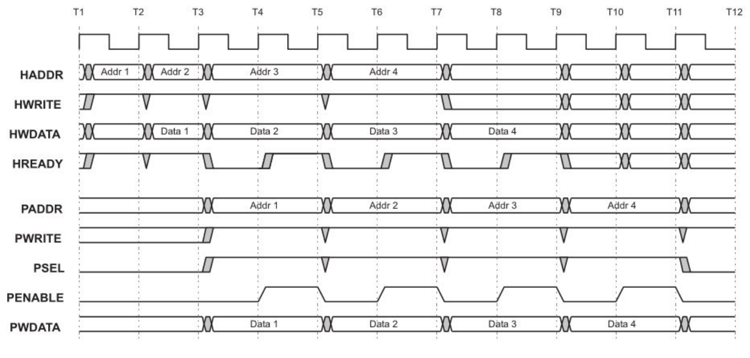


Figure 5-12 Burst of write transfers

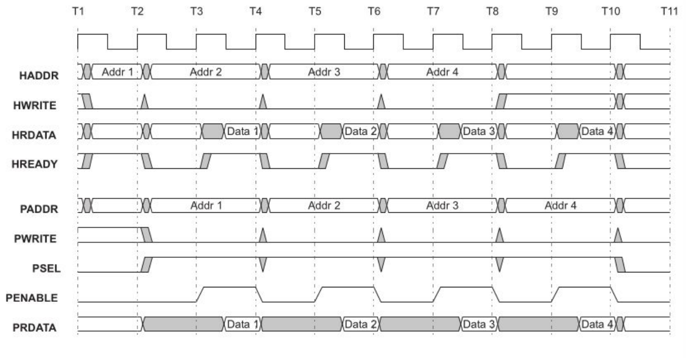


Figure 5-10 Burst of read transfers

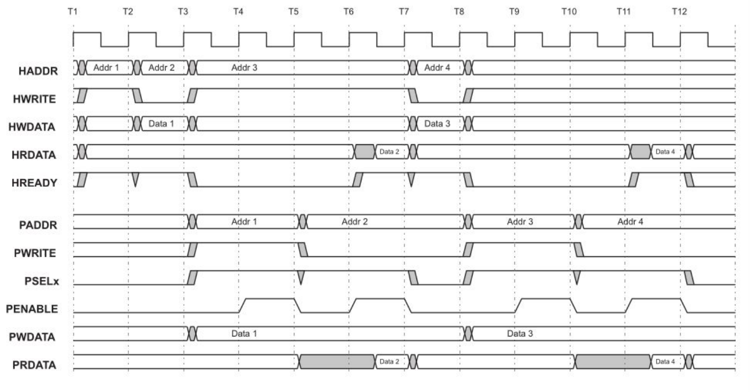


Figure 5-13 Back to back transfers

Five Scenarios:

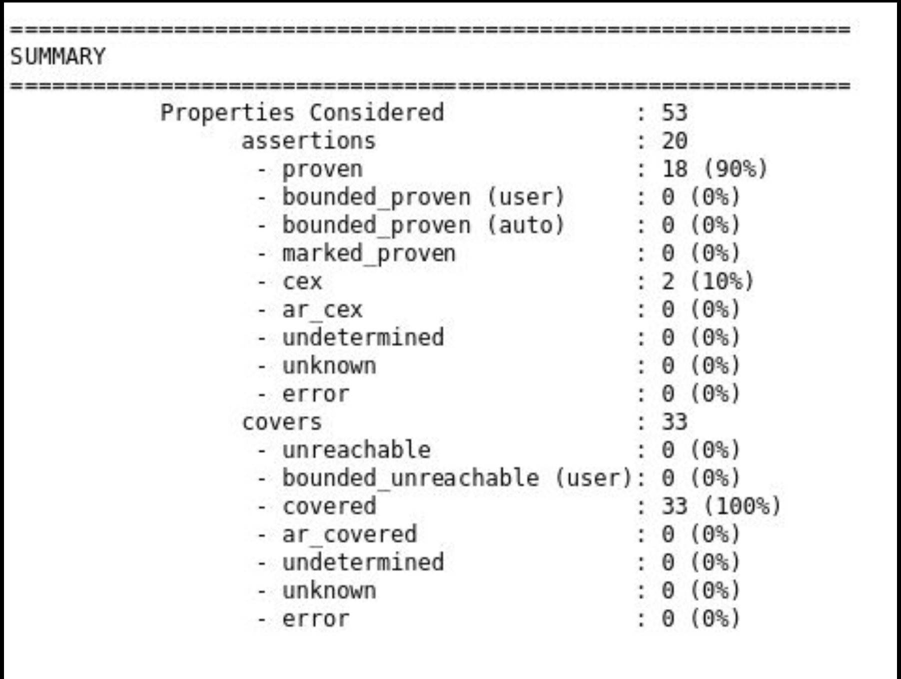
- Single Write
- Single Read
- Burst write
- Burst read
- Back to back

Property Verification

- **Input signal timing constraints**
  Hwrite
  Hreadyin
  Haddr
  Hwdata
  Prdata

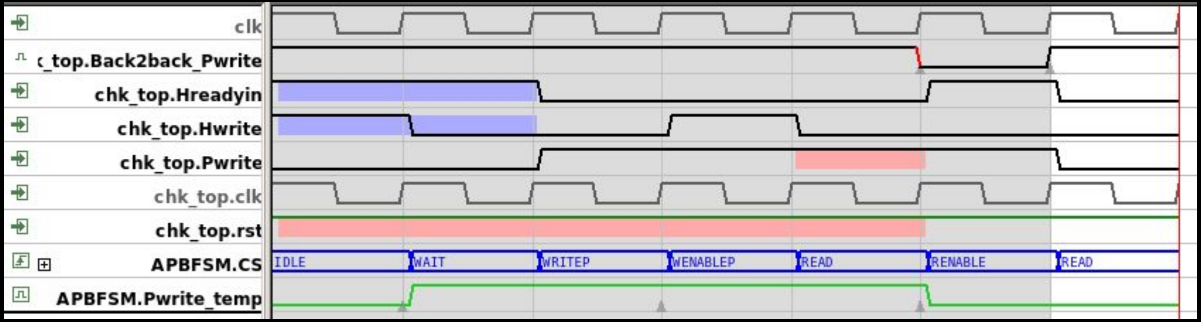
- **Output check:**
  Pwrite
  Paddr
  Penable
  Pwdata
  Hrdata
  Pselx

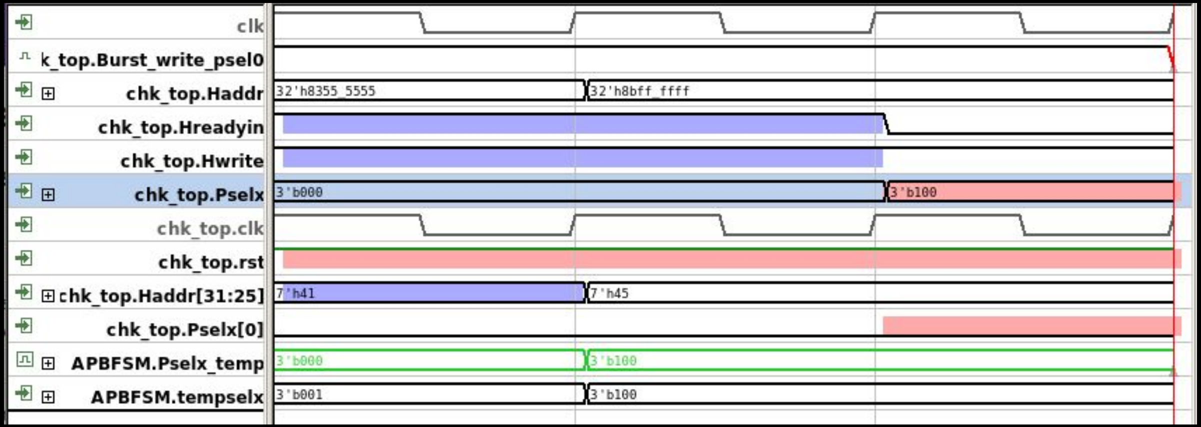
- **Assumptions:**
  -valid input address
  -transfer type
  -burst read constraint
  -burst write constraint
  -back to back constraint



```
==============================================================
SUMMARY
==============================================================
           Properties Considered              : 53
                 assertions                   : 20
                  - proven                    : 18 (90%)
                  - bounded_proven (user)     : 0 (0%)
                  - bounded_proven (auto)     : 0 (0%)
                  - marked_proven             : 0 (0%)
                  - cex                       : 2 (10%)
                  - ar_cex                    : 0 (0%)
                  - undetermined              : 0 (0%)
                  - unknown                   : 0 (0%)
                  - error                     : 0 (0%)
                 covers                       : 33
                  - unreachable               : 0 (0%)
                  - bounded_unreachable (user): 0 (0%)
                  - covered                   : 33 (100%)
                  - ar_covered                : 0 (0%)
                  - undetermined              : 0 (0%)
                  - unknown                   : 0 (0%)
                  - error                     : 0 (0%)
```

SVA - TOP



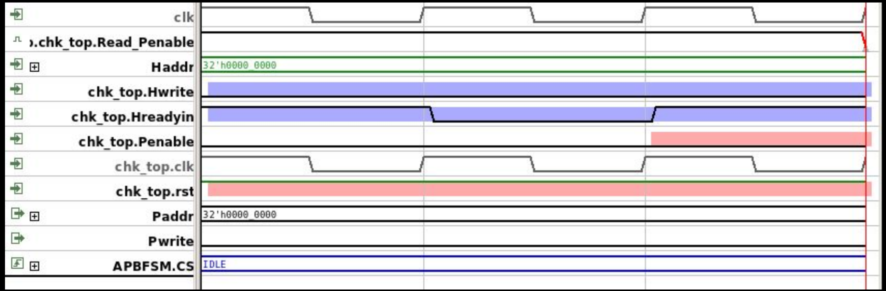


All passed except:

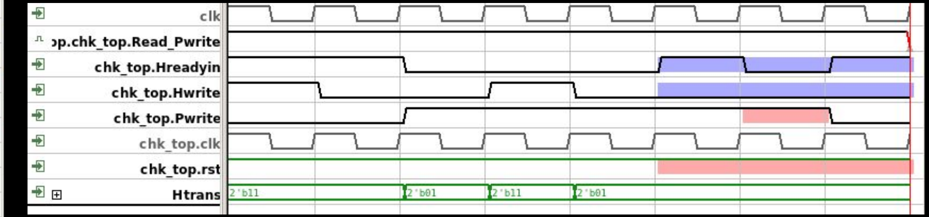
- **Back2back_Pwrite**:
  - Sequence: write ⟶ read ⟶ invalid ⟶ invalid ⟶ invalid
  - First and second cycles: back-to-back transfers
  - Error: Pwrite incorrectly high at the fifth cycle
  - Expected: Pwrite should match Hwrite from the second cycle (low)
  - Caused by insufficient RTL design

- **Brust_write_psel0**:
  - Error: Pselx should be 3’b001
  - 3’b100 should occur at the fifth cycle
  - Pselx does not transfer correctly in the original RTL FSM code

SVA - TOP Counterexample Analysis



read_Penable



read_Pwrite

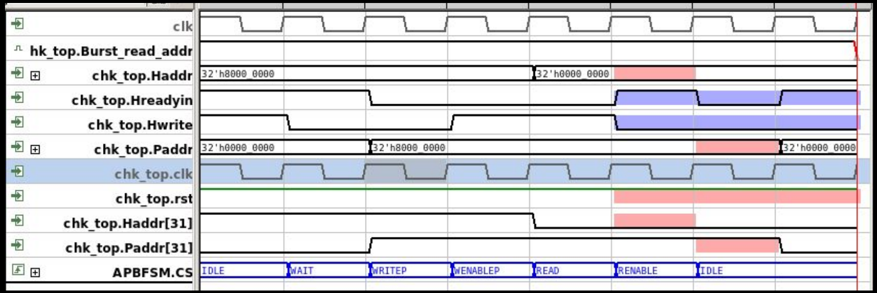
Removing valid address range assumption:

- State machine remains in the IDLE state due to invalid address

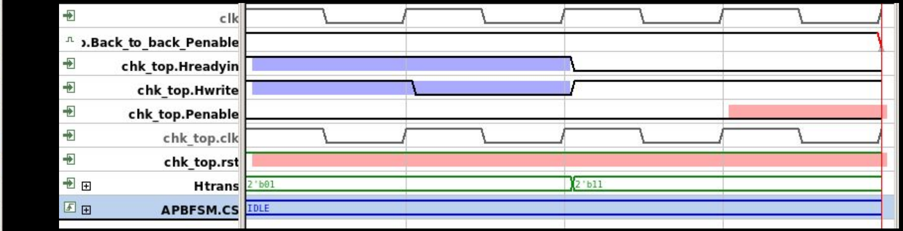
Removing transfer type assumption:

- Htrans in Busy mode causes the state to remain in the IDLE state

Burst_read_addr



Back_to_back_Penable



Stimulation vs SVA

Stimulation:

- Verified single write/read and identified the Pselx error
- Unable to fully check burst read/write scenarios and back-to-back transfers

SVA:

- More effective in verifying burst read/write and complex state transitions
- Captured issues like incorrect Pwrite behavior during back-to-back transfers, which were missed in stimulation

Conclusion & Future Work

Conclusion:

- Formal verification of the AHB-to-APB bridge confirmed correct data transfer.
- Identified and addressed issues in state transitions and address handling in the RTL code.

Future Work:

- Fix identified errors in the RTL code.
- Expand verification to cover more scenarios and edge cases.
- Optimize tool integration and extend verification to other AMBA components.