Homework2

21307099 liyingjun

P1.

a. Each write buffer entry should be as wide as the L2 cache write data bus, which is 16 B.

b. L2 cache can perform a write to an independent cache address every 4 processor cycles. If all other instructions can be issued in parallel with the stores, then theoretically, 4 different write operations could be executed in every 4 processor cycles.

c. In the case of possible L1 misses, systems with blocking caches would require more write buffer entries to store data that is waiting to be written to the L2 cache, as the processor would stall until the data returns on an L1 miss. Non-blocking cache systems might not require additional write buffer entries as they can continue to execute other instructions.

P2. The formula for Average Memory Access Time (AMAT) is:

$$AMAT = \text{Hit Time} + (\text{Miss Rate} \times \text{Miss Penalty}) \tag{1}$$

The average Memory Access Time for Configuration 1 (32KB L1; 8MB L2; off-chip memory) is 2.44 cycles.
The AMAT for Configuration 2 (32KB L1; 2MB L2; 8MB L3; off-chip memory) is 1.60 cycles.
The AMAT for Configuration 3 (32KB L1; 512KB L2; 2MB L3; 8MB L4; off-chip memory) is 1.39 cycles.

Observations:

- When the cache hierarchy is too shallow, as in Configuration 1, the AMAT is relatively high. This is because fewer cache levels result in more accesses needing to be fetched from off-chip memory, increasing the average access time.

- When the cache hierarchy is too deep, as in Configuration 3, although the AMAT is the lowest, adding more cache levels could introduce other issues like hardware complexity and power consumption.

P3. The processor with the branch-target buffer is about 12.75% faster than the processor with a fixed two-cycle branch penalty.

1. Processor with Branch-Target Buffer
   Hit rate = 0.9, Accuracy = 0.8, Branch frequency = 0.15
   Misprediction penalty = 4, Buffer miss penalty = 3
   CPI Impact = $(1-0.15)\times 0+0.15\times[(0.9\times 0.8\times 0+0.9\times 0.2\times 4)+0.1\times 3]$

2. Processor with Fixed Two-Cycle Branch Penalty
   Branch penalty = 2, Branch frequency = 0.15
   CPI Impact = 0.15×2

Target buffer shows a speed improvement of approximately 12.75%.

P4.

a. When an unconditional branch is found in the buffer, the penalty in clock cycles is 0 as the target instruction for the unconditional branch is stored in the buffer.

b. Average Penalty = $0.9 \times 0 + 0.1 \times 2 = 0.2$ clock cycles
   Improvement = $\frac{2-0.2}{2} = 1.8$ clock cycles

P5.

a. The desktop system has 2 GB of DRAM, and each DRAM chip is 1 Gb. Therefore, $2 \times 1024 = 2048$ Gb DRAM chips are needed. Since each DRAM connects to each DIMM data pin, each DRAM chip must have 64 data I/Os.

b. The DIMM is 64 bits wide (8 bytes). To support 32B (32 bytes) L2 cache blocks, a burst length of $\frac{32}{8} = 4$ is required.

c. The DDR2-533 DIMM has a data rate of 533 MT/s. Since each transfer is 64 bits (8 bytes), the peak bandwidth is $533 \times 10^6 \times 8 = 4.264$ GB/s bytes/sec.