# VLSI Testing and Design for Testability

# Assignment0

B103526 中央電機黃聖倫

I used the existing function **“SetupIO_ID()”** to complete this assignment.

I added some data members to store information about inputs, outputs, and gate data.

For **flip-flops**, I used the number of **PPIs** to calculate how many flip-flops exist, and for other gates, I used the existing enumeration for the calculation.

The most challenging part was calculating **the total number of signal nets**. However, I found that the total number of signal nets is **the sum of branch nets, stem nets, and nets with only one fanout**.

To calculate **the average number of fanouts per gate**, I also **modified the “SetupIO_ID” function and added some data members** to the circuit class in **“circuit.h”** to complete this part.

Additionally, I placed the “circuits” and “podem” files in **separate directories**, so the command format would be something like ./atpg -ass0 ../circuits/iscas85/c6288.bench, for example.

```
[s110305504@cad podem]$ ./atpg -ass0 /home/Student113/s110305504/VLSI_Testing/Assignment0/circuits/iscas85/c6288.bench
Start parsing input file
Finish reading circuit file
Number of inputs: 32
Number of outputs: 32
Total number of gates including inverter, or, nor, and, nand: 4768
Total number of gates inverter: 2384
Total number of gates or: 0
Total number of gates nor: 0
Total number of gates and: 2384
Total number of gates nand: 0
Total number of Number of flip-flops: 0
Total number of signal nets: 8688
Number of branch nets: 3856
Number of stem nets: 1472
Average number of fanouts of all gate (including inverter, or, nor, and, nand): 1.39597
total CPU time = 0.02
```