VLSI Testing and Design for Testability

Assignment 5

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a)指令:

generate patterns for a circuit by running built-in ATPG:

./atpg -output [output_pattern_file] [絕對路徑+circuit_name]

使用 checkpoint 產生的 fault

./atpg -check-point -output [output_pattern_file] <絕對路徑+ [circuit_name]>

run fault simulation to obtain fault coverages respectively for original and checlpoint-based ATPG

./atpg -fsim -input [input_pattern_file] <絕對路徑+ [circuit_name]>

Result:

表一、the fault coverage for built-in and checkpoint-based ATPG//**()內為 pattern 數量**

Testbench	original	checkpoint
c17.bench	100%(8)	100%(7)
c499.bench	96.99%(79)	96.99%(80)
c7552.bench	98.42%(361)	98.43%(342)

可從表一發現大多數情況 checkpoint 的 pattern 數會比較少

```
[s110305504@cad podem]$ ./atpg -fsim -input c17.atpg "/home/Student113/s110305504/VLSI_Testing/Assignment5/circuits/iscas85/c17.bench"
Start parsing input file
Finish reading circuit file
Generate stuck-at fault list
AllFaultList: 36
Run stuck-at fault simulation
---------------------------------------
Test pattern number = 8
---------------------------------------
Total fault number = 36
Detected fault number = 36
Undetected fault number = 0
---------------------------------------
Equivalent fault number = 36
Equivalent detected fault number = 36
Equivalent undetected fault number = 0
---------------------------------------
Fault Coverge = 100.00%
Equivalent FC = 100.00%
---------------------------------------
total CPU time = 0.00
```

圖一、c17.bench built-in test 結果

```
[s110305504@cad podem]$ ./atpg -fsim -input c499.atpg "/home/Student113/s110305504/VLSI_Testing/Assignment5/circuits/iscas85/c499.bench"
Start parsing input file
Finish reading circuit file
Generate stuck-at fault list
AllFaultList: 2390
Run stuck-at fault simulation
---------------------------------------
Test pattern number = 79
---------------------------------------
Total fault number = 2390
Detected fault number = 2318
Undetected fault number = 72
---------------------------------------
Equivalent fault number = 2390
Equivalent detected fault number = 2318
Equivalent undetected fault number = 72
---------------------------------------
Fault Coverge = 96.99%
Equivalent FC = 96.99%
---------------------------------------
total CPU time = 0.02
```

圖二、c499.bench built-in test 結果

```
[s110305504@cad podem]$ ./atpg -fsim -input c7552.atpg "/home/Student113/s110305504/VLSI_Testing/Assignment5/circuits/iscas85/c7552.bench"
Start parsing input file
Finish reading circuit file
Generate stuck-at fault list
AllFaultList: 19456
Run stuck-at fault simulation
---------------------------------------
Test pattern number = 361
---------------------------------------
Total fault number = 19456
Detected fault number = 19149
Undetected fault number = 307
---------------------------------------
Equivalent fault number = 19456
Equivalent detected fault number = 19149
Equivalent undetected fault number = 307
---------------------------------------
Fault Coverge = 98.42%
Equivalent FC = 98.42%
---------------------------------------
total CPU time = 0.29
```

圖三、c7552.bench built-in test 結果

```
[s110305504@cad podem]$ ./atpg -fsim -input c17_atpg "/home/Student113/s110305504/VLSI_Testing/Assignment5/circuits/iscas85/c17.bench"
Start parsing input file
Finish reading circuit file
Generate stuck-at fault list
AllFaultList: 36
Run stuck-at fault simulation
---------------------------------------
Test pattern number = 7
---------------------------------------
Total fault number = 36
Detected fault number = 36
Undetected fault number = 0
---------------------------------------
Equivalent fault number = 36
Equivalent detected fault number = 36
Equivalent undetected fault number = 0
---------------------------------------
Fault Coverge = 100.00%
Equivalent FC = 100.00%
---------------------------------------
total CPU time = 0.00
```

圖四、c17.bench checkpoint 結果

```
[s110305504@cad podem]$ ./atpg -fsim -input c499_atpg "/home/Student113/s110305504/VLSI_Testing/Assignment5/circuits/iscas85/c499.bench"
Start parsing input file
Finish reading circuit file
Generate stuck-at fault list
AllFaultList: 2390
Run stuck-at fault simulation
---------------------------------------
Test pattern number = 80
---------------------------------------
Total fault number = 2390
Detected fault number = 2318
Undetected fault number = 72
---------------------------------------
Equivalent fault number = 2390
Equivalent detected fault number = 2318
Equivalent undetected fault number = 72
---------------------------------------
Fault Coverge = 96.99%
Equivalent FC = 96.99%
---------------------------------------
total CPU time = 0.02
```

圖五、c499.bench checkpoint 結果

```
[s110305504@cad podem]$ ./atpg -fsim -input c7552_atpg "/home/Student113/s110305504/VLSI_Testing/Assignment5/circuits/iscas85/c7552.bench"
Start parsing input file
Finish reading circuit file
Generate stuck-at fault list
AllFaultList: 19456
Run stuck-at fault simulation
---------------------------------------
Test pattern number = 342
---------------------------------------
Total fault number = 19456
Detected fault number = 19151
Undetected fault number = 305
---------------------------------------
Equivalent fault number = 19456
Equivalent detected fault number = 19151
Equivalent undetected fault number = 305
---------------------------------------
Fault Coverge = 98.43%
Equivalent FC = 98.43%
---------------------------------------
total CPU time = 0.29
```

圖六、c7552.bench checkpoint 結果

b)

通過使用 Assignment2 中寫過產生 pattern 的 function 產出 one million random patterns。因為我每次作業都是從最原始的 Assignemt0 修改，所以我通過執行 Assignment2，將其產生隨機的檔案放入 podem 內來完成這個 part。

表二、不同 faults per pass 輸出結果(with unkown)

Circuit netlist	1	4	8	16	32	64	Fault coverage
c17.bench	0.56(s)	0.56(s)	0.56(s)	0.55(s)	0.52(s)	0.55(s)	100%
Speed-up	1.00	0.98	0.98	0.98	0.96	1.00	
c499.bench	22.63(s)	22.00(s)	21.54(s)	21.13(s)	20.67(s)	20.66(s)	96.99%
Speed-up	1.00	1.02	1.05	1.07	1.09	1.10	
c7552.bench	281.33 (s)	274.47 (s)	270.80 (s)	264.94 (s)	260.50 (s)	257.58 (s)	97.59%
Speed-up	1.00	1.02	1.04	1.06	1.08	1.09	

從上表可看出，即使不同 faults per pass 的數量，相同 CIRCUIT 會有相同 fault coverage。此外從較大的 case c499.bench 中可看出隨著 faults per pass 的數量增加，時間也會越來越少。

```
[s110305504@cad podem]$ ./atpg -fsim -input c17_1M.input "/home/Student113/s110305504/VLSI_Testing/Assignment5/circuits/iscas85/c17.bench"
Start parsing input file
Finish reading circuit file
Generate stuck-at fault list
AllFaultList: 36
Run stuck-at fault simulation
---------------------------------------
Test pattern number = 1000000
---------------------------------------
Total fault number = 36
Detected fault number = 36
Undetected fault number = 0
---------------------------------------
Equivalent fault number = 36
Equivalent detected fault number = 36
Equivalent undetected fault number = 0
---------------------------------------
Fault Coverge = 100.00%
Equivalent FC = 100.00%
---------------------------------------
total CPU time = 0.56
```

圖七、c17.bench 1 faults per pass 結果

```
[s110305504@cad podem]$ ./atpg -fsim -input c17_1M.input "/home/Student113/s110305504/VLSI_Testing/Assignment5/circuits/iscas85/c17.bench"
Start parsing input file
Finish reading circuit file
Generate stuck-at fault list
AllFaultList: 36
Run stuck-at fault simulation
---------------------------------------
Test pattern number = 1000000
---------------------------------------
Total fault number = 36
Detected fault number = 36
Undetected fault number = 0
---------------------------------------
Equivalent fault number = 36
Equivalent detected fault number = 36
Equivalent undetected fault number = 0
---------------------------------------
Fault Coverge = 100.00%
Equivalent FC = 100.00%
---------------------------------------
total CPU time = 0.56
```

圖八、c17.bench 4 faults per pass 結果

```
[s110305504@cad podem]$ ./atpg -fsim -input c17_1M.input "/home/Student113/s110305504/VLSI_Testing/Assignment5/circuits/iscas85/c17.bench"
Start parsing input file
Finish reading circuit file
Generate stuck-at fault list
AllFaultList: 36
Run stuck-at fault simulation
---------------------------------------
Test pattern number = 1000000
---------------------------------------
Total fault number = 36
Detected fault number = 36
Undetected fault number = 0
---------------------------------------
Equivalent fault number = 36
Equivalent detected fault number = 36
Equivalent undetected fault number = 0
---------------------------------------
Fault Coverge = 100.00%
Equivalent FC = 100.00%
---------------------------------------
total CPU time = 0.56
```

圖九、c17.bench 8 faults per pass 結果

```
[s110305504@cad podem]$ ./atpg -fsim -input c17_1M.input "/home/Student113/s110305504/VLSI_Testing/Assignment5/circuits/iscas85/c17.bench"
Start parsing input file
Finish reading circuit file
Generate stuck-at fault list
AllFaultList: 36
Run stuck-at fault simulation
---------------------------------------
Test pattern number = 1000000
---------------------------------------
Total fault number = 36
Detected fault number = 36
Undetected fault number = 0
---------------------------------------
Equivalent fault number = 36
Equivalent detected fault number = 36
Equivalent undetected fault number = 0
---------------------------------------
Fault Coverge = 100.00%
Equivalent FC = 100.00%
---------------------------------------
total CPU time = 0.55
```

圖十、c17.bench 16 faults per pass 結果

```
[s110305504@cad podem]$ ./atpg -fsim -input c17_1M.input "/home/Student113/s110305504/VLSI_Testing/Assignment5/circuits/iscas85/c17.bench
Start parsing input file
Finish reading circuit file
Generate stuck-at fault list
AllFaultList: 36
Run stuck-at fault simulation
---------------------------------------
Test pattern number = 1000000
---------------------------------------
Total fault number = 36
Detected fault number = 36
Undetected fault number = 0
---------------------------------------
Equivalent fault number = 36
Equivalent detected fault number = 36
Equivalent undetected fault number = 0
---------------------------------------
Fault Coverge = 100.00%
Equivalent FC = 100.00%
---------------------------------------
total CPU time = 0.52
```

圖十一、c17.bench 32 faults per pass 結果

```
[s110305504@cad podem]$ ./atpg -fsim -input c17_1M.input "/home/Student113/s110305504/VLSI_Testing/Assignment5/circuits/iscas85/c17.bench"
Start parsing input file
Finish reading circuit file
Generate stuck-at fault list
AllFaultList: 36
Run stuck-at fault simulation
---------------------------------------
Test pattern number = 1000000
---------------------------------------
Total fault number = 36
Detected fault number = 36
Undetected fault number = 0
---------------------------------------
Equivalent fault number = 36
Equivalent detected fault number = 36
Equivalent undetected fault number = 0
---------------------------------------
Fault Coverge = 100.00%
Equivalent FC = 100.00%
---------------------------------------
total CPU time = 0.55
```

圖十二、c17.bench 64 faults per pass 結果

```
[s110305504@cad podem]$ ./atpg -fsim -input c499_1M.input "/home/Student113/s110305504/VLSI_Testing/Assignment5/circuits/iscas85/c499.bench"
Start parsing input file
Finish reading circuit file
Generate stuck-at fault list
AllFaultList: 2390
Run stuck-at fault simulation
---------------------------------------
Test pattern number = 1000000
---------------------------------------
Total fault number = 2390
Detected fault number = 2318
Undetected fault number = 72
---------------------------------------
Equivalent fault number = 2390
Equivalent detected fault number = 2318
Equivalent undetected fault number = 72
---------------------------------------
Fault Coverge = 96.99%
Equivalent FC = 96.99%
---------------------------------------
total CPU time = 22.63
```

圖十四、c499.bench 1 faults per pass 結果

```
[s110305504@cad podem]$ ./atpg -fsim -input c499_1M.input "/home/Student113/s110305504/VLSI_Testing/Assignment5/circuits/iscas85/c499.bench"
Start parsing input file
Finish reading circuit file
Generate stuck-at fault list
AllFaultList: 2390
Run stuck-at fault simulation
---------------------------------------
Test pattern number = 1000000
---------------------------------------
Total fault number = 2390
Detected fault number = 2318
Undetected fault number = 72
---------------------------------------
Equivalent fault number = 2390
Equivalent detected fault number = 2318
Equivalent undetected fault number = 72
---------------------------------------
Fault Coverge = 96.99%
Equivalent FC = 96.99%
---------------------------------------
total CPU time = 22.00
```

圖十四、c499.bench 4 faults per pass 結果

```
[s110305504@cad podem]$ ./atpg -fsim -input c499_1M.input "/home/Student113/s110305504/VLSI_Testing/Assignment5/circuits/iscas85/c499.bench"
Start parsing input file
Finish reading circuit file
Generate stuck-at fault list
AllFaultList: 2390
Run stuck-at fault simulation
---------------------------------------
Test pattern number = 1000000
---------------------------------------
Total fault number = 2390
Detected fault number = 2318
Undetected fault number = 72
---------------------------------------
Equivalent fault number = 2390
Equivalent detected fault number = 2318
Equivalent undetected fault number = 72
---------------------------------------
Fault Coverge = 96.99%
Equivalent FC = 96.99%
---------------------------------------
total CPU time = 21.54
```

圖十五、c499.bench 8 faults per pass 結果

```
[s110305504@cad podem]$ ./atpg -fsim -input c499_1M.input "/home/Student113/s110305504/VLSI_Testing/Assignment5/circuits/iscas85/c499.bench"
Start parsing input file
Finish reading circuit file
Generate stuck-at fault list
AllFaultList: 2390
Run stuck-at fault simulation
---------------------------------------
Test pattern number = 1000000
---------------------------------------
Total fault number = 2390
Detected fault number = 2318
Undetected fault number = 72
---------------------------------------
Equivalent fault number = 2390
Equivalent detected fault number = 2318
Equivalent undetected fault number = 72
---------------------------------------
Fault Coverge = 96.99%
Equivalent FC = 96.99%
---------------------------------------
total CPU time = 21.13
```

圖十六、c499.bench 16 faults per pass 結果

```
[s110305504@cad podem]$ ./atpg -fsim -input c499_1M.input "/home/Student113/s110305504/VLSI_Testing/Assignment5/circuits/iscas85/c499.bench"
Start parsing input file
Finish reading circuit file
Generate stuck-at fault list
AllFaultList: 2390
Run stuck-at fault simulation
---------------------------------------
Test pattern number = 1000000
---------------------------------------
Total fault number = 2390
Detected fault number = 2318
Undetected fault number = 72
---------------------------------------
Equivalent fault number = 2390
Equivalent detected fault number = 2318
Equivalent undetected fault number = 72
---------------------------------------
Fault Coverge = 96.99%
Equivalent FC = 96.99%
---------------------------------------
total CPU time = 20.67
```

圖十七、c499.bench 32 faults per pass 結果

```
[s110305504@cad podem]$ ./atpg -fsim -input c499_1M.input "/home/Student113/s110305504/VLSI_Testing/Assignment5/circuits/iscas85/c499.bench"
Start parsing input file
Finish reading circuit file
Generate stuck-at fault list
AllFaultList: 2390
Run stuck-at fault simulation
---------------------------------------
Test pattern number = 1000000
---------------------------------------
Total fault number = 2390
Detected fault number = 2318
Undetected fault number = 72
---------------------------------------
Equivalent fault number = 2390
Equivalent detected fault number = 2318
Equivalent undetected fault number = 72
---------------------------------------
Fault Coverge = 96.99%
Equivalent FC = 96.99%
---------------------------------------
total CPU time = 20.66
```

圖十八、c499.bench 64 faults per pass 結果

```
[s110305504@cad podem]$ ./atpg -fsim -input c7552_1M.input "/home/Student113/s110305504/VLSI_Testing/Assignment5/circuits/iscas85/c7552.bench"
Start parsing input file
Finish reading circuit file
Generate stuck-at fault list
AllFaultList: 19456
Run stuck-at fault simulation
---------------------------------------
Test pattern number = 1000000
---------------------------------------
Total fault number = 19456
Detected fault number = 18987
Undetected fault number = 469
---------------------------------------
Equivalent fault number = 19456
Equivalent detected fault number = 18987
Equivalent undetected fault number = 469
---------------------------------------
Fault Coverge = 97.59%
Equivalent FC = 97.59%
---------------------------------------
total CPU time = 281.33
```

圖十九、c7552.bench 1 faults per pass 結果

```
[s110305504@cad podem]$ ./atpg -fsim -input c7552_1M.input "/home/Student113/s110305504/VLSI_Testing/Assignment5/circuits/iscas85/c7552.bench"
Start parsing input file
Finish reading circuit file
Generate stuck-at fault list
AllFaultList: 19456
Run stuck-at fault simulation
---------------------------------------
Test pattern number = 1000000
---------------------------------------
Total fault number = 19456
Detected fault number = 18987
Undetected fault number = 469
---------------------------------------
Equivalent fault number = 19456
Equivalent detected fault number = 18987
Equivalent undetected fault number = 469
---------------------------------------
Fault Coverge = 97.59%
Equivalent FC = 97.59%
---------------------------------------
total CPU time = 274.47
```

圖二十、c7552.bench 4 faults per pass 結果

```
[s110305504@cad podem]$ ./atpg -fsim -input c7552_1M.input "/home/Student113/s110305504/VLSI_Testing/Assignment5/circuits/iscas85/c7552.bench"
Start parsing input file
Finish reading circuit file
Generate stuck-at fault list
AllFaultList: 19456
Run stuck-at fault simulation
---------------------------------------
Test pattern number = 1000000
---------------------------------------
Total fault number = 19456
Detected fault number = 18987
Undetected fault number = 469
---------------------------------------
Equivalent fault number = 19456
Equivalent detected fault number = 18987
Equivalent undetected fault number = 469
---------------------------------------
Fault Coverge = 97.59%
Equivalent FC = 97.59%
---------------------------------------
total CPU time = 270.80
```

圖二十一、c7552.bench 8 faults per pass 結果

```
[s110305504@cad podem]$ ./atpg -fsim -input c7552_1M.input "/home/Student113/s110305504/VLSI_Testing/Assignment5/circuits/iscas85/c7552.bench"
Start parsing input file
Finish reading circuit file
Generate stuck-at fault list
AllFaultList: 19456
Run stuck-at fault simulation
---------------------------------------
Test pattern number = 1000000
---------------------------------------
Total fault number = 19456
Detected fault number = 18987
Undetected fault number = 469
---------------------------------------
Equivalent fault number = 19456
Equivalent detected fault number = 18987
Equivalent undetected fault number = 469
---------------------------------------
Fault Coverge = 97.59%
Equivalent FC = 97.59%
---------------------------------------
total CPU time = 264.94
```

圖二十二、c7552.bench 16 faults per pass 結果

```
[s110305504@cad podem]$ ./atpg -fsim -input c7552_1M.input "/home/Student113/s110305504/VLSI_Testing/Assignment5/circuits/iscas85/c7552.bench"
Start parsing input file
Finish reading circuit file
Generate stuck-at fault list
AllFaultList: 19456
Run stuck-at fault simulation
---------------------------------------
Test pattern number = 1000000
---------------------------------------
Total fault number = 19456
Detected fault number = 18987
Undetected fault number = 469
---------------------------------------
Equivalent fault number = 19456
Equivalent detected fault number = 18987
Equivalent undetected fault number = 469
---------------------------------------
Fault Coverge = 97.59%
Equivalent FC = 97.59%
---------------------------------------
total CPU time = 260.50
```

圖二十三、c7552.bench 32 faults per pass 結果

```
[s110305504@cad podem]$ ./atpg -fsim -input c7552_1M.input "/home/Student113/s110305504/VLSI_Testing/Assignment5/circuits/iscas85/c7552.bench"
Start parsing input file
Finish reading circuit file
Generate stuck-at fault list
AllFaultList: 19456
Run stuck-at fault simulation
---------------------------------------
Test pattern number = 1000000
---------------------------------------
Total fault number = 19456
Detected fault number = 18987
Undetected fault number = 469
---------------------------------------
Equivalent fault number = 19456
Equivalent detected fault number = 18987
Equivalent undetected fault number = 469
---------------------------------------
Fault Coverge = 97.59%
Equivalent FC = 97.59%
---------------------------------------
total CPU time = 257.58
```

圖二十四、c7552.bench 64 faults per pass 結果

c)指令: ./atpg -bridging_fsim -input [input_pattern_file] [絕對路徑+circuit_name]

```
void CIRCUIT::ParellelBridgingFault()
{
    std::vector<std::list<GATE*> > LevelQueue(MaxLevel + 1);
    for (unsigned i = 0; i < No_Gate(); i++) {
        GATE* gptr = Gate(i);
        if(gptr->GetFunction() == G_PO) continue;
        unsigned level = gptr->GetLevel();
        LevelQueue[level].push_back(gptr);
    }
    GATE* n0, * n1;
    for (unsigned i = 0; i <= MaxLevel; i++) {
        while (LevelQueue[i].size() >= 2) {
            n0 = LevelQueue[i].front();
            LevelQueue[i].pop_front();
            n1 = LevelQueue[i].front();
            BFlist.push_back(new BridgingFAULT(n0, n1, AND));
            BFlist.push_back(new BridgingFAULT(n0, n1, OR));
        }
    }
    UBFlist = BFlist;
}
```

圖二十五、ParellelBridgeFault() function

使用 assignment 4 已寫好的功能加入 and bridging 和 or bridging。

之後仿照 FaultSimVectors()寫出 BFaultSimVectors()用來計算在處理每次 PATTERN 時有找出多少 FAULT。

```
// fault simulation test patterns
void CIRCUIT::BFaultSimVectors()
{
    cout << "Run bridging fault simulation" << endl;
    unsigned pattern_num(0);
    if(!Pattern.eof()){ // Readin the first vector
        while(!Pattern.eof()){
            ++pattern_num;
            Pattern.ReadNextPattern();
            //fault-free simulation
            SchedulePI();
            LogicSim();
            int a=UBFlist.size();
            //single pattern parallel fault simulation
            BFaultSim();
            int b=UBFlist.size();
            cout << "Found fault number :"<< a-b << endl;

        }
    }

    //compute fault coverage
    unsigned total_num(0);
    unsigned undetected_num(0), detected_num(0);
    unsigned eqv_undetected_num(0), eqv_detected_num(0);
    BridgingFAULT* fptr;
    list<BridgingFAULT*>::iterator fite;
    for (fite = BFlist.begin();fite!=BFlist.end();++fite) {
        fptr = *fite;
        switch (fptr->GetStatus()) {
            case DETECTED:
                ++eqv_detected_num;
                detected_num += fptr->GetEqvFaultNum();
                break;
            default:
                ++eqv_undetected_num;
                undetected_num += fptr->GetEqvFaultNum();
                break;
        }
```

圖二十六、BFaultSimVectors() function

之後通過修改 FAULTSIM 寫出 BFaultSim()來判斷 BRIDGING。

因為 BRIDGING 只有當兩個線的 VALUE 不同時，才會產生 BRIDGING，所以通過此判斷可以先將一些 CASE 刪掉。

```
for (fite = UBFlist.begin();fite!=UBFlist.end();++fite) {
    fptr = *fite;
    //skip redundant and detected faults
    if (fptr->GetStatus() == REDUNDANT || fptr->GetStatus() == DETECTED) { continue; }
    //the fault is not active (when the fault value )
    if (fptr->Getn1()->GetValue() ==  fptr->Getn0()->GetValue()) { continue; }
    //the fault can be directly seen
    gptr = fptr->Getn0();
    gptr2 = fptr->Getn1();

    if ((gptr->GetFlag(OUTPUT) && fptr->Getn0()->GetFunction() == G_PO) || (gptr2->GetFlag(OUTPUT) && (fptr->Getn1()->GetFunction() == G_PO))) {

        fptr->SetStatus(DETECTED);
        continue;
    }
```

圖二十七、BFaultSim () function 無產生 bridging 部分通過 continue 忽略

對於 OR-bridging fault, 對 net assign 1; 對 AND-bridging 對 net assign 0。

```
//inject faulty value to the gate
void CIRCUIT::BF_InjectFaultValue(GATEPTR gptr, unsigned idx, Bridging value)
{
    if (value == OR) {
        gptr->SetValue1(idx);
        gptr->SetValue2(idx);
    }
    else if (value == AND) {
        gptr->ResetValue1(idx);
        gptr->ResetValue2(idx);
    }
    gptr->SetFaultFlag(idx);
    return;
}
```

圖二十八、BF_InjectFaultValue() function

```
[s110305504@cad podem]$ ./atpg -bridging_fsim -input test.txt "/home/Student113/s110305504/VLSI_Testing/Assignment5/circuits/iscas85/c17.bench"
Start parsing input file
Finish reading circuit file
Run bridging fault simulation
Found fault number :1
Found fault number :2
Found fault number :9
Found fault number :1
Found fault number :0
Found fault number :0
Found fault number :3
Found fault number :0
---------------------------------------
Test pattern number = 8
---------------------------------------
Total fault number = 16
Detected fault number = 16
Undetected fault number = 0
---------------------------------------
Equivalent fault number = 16
Equivalent detected fault number = 16
Equivalent undetected fault number = 0
---------------------------------------
Fault Coverge = 100.00%
Equivalent FC = 100.00%
---------------------------------------
total CPU time = 0.00
```

圖二十九、c17.bench test.txt 結果

表三、c17.bench parallel fault simulator for the bridging fault 結果

INPUT	newly detected fault	undetected fault
(start)	-	16
00110	1	15
01111	2	13
10101	9	4
11011	1	3
11001	0	3
11010	0	3
10001	3	0
00010	0	0

Build:

make