VLSI Testing and Design for Testability

LAB1、LAB2 report

B103526 中央電機黃聖倫

LAB1-pre_norm

pre-norm	Area	Power	Fault count	Coverage (collapsed)	ATPG Run Time(s)	Pattern
Non-Scanned (-full seq atpg)	98495	254.0348μW	4019	98.15%	3434.06	269
Scanned	105522	265.322μW	4419	99.29%	0.54	151

LAB1-s38584_seq

s38584_seq	Area	Power	Fault count	Coverage (collapsed)	ATPG Run Time(s)	Pattern
Non-Scanned (-full seq atpg)	1081173	1.864mW	33951	21.45%	91452.71	10
Scanned	1222797	5.9445mW	42180	100%	0.79	133

LAB2-pre_norm

Flow	#Faults	Test Coverage	# Patterns	Run time(s)
DC+TMAX	6024	99.14%	151	0.54
TS	6218	99.80%	198	251.9
DC+TS	6024	99.86%	183	130.7