EEIE30069: VLSI Testing

Assignment #5 (Due: Nov. 11, 2024 23:59:99)

Last update: Oct. 27, 2024

Reading:

- Section 5.5 (Fault Simulation) and Sections 5.6 (Fault Sampling) (Bushnell and Agrawal) or Section 3.4 (Wang, Wu and Wen)
- Source code provided in homework #0
- Please put all results into a report and try to discuss the them
- Please compress the folder containing your source codes and reports to a file named by ASS5_<your-student-ID> and upload it to New E3
- The report should include
 - The algorithm or idea of your code
 - Several case results
 - Discuss your results
 - How to compile your code
 - Other information (optional)

Homework Description:

- 1. (150 pts) Fault Simulation
 - a. (20 pts) Generate patterns with PODEM, and then run PODEM using the patterns and the "fault simulation only" option to obtain fault coverages. Also, compare the fault coverage reported by the original PODEM program and the one based on checkpoint theorem (implemented in the assignment #4).
 - Note that you <u>don't</u> need to translate the results of checkpoint faults back to the original full fault list (without collapsing).
 - b. (30 pts) The fault simulator implemented in the package uses parallel fault simulation algorithm which simulates 16 faults per pass by default. Modify the fault simulation routine to simulate more/fewer faults per pass, say 4, 8, 32, 64, etc. Fault simulator should report the same fault coverage for all these cases.
 - Create a table comparing the CPU runtimes under different fault numbers. Show each speed-up with respect to the case of simulating just one fault per pass. Use random patterns (one million random patterns) for fault simulation in your comparison.
 - c. (100 pts) Please implement a parallel fault simulator for the bridging fault model described in <u>assignment #4</u>.

Grading:

- Correctness 90%
- Report 10%

Attention:

1. Use the command to generate patterns for a circuit by running built-in ATPG:

```
./atpg -output [output_pattern_file] [circuit_name]
```

2. You need to enroll a new command for 1.-c.:

```
./atpg -bridging_fsim -input [input_pattern_file] [circuit_name]
```