Computer Architecture and Organization HW#3

Due by 10/8(Fri.) through HDLMS

1. Translate the following C code to MIPS. Assume that the variables f, g, h, i, and j are assigned to registers $s0, $s1, $s2, $s3, and $s4, respectively. Assume that the base address of the arrays A and B are in registers $s6 and $s7, respectively. Assume that the elements of the arrays A and B are 4-byte words:

```
B[8] = A[i] + A[j];
```

2. Translate the following MIPS code to C. Assume that the variables f, g, h, i, and j are assigned to registers $s0, $s1, $s2, $s3, and $s4, respectively. Assume that the base address of the arrays A and B are in registers $s6 and $s7, respectively.

```
addi $t0, $s6, 4
add $t1, $s6, $0
sw $t1, 0($t0)
lw $t0, 0($t0)
add $s0, $t1, $t0
```

3. Provide the type and assembly language instruction for the following binary value:

$0000\ 0010\ 0001\ 0000\ 1000\ 0000\ 0010\ 0000_{two}$

4. Provide the type, assembly language instruction, and binary representation of instruction described by the following MIPS fields:op=0, rs=3, rt=2, rd=3, shamt=0, funct=34.

5. Consider the following MIPS loop:

```
LOOP:   slt $t2, $0, $t1
        beq $t2, $0, DONE
        subi $t1, $t1, 1
        addi $s2, $s2, 2
        j LOOP
DONE:
```

assume that the register $t1 is initialized to the value N. How many MIPS instructions are executed?