1.

(a) add $s2, $s1, $s1

(b) RegDst = 1, ALUSrc = 0, ALUOP = 10

2.

pipelined processor

: a → 350ps

b → 220ps

non-piplined processor

: a → 1250ps

b → 950ps

3

register $s0 in add instruction
depends on lw instruction.

register $s1 in sub instruction
depends on add instruction

register $s0 in sub instruction
depends on lw instruction.