HW5
COMBINATIONAL SYSTEM 1

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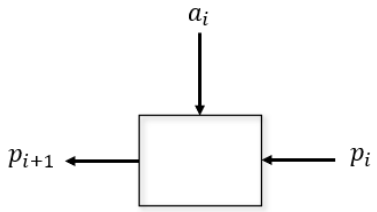
HW5

- 1. We are going to design a circuit to compute an odd parity of an n-bit binary number.
  - The odd parity is generated so that the number of 1's in the (n+1)-bit binary number which is including the parity bit is odd.
  - (a) design a circuit to compute an odd parity of one-bit binary number.
    - Use only NAND gates and NOT gates.
    - Complemented input signals can not be used.
    - Input signals: a_i and p_i
    - Output signal: p_{i+1}



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- 1. We are going to design a circuit to compute an odd parity of an n-bit binary number.
  - (b) design a circuit to compute an odd parity of a 3-bit binary number, (use the circuit designed in (a)) and verify it's operation by logisim-evolution.
  - (c) Determine the delay to compute an odd parity of an n-bit binary number.

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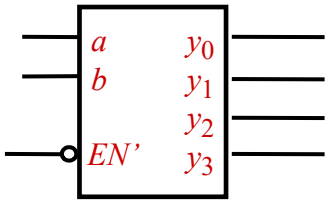
- 2. (a) Design active high 3-to-8 decoder using active high 2-to-4 decoder with enable.
  - Use minimum number of IC's.
  - Can use general gates such as NOT, NAND, and NOR when they are absolutely necessary.
  - Inputs: abc (a: MSB)



EN'	a	b	y_0	y_1	y_2	y_3
1	x	x	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	1	0	0
0	1	0	0	0	1	0
0	1	1	0	0	0	1

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- 2. (b) Design a circuit for f and g using active high 3-to-8 decoder designed in the problem 2(a).
  - $f(a,b,c)=\sum m(1, 3, 6)$, $g(a,b,c)=\sum m(0,4,7)$

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- 3. Design a 4-to-2 priority encoder with the following truth table.

A3	A2	A1	A0	Z1	Z0
0	x	x	x	1	1
1	0	x	x	1	0
1	1	0	x	0	1
1	1	1	0	0	0