

RoboChip

*** note that this is on scratch space of bwrcix. You will need to ssh to the machine.**

The run is at:

/scratch/rezasjd/new-robo/vlsi/build/chipyard.TestHarness.RoboConfig-ChipTop/

Final GDS is at:

/scratch/rezasjd/new-robo/vlsi/build/chipyard.TestHarness.RoboConfig-ChipTop/par-ChipTop/ChipTop.gds

Manual fixes:

1. Diode insertion for antenna violations (eco'd)
2. Removal of VIA2 on the four corners of the 4 clamps in the middle of the die

RTL Sim

Run Located at:

/scratch/rezasjd/new-robo/sims/vcs/output/chipyard.TestHarness.RoboConfig

```
g tools/synopsys/vcs/S-2021.09-SP1-1/include -c /scratch/rezasjd/new-robo/sims/vcs/generated-src/chipyard.TestHarness.RoboConfig/gen-collateral/uart.cc
ccl: warning: command-line option '-std=c++17' is valid for C++/ObjC++ but not for C
/scratch/rezasjd/new-robo/.conda-env/bin/./lib/gcc/x86_64-conda-linux-gnu/12.2.0/../../../../x86_64-conda-linux-gnu/bin/ld: warning: rmar.nd.o: missing .note.GNU-stack section
/scratch/rezasjd/new-robo/.conda-env/bin/./lib/gcc/x86_64-conda-linux-gnu/12.2.0/../../../../x86_64-conda-linux-gnu/bin/ld: NOTE: This behaviour is deprecated and will be removed
/scratch/rezasjd/new-robo/sims/vcs/simv-chipyard-RoboConfig up to date
make[1]: Leaving directory '/scratch/rezasjd/new-robo/sims/vcs/generated-src/chipyard.TestHarness.RoboConfig/chipyard.TestHarness.RoboConfig'
(set -o pipefail && /scratch/rezasjd/new-robo/sims/vcs/simv-chipyard-RoboConfig +permissive +spiflash0=../tests/spiflash.img +spiflash1=../tests/spiflash.img +dramsim +
/src/main/resources/drumsim2.ini +max-cycles=200000000 +ntb_random_seed_automatc +verbose +permissive-off ../tests/hello.riscv </dev/null 2> >(spike-dasm > /scratch/rezasj
o.out) | tee /scratch/rezasjd/new-robo/sims/vcs/output/chipyard.TestHarness.RoboConfig/hello.log)
Chronologic VCS simulator copyright 1991-2021
Contains Synopsys proprietary information.
Compiler version S-2021.09-SP1-1 Full64; Runtime version S-2021.09-SP1-1 Full64; May 13 16:03 2023
NOTE: automatic random seed used: 2739442296
[UART] UART0 is here (stdin/stdout).
[UART] UART0 is here (stdin/stdout).
[UART] UART0 is here (stdin/stdout).
||
hello world
$finish called from file "/scratch/rezasjd/new-robo/sims/vcs/generated-src/chipyard.TestHarness.RoboConfig/gen-collateral/TestDriver.v", line 158.
$finish at simulation time 12995143
VCS Simulation Report
Time: 12995143 ps
CPU Time: 173.580 seconds; Data structure size: 8.0Mb
Sat May 13 16:06:29 2023
(/scratch/rezasjd/new-robo/.conda-env) rezasjd@bwrcix-1: /scratch/rezasjd/new-robo/sims/vcs
```

DRC status

DRC runs are at:

/scratch/rezasjd/new-robo/vlsi/build/chipyard.TestHarness.RoboConfig-ChipTop/

DRCD:

0 errors.

VUE: [...zasjd/new-robo/vlsi/build/chipyard.TestHarness.RoboConfig-ChipTop/drc-final-drcd/drc-ChipTop/ChipT

FileViewToolsClassificationWindowsHelp

Load Results ×Run Summary ×DRC Errors ×

Show AllSearch (Alt+E)

Violation Browser

/Violation/Func	Waive	Total Errors
▼ ChipTop	198,836	198,836
▶ EA_91	1	1
▶ TID_1...	1	1
▶ TID_1...	1	1
▶ TID_1...	1	1
▶ TID_1...	1	1
▶ TID_1...	1	1
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▶ TID_1...	1	1
▶ TID_1...	1	1
▶ TID_1...	1	1
▶ TID_1...	1	1

Error List

IL:

0 errors.

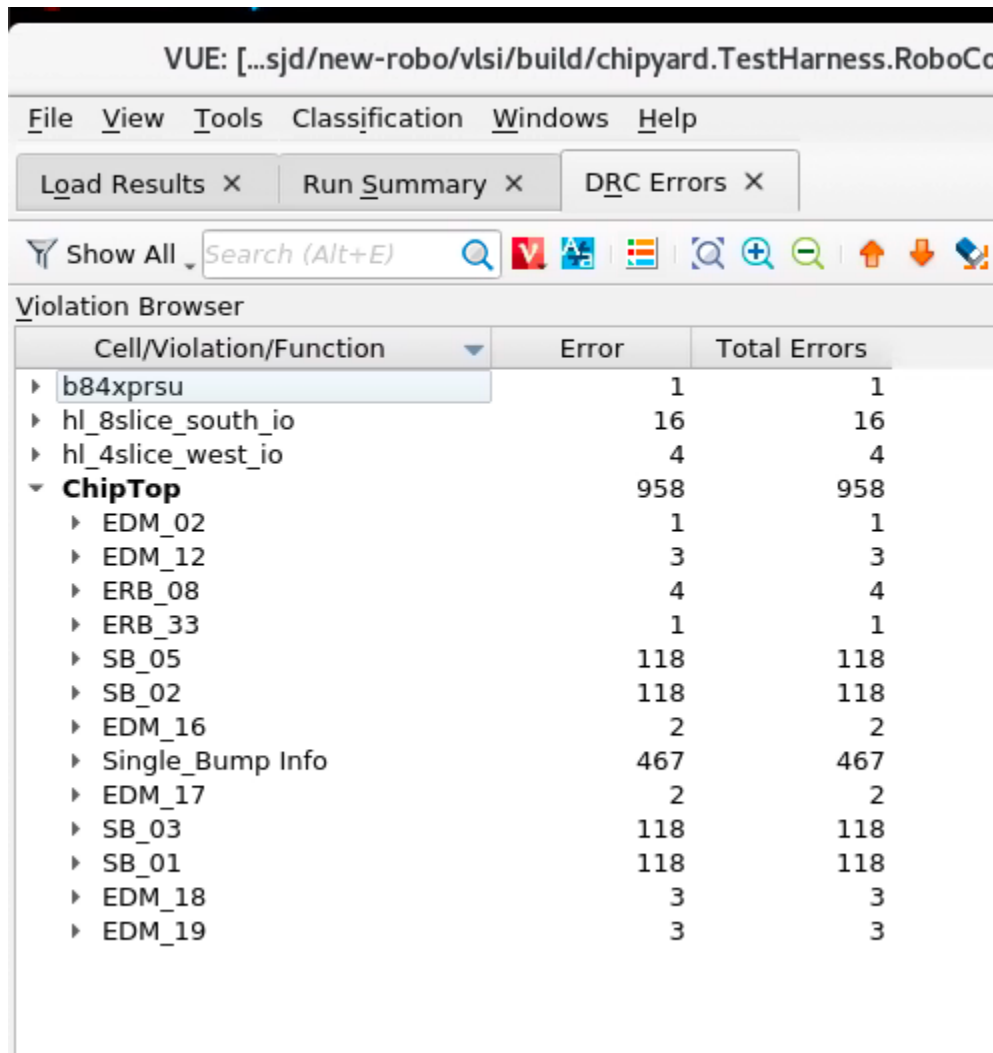
clean

DENALL:

5 errors:

FULLCHIP:

Total of 958 errors. All can be ignored. All due to the existence of two bumps on top of each other. (one hammer/innovus inserted and one from the die ring)



The screenshot shows the VUE Violation Browser window. The title bar reads "VUE: [...sjd/new-robo/vlsi/build/chipyard.TestHarness.RoboCo...". The menu bar includes "File", "View", "Tools", "Classification", "Windows", and "Help". Below the menu bar are three tabs: "Load Results X", "Run Summary X", and "DRC Errors X". A toolbar contains a "Show All" button, a search field with the placeholder "Search (Alt+E)", and several icons for navigation and zooming. The main area is a table titled "Violation Browser" with three columns: "Cell/Violation/Function", "Error", and "Total Errors". The table lists various cells and their associated error counts. The "ChipTop" cell is expanded, showing a list of sub-cells and their error counts.


Cell/Violation/Function	Error	Total Errors
▶ b84xprsu	1	1
▶ hl_8slice_south_io	16	16
▶ hl_4slice_west_io	4	4
▼ ChipTop	958	958
▶ EDM_02	1	1
▶ EDM_12	3	3
▶ ERB_08	4	4
▶ ERB_33	1	1
▶ SB_05	118	118
▶ SB_02	118	118
▶ EDM_16	2	2
▶ Single_Bump Info	467	467
▶ EDM_17	2	2
▶ SB_03	118	118
▶ SB_01	118	118
▶ EDM_18	3	3
▶ EDM_19	3	3

LU:

VUE: [.../rezasjd/new-robo/vlsi/build/chipyard.TestHarness.RoboConfig-ChipTop/drc-final-lu/drc-ChipTop/ChipTop.vue] x

File View Tools Windows Help

Load Results x Run Summary x



LAYOUT ERRORS RESULTS

CLEAN

Model: Intel(R) Xeon(R) Platinum 8380 CPU @ 2.30GHz

DRC Error Statistics

Library name: /scratch/rezasjd/new-robo/vlsi/build/chipyard.TestHarness.RoboConfig-ChipTop/drc-tapein/drc-ChipTop/Chi
Structure name: ChipTop
Generated by: IC Validator RHEL64 S-2021.06-SP3-2.7200131 2022/01/06
Runset name: /scratch/rezasjd/new-robo/vlsi/build/chipyard.TestHarness.RoboConfig-ChipTop/drc-final-lu/drc-ChipTop/d
User name: rezasjd
Time started: 2023/05/13 02:55:45PM
Time ended: 2023/05/13 03:01:09PM

Called as: /tools/synopsys/icv/S-2021.06-SP3-2/bin/LINUX.64/icv -64 -host_init 32 -clf /scratch/rezasjd/new-robo/vlsi/bu
CLF: -i /scratch/rezasjd/new-robo/vlsi/build/chipyard.TestHarness.RoboConfig-ChipTop/drc-tapein/drc-ChipTop/ChipTop.gds

TUC:

VUE: [...rezasjd/new-robo/vlsi/build/chipyard.TestHarness.RoboConfig-ChipTop/drc-final-tuc/drc-ChipTop/ChipTop.vue]

FileViewToolsWindowsHelp

Load Results ×Run Summary ×

LAYOUT ERRORS RESULTS

CLEAN

Model: Intel(R) Xeon(R) Platinum 8380 CPU @ 2.30GHz

DRC Error Statistics

Library name: /scratch/rezasjd/new-robo/vlsi/build/chipyard.TestHarness.RoboConfig-ChipTop/drc-tapein/drc-ChipTop/Chi

Structure name: ChipTop

Generated by: IC Validator RHEL64 S-2021.06-SP3-2.7200131 2022/01/06

Runset name: /scratch/rezasjd/new-robo/vlsi/build/chipyard.TestHarness.RoboConfig-ChipTop/drc-final-tuc/drc-ChipTop/

User name: rezasjd

Time started: 2023/05/13 02:51:53PM

Time ended: 2023/05/13 02:54:57PM

Called as: /tools/synopsys/icv/S-2021.06-SP3-2/bin/LINUX.64/icv -64 -host_init 32 -clf /scratch/rezasjd/new-robo/vlsi/bu

CLF: -i /scratch/rezasjd/new-robo/vlsi/build/chipyard.TestHarness.RoboConfig-ChipTop/drc-tapein/drc-ChipTop/ChipTop.gds


IPALL:

Clean

VUE: [...ezasjd/new-robo/vlsi/build/chipyard.TestHarness.RoboConfig-ChipTop/drc-final-ipall/drc-ChipTop/ChipTop.vue] x

File View Tools Windows Help

Load Results x Run Summary x



LAYOUT ERRORS RESULTS

CLEAN

Model: Intel(R) Xeon(R) Platinum 8380 CPU @ 2.30GHz

DRC Error Statistics

Library name: /scratch/rezasjd/new-robo/vlsi/build/chipyard.TestHarness.RoboConfig-ChipTop/drc-tapein/drc-ChipTop/Chi
Structure name: ChipTop
Generated by: IC Validator RHEL64 S-2021.06-SP3-2.7200131 2022/01/06
Runset name: /scratch/rezasjd/new-robo/vlsi/build/chipyard.TestHarness.RoboConfig-ChipTop/drc-final-ipall/drc-ChipTo
User name: rezasjd
Time started: 2023/05/13 03:02:07PM
Time ended: 2023/05/13 03:11:07PM

Called as: /tools/synopsys/icv/S-2021.06-SP3-2/bin/LINUX.64/icv -64 -host_init 32 -clf /scratch/rezasjd/new-robo/vlsi/bu
CLF: -i /scratch/rezasjd/new-robo/vlsi/build/chipyard.TestHarness.RoboConfig-ChipTop/drc-tapein/drc-ChipTop/ChipTop.gds

LVS status