RoboChip

*** note that this is on scratch space of bwrcix. You will need to ssh to the machine.**
The run is at:
/scratch/rezasjd/new-robo/vlsi/build/chipyard.TestHarness.RoboConfig-ChipTop/

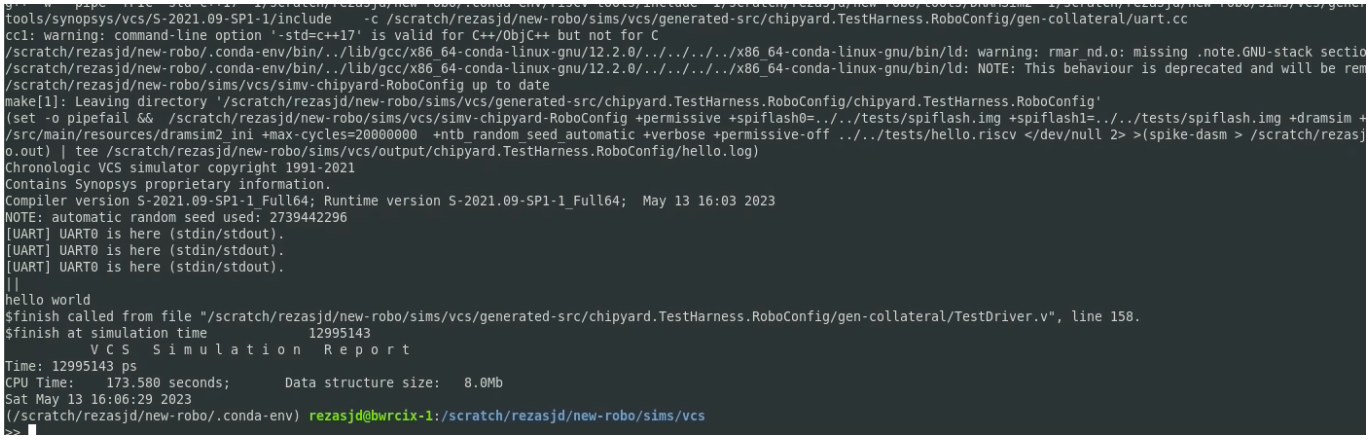
Final GDS is at:
/scratch/rezasjd/new-robo/vlsi/build/chipyard.TestHarness.RoboConfig-ChipTop/par-ChipTop/ChipTop.gds

Manual fixes:

1. Diode insertion for antenna violations (eco'd)
2. Removal of VIA2 on the four corners of the 4 clamps in the middle of the die

RTL Sim

Run Located at:
/scratch/rezasjd/new-robo/sims/vcs/output/chipyard.TestHarness.RoboConfig

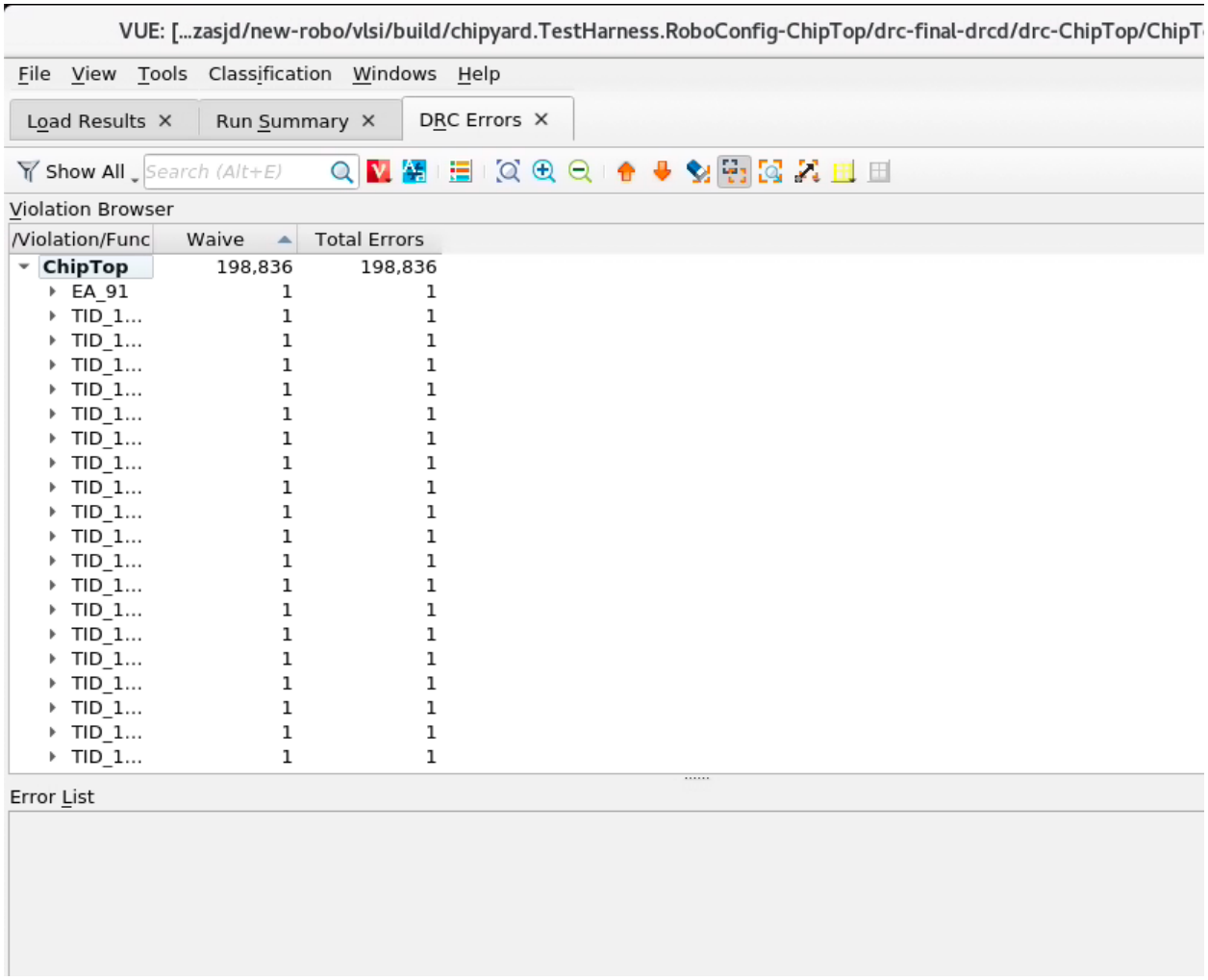


DRC status

DRC runs are at:
/scratch/rezasjd/new-robo/vlsi/build/chipyard.TestHarness.RoboConfig-ChipTop/

DRCD:

0 errors.



IL:

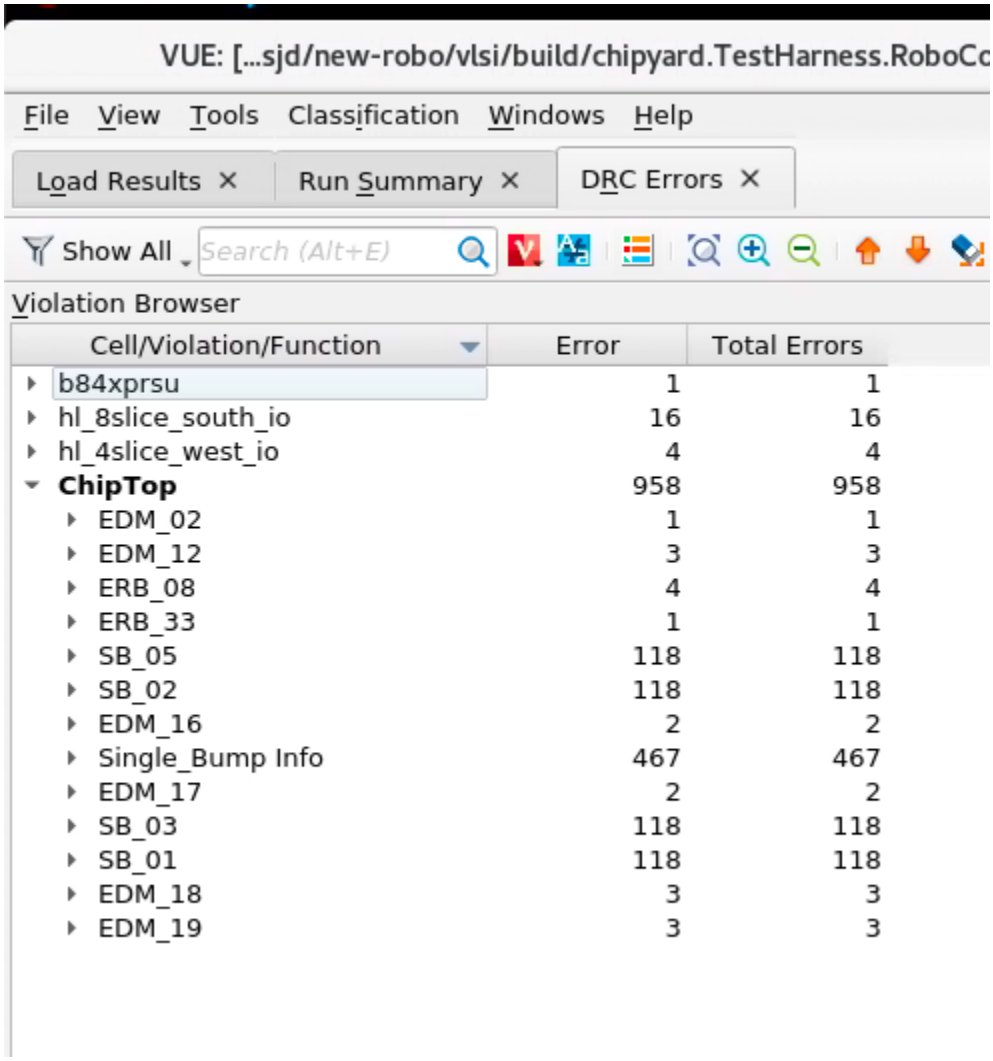
0 errors.
clean

DENALL:

5 errors:

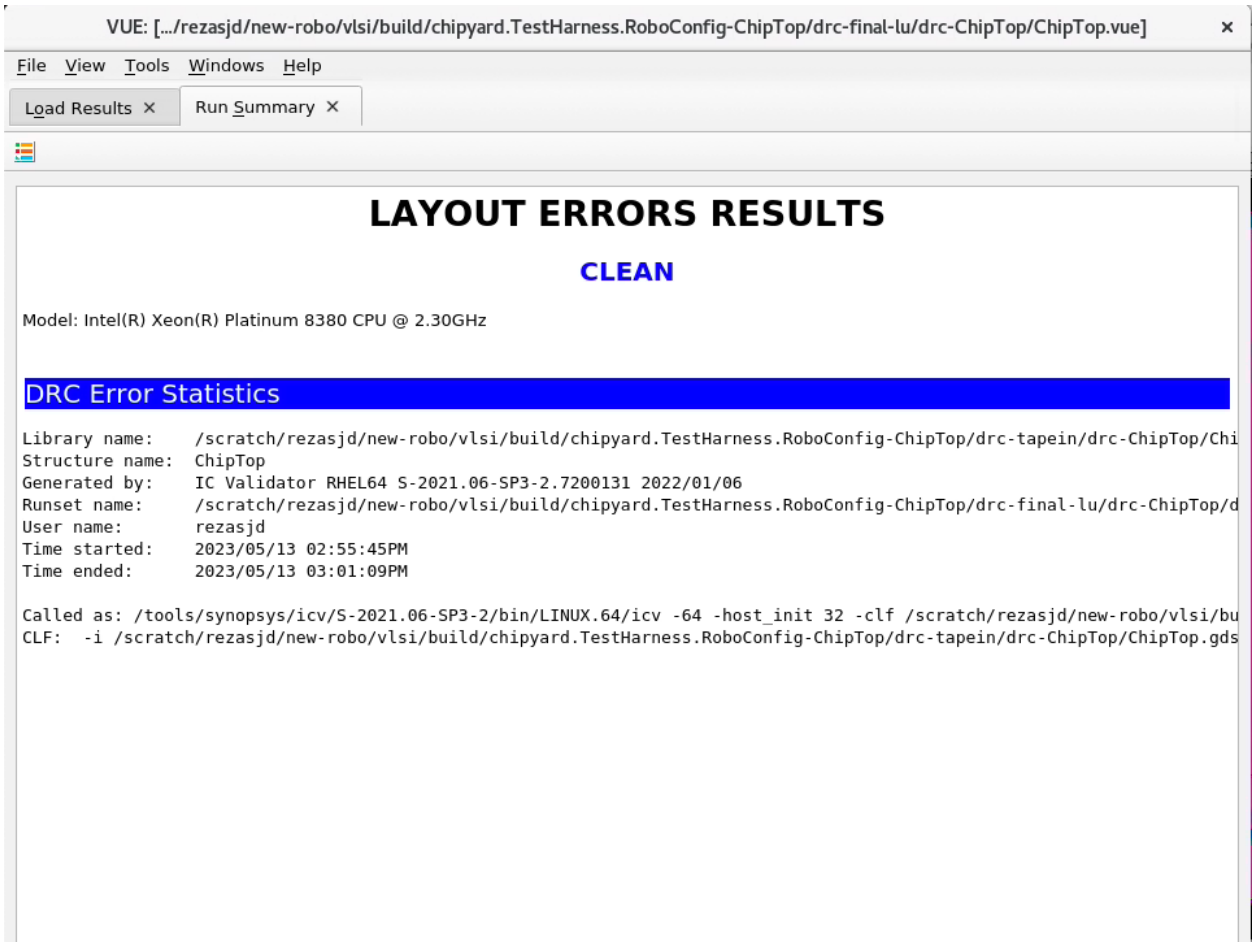
FULLCHIP:

Total of 958 errors. All can be ignored. All due to the existence of two bumps on top of each other. (one hammer/innovus inserted and one from the die ring)

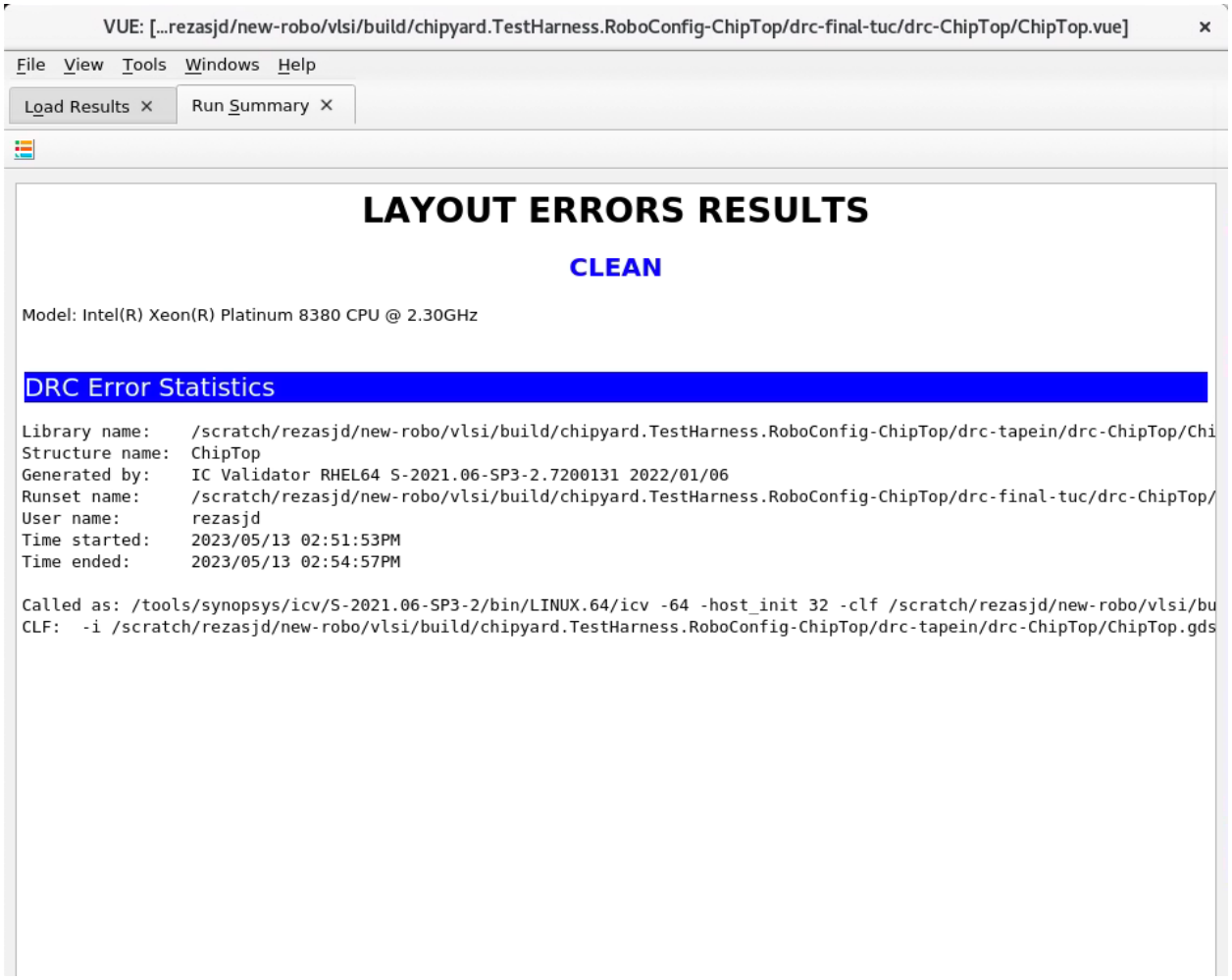


Cell/Violation/Function	Error	Total Errors
b84xprsu	1	1
hl_8slice_south_io	16	16
hl_4slice_west_io	4	4
ChipTop	958	958
EDM_02	1	1
EDM_12	3	3
ERB_08	4	4
ERB_33	1	1
SB_05	118	118
SB_02	118	118
EDM_16	2	2
Single_Bump Info	467	467
EDM_17	2	2
SB_03	118	118
SB_01	118	118
EDM_18	3	3
EDM_19	3	3

LU:

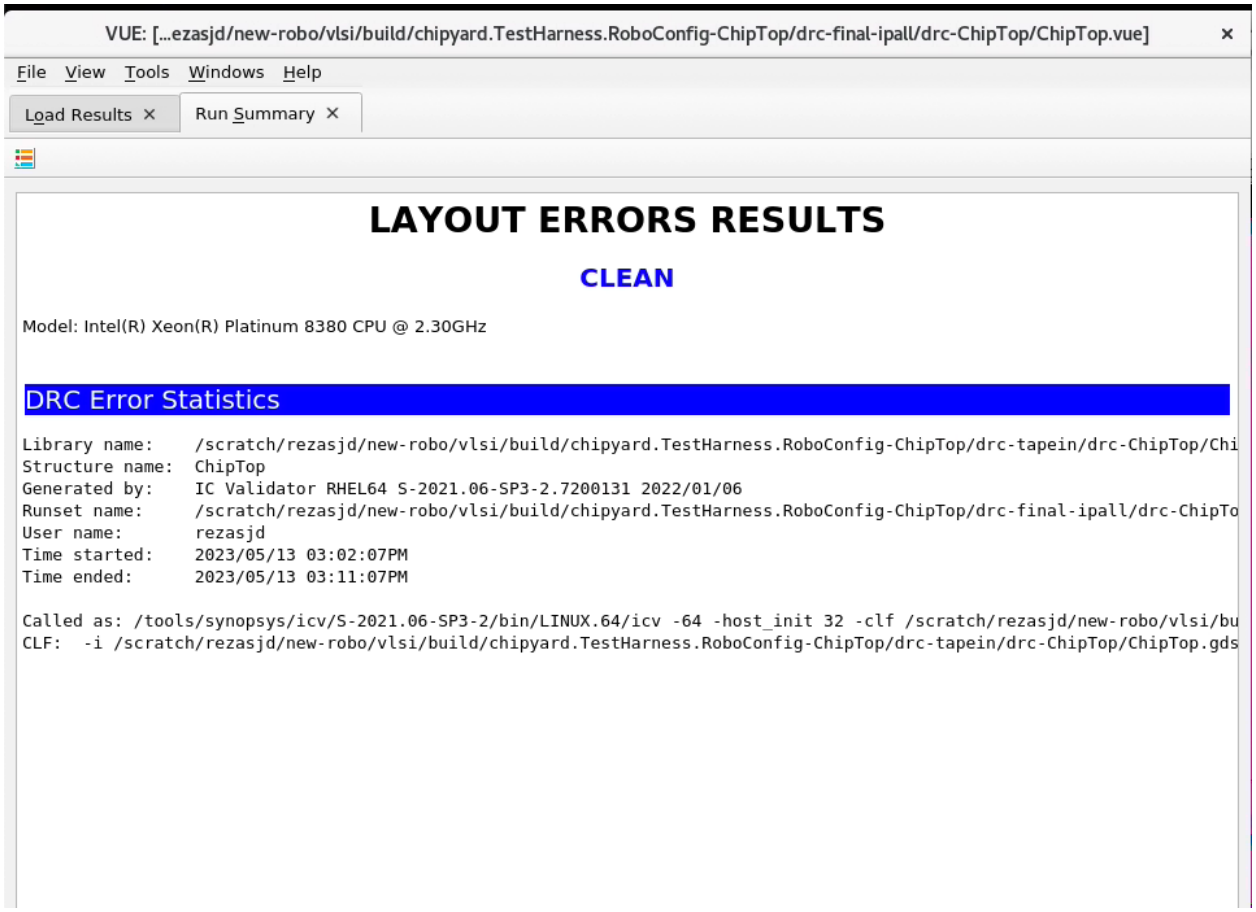

VUE: [.../rezasjd/new-robo/vlsi/build/chipyard.TestHarness.RoboConfig-ChipTop/drc-final-lu/drc-ChipTop/ChipTop.vue]
File View Tools Windows Help
Load Results
Run Summary
LAYOUT ERRORS RESULTS
CLEAN
Model: Intel(R) Xeon(R) Platinum 8380 CPU @ 2.30GHz
DRC Error Statistics
Library name: /scratch/rezasjd/new-robo/vlsi/build/chipyard.TestHarness.RoboConfig-ChipTop/drc-tapein/drc-ChipTop/Chi
Structure name: ChipTop
Generated by: IC Validator RHEL64 S-2021.06-SP3-2.7200131 2022/01/06
Runset name: /scratch/rezasjd/new-robo/vlsi/build/chipyard.TestHarness.RoboConfig-ChipTop/drc-final-lu/drc-ChipTop/d
User name: rezasjd
Time started: 2023/05/13 02:55:45PM
Time ended: 2023/05/13 03:01:09PM
Called as: /tools/synopsys/icv/S-2021.06-SP3-2/bin/LINUX.64/icv -64 -host_init 32 -clf /scratch/rezasjd/new-robo/vlsi/bu
CLF: -i /scratch/rezasjd/new-robo/vlsi/build/chipyard.TestHarness.RoboConfig-ChipTop/drc-tapein/drc-ChipTop/ChipTop.gds

TUC:



IPALL:

Clean


VUE: [...ezasjd/new-robo/vlsi/build/chipyard.TestHarness.RoboConfig-ChipTop/drc-final-ipall/drc-ChipTop/ChipTop.vue]
File View Tools Windows Help
Load Results
Run Summary
LAYOUT ERRORS RESULTS
CLEAN
Model: Intel(R) Xeon(R) Platinum 8380 CPU @ 2.30GHz
DRC Error Statistics
Library name: /scratch/rezasjd/new-robo/vlsi/build/chipyard.TestHarness.RoboConfig-ChipTop/drc-tapein/drc-ChipTop/Chi
Structure name: ChipTop
Generated by: IC Validator RHEL64 S-2021.06-SP3-2.7200131 2022/01/06
Runset name: /scratch/rezasjd/new-robo/vlsi/build/chipyard.TestHarness.RoboConfig-ChipTop/drc-final-ipall/drc-ChipTo
User name: rezasjd
Time started: 2023/05/13 03:02:07PM
Time ended: 2023/05/13 03:11:07PM
Called as: /tools/synopsys/icv/S-2021.06-SP3-2/bin/LINUX.64/icv -64 -host_init 32 -clf /scratch/rezasjd/new-robo/vlsi/bu
CLF: -i /scratch/rezasjd/new-robo/vlsi/build/chipyard.TestHarness.RoboConfig-ChipTop/drc-tapein/drc-ChipTop/ChipTop.gds

LVS status