

BearlyML

*** note that this is on scratch space of bwrcix. You will need to ssh to the machine.**

The run is at:

/scratch/rezasjd/outel/vlsi/build-2/chipyard.TestHarness.BearlyConfig-ChipTop

Final GDS is at:

/scratch/rezasjd/outel/vlsi/build-2/chipyard.TestHarness.BearlyConfig-ChipTop/par-ChipTop/ChipTop.gds

Manual fixes:

1. Diode insertion for antenna violations (eco'd)
2. Removal of VIA2 on the four corners of the 4 clamps in the middle of the die
3. One M8 routing adjustment on top of the PLL

RTL Sim

```
Contains Synopsys proprietary information.
Compiler version S-2021.09-SP1-1_Full64; Runtime version S-2021.09-SP1-1_Full64; May 13 16:02 2023
NOTE: automatic random seed used: 1375321833
[UART] UART0 is here (stdin/stdout).
[UART] UART0 is here (stdin/stdout).
[UART] UART0 is here (stdin/stdout).
[]
[]
hello world
$finish called from file "/scratch/rezasjd/outel/sims/vcs/generated-src/chipyard.TestHarness.BearlyConfig/gen-collateral/TestDriver.v", line 158.
$finish at simulation time 13084283
VCS Simulation Report
Time: 13084283 ps
CPU Time: 516.620 seconds; Data structure size: 34.9Mb
Sat May 13 16:10:44 2023
```

DRC status

DRC runs are at:

/scratch/rezasjd/outel/vlsi/build-2/chipyard.TestHarness.BearlyConfig-ChipTop

DRCD:

0 errors.

VUE: [./scratch/rezasjd/outel/vlsi/build-2/chipyard.TestHarness.BearlyConfig-ChipTop/drc-final-drcd/drc-ChipTop/ChipTop.vue]

File

View

Tools

Classification

Windows

Help

Load Results

Run Summary

DRC Errors

Show All

Search (Alt+E)

Violation Browser

Violation/Func	Waive	Total Errors
<div> <div>ChipTop</div> <div>EA_91</div> <div>TID_1...</div> <div>TID_1...</div> <div>TID_1...</div> <div>TID_1...</div> <div>TID_1...</div> <div>TID_1...</div> <div>TID_1...</div> <div>TID_1...</div> <div>TID_1...</div> <div>TID_1...</div> <div>TID_1...</div> <div>TID_1...</div> <div>TID_1...</div> <div>TID_1...</div> <div>TID_1...</div> <div>TID_1...</div> <div>TID_1...</div> <div>TID_1...</div> <div>TID_1...</div> </div>	<div>198,836</div> <div>1</div> <div>1</div> <div>1</div> <div>1</div> <div>1</div> <div>1</div> <div>1</div> <div>1</div> <div>1</div> <div>1</div> <div>1</div> <div>1</div> <div>1</div> <div>1</div> <div>1</div> <div>1</div> <div>1</div> <div>1</div> <div>1</div>	<div>198,836</div> <div>1</div> <div>1</div> <div>1</div> <div>1</div> <div>1</div> <div>1</div> <div>1</div> <div>1</div> <div>1</div> <div>1</div> <div>1</div> <div>1</div> <div>1</div> <div>1</div> <div>1</div> <div>1</div> <div>1</div> <div>1</div> <div>1</div>

IL:

0 errors.

Cell/Violation/Function	Waive	Total Errors
unl2_2x2sub4x4_c4_er.edm...	3	3
IL_edm_id-EDMID edm_...	2	2
IL_ER_diffCheck_drawing	1	1

DENALL:

5 errors:

VUE: [/scratch/rezasjd/outel/vlsi/build-2/chippyard.TestHarness.BearlyConfig-ChipTop/drc-final-denall/drc-ChipTop/ChipTop.vue]
File View Tools Classification Windows Help

Load Results x Run Summary x DRC Errors x

Show All Search (Alt+E)

Violation Browser

Cell/Violation/Function	Error	Total Errors
▼ ChipTop	5	5
▼ LD_153	5	5
gradient_density ...	5	5

KB

Bhutada, Kajol

RE: Ring PLL Desnity

To: Sajadiany, Reza

May 6, 2023 at 11:07 PM

Hi Reza,

If it's LD_* then it's fine. Or you can check the DRC excel spreadsheet in the ring pll documentation to see all DRC waivers for ringpll.

Path to dir: \$INTEL_PDK/./gpio (the ring pll dir should be there)

Thanks,
Kajol

[See More from Reza Sajadiany](#)

FULLCHIP:

Total of 958 errors. All can be ignored. All due to the existence of two bumps on top of each other. (one hammer/innovus inserted and one from the die ring)

VUE: [/scratch/rezasjd/outel/vlsi/build-2/chipyard.TestHarness.BearlyConfig-ChipTop/drc-final-fullchip/drc-ChipTop/ChipTop.vue]

Cell/Violation/Function	Error	Total Errors
ChipTop	958	958
Single_Bump Info	467	467
SB_03	118	118
SB_01	118	118
SB_05	118	118
SB_02	118	118
ERB_08	4	4
EDM_12	3	3
EDM_18	3	3
EDM_19	3	3
EDM_17	2	2
EDM_16	2	2
EDM_02	1	1
ERB_33	1	1
hl_8slice_south_io	16	16
hl_4slice_west_io	4	4
b84xprsu	1	1

LU:

VUE: [/scratch/rezasjd/outel/vlsi/build-2/chipyard.TestHarness.BearlyConfig-ChipTop/drc-final-lu/drc-ChipTop/ChipTop.vue]

Layout Results X

Run Summary X

LAYOUT ERRORS RESULTS

CLEAN

Model: Intel(R) Xeon(R) Platinum 8380 CPU @ 2.30GHz

DRC Error Statistics

Library name: /scratch/rezasjd/outel/vlsi/build-2/chipyard.TestHarness.BearlyConfig-ChipTop/drc-tapein/drc-ChipTop/ChipTop.gds
Structure name: ChipTop
Generated by: IC Validator RHEL64 5-2021.06-SP3-2.7200131 2022/01/06
Runset name: /scratch/rezasjd/outel/vlsi/build-2/chipyard.TestHarness.BearlyConfig-ChipTop/drc-final-lu/drc-ChipTop/drc_run_file
User name: rezasjd
Time started: 2023/05/09 03:53:41PM
Time ended: 2023/05/09 03:58:54PM

Called as: /tools/synopsys/icv/5-2021.06-SP3-2/bin/LINUX.64/icv -64 -host init 32 -clf /scratch/rezasjd/outel/vlsi/build-2/chipyard.TestHarness.BearlyConfig-ChipTop/drc-final-lu/drc-ChipTop/drc_args_file -vue -verb
CLF: -i /scratch/rezasjd/outel/vlsi/build-2/chipyard.TestHarness.BearlyConfig-ChipTop/drc-tapein/drc-ChipTop/ChipTop.gds -c ChipTop -f GDSII -D _drLAYERSTACK=ml1_1x_3xa_1xb_1xc_2y

TUC:

VUE: [/scratch/rezasjd/outel/vlsi/build-2/chipyard.TestHarness.BearlyConfig-ChipTop/drc-final-tuc/drc-ChipTop/ChipTop.vue]

FileViewToolsWindowsHelp

Load Results XRun Summary X

LAYOUT ERRORS RESULTS

CLEAN

Model: Intel(R) Xeon(R) Platinum 8380 CPU @ 2.30GHz

DRC Error Statistics

Library name: /scratch/rezasjd/outel/vlsi/build-2/chipyard.TestHarness.BearlyConfig-ChipTop/drc-tapein/drc-ChipTop/ChipTop.gds

Structure name: ChipTop

Generated by: IC Validator RHEL64 5-2021.06-SP3-2.7200131 2022/01/06

Runset name: /scratch/rezasjd/outel/vlsi/build-2/chipyard.TestHarness.BearlyConfig-ChipTop/drc-final-tuc/drc-ChipTop/drc_run_file

User name: rezasjd

Time started: 2023/05/09 03:49:45PM

Time ended: 2023/05/09 03:52:48PM

Called as: /tools/synopsys/icv/5-2021.06-SP3-2/bin/LINUX.64/icv -64 -host_init 32 -clf /scratch/rezasjd/outel/vlsi/build-2/chipyard.TestHarness.BearlyConfig-ChipTop/drc-final-tuc/drc-ChipTop/drc_args_file -vue -verbose /scratch/rezasjd/outel/vlsi/build-2/chipyard.TestHarness.BearlyConfig-ChipTop/drc-tapein/drc-ChipTop/ChipTop.gds -c ChipTop -f 00511 -D _drLAYERSTACK=m11_1x_3xa_1xb_1xc_2yb_2ga_min2_1gb_bumpp -D DR_L

IPALL:

This one is a relief:

VUE: [/scratch/rezasjd/outel/vlsi/build-2/chipyard.TestHarness.BearlyConfig-ChipTop/drc-final-ipall/drc-ChipTop/ChipTop.vue]

FileViewToolsWindowsHelp

Load Results XRun Summary X

LAYOUT ERRORS RESULTS

CLEAN

Model: Intel(R) Xeon(R) Platinum 8380 CPU @ 2.30GHz

DRC Error Statistics

Library name: /scratch/rezasjd/outel/vlsi/build-2/chipyard.TestHarness.BearlyConfig-ChipTop/drc-tapein/drc-ChipTop/ChipTop.gds

Structure name: ChipTop

Generated by: IC Validator RHEL64 5-2021.06-SP3-2.7200131 2022/01/06

Runset name: /scratch/rezasjd/outel/vlsi/build-2/chipyard.TestHarness.BearlyConfig-ChipTop/drc-final-ipall/drc-ChipTop/drc_run_file

User name: rezasjd

Time started: 2023/05/09 03:59:57PM

Time ended: 2023/05/09 04:07:50PM

Called as: /tools/synopsys/icv/5-2021.06-SP3-2/bin/LINUX.64/icv -64 -host_init 32 -clf /scratch/rezasjd/outel/vlsi/build-2/chipyard.TestHarness.BearlyConfig-ChipTop/drc-final-ipall/drc-ChipTop/drc_args_file -vue -verbose /scratch/rezasjd/outel/vlsi/build-2/chipyard.TestHarness.BearlyConfig-ChipTop/drc-tapein/drc-ChipTop/ChipTop.gds -c ChipTop -f 00511 -D _drLAYERSTACK=m11_1x_3xa_1xb_1xc_2yb_2ga_min2_1gb_bumpp -D DR_L

LVS status