BearlyML

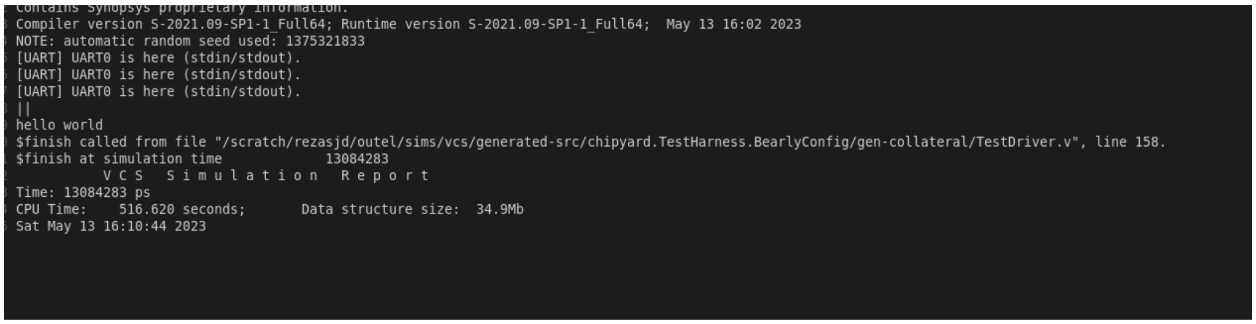
*** note that this is on scratch space of bwrcix. You will need to ssh to the machine.**
The run is at:
/scratch/rezasjd/outel/vlsi/build-2/chipyard.TestHarness.BearlyConfig-ChipTop

Final GDS is at:
/scratch/rezasjd/outel/vlsi/build-2/chipyard.TestHarness.BearlyConfig-ChipTop/par-ChipTop/ChipTop.gds

Manual fixes:

1. Diode insertion for antenna violations (eco'd)
2. Removal of VIA2 on the four corners of the 4 clamps in the middle of the die
3. One M8 routing adjustment on top of the PLL

RTL Sim

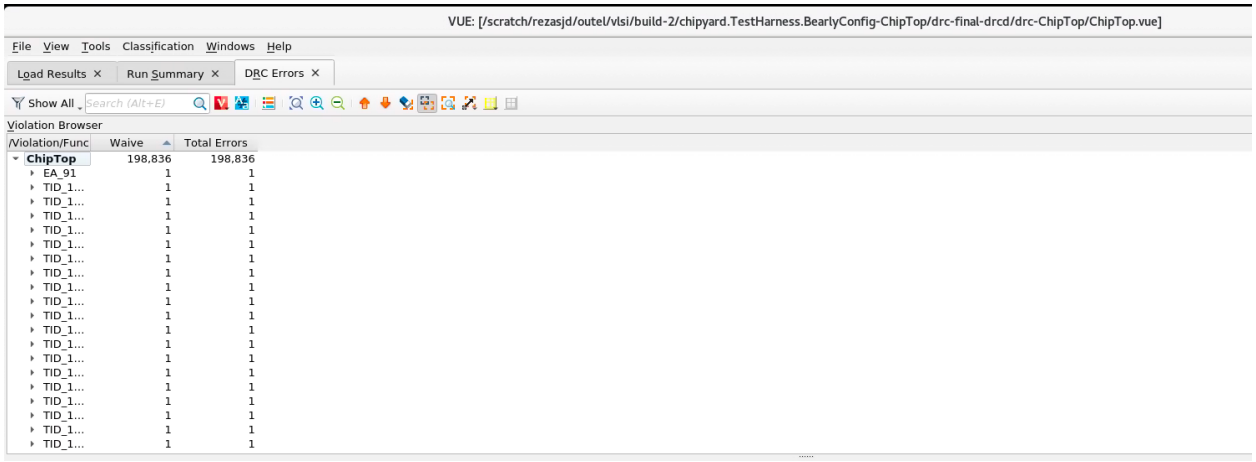


DRC status

DRC runs are at:
/scratch/rezasjd/outel/vlsi/build-2/chipyard.TestHarness.BearlyConfig-ChipTop

DRCD:

0 errors.

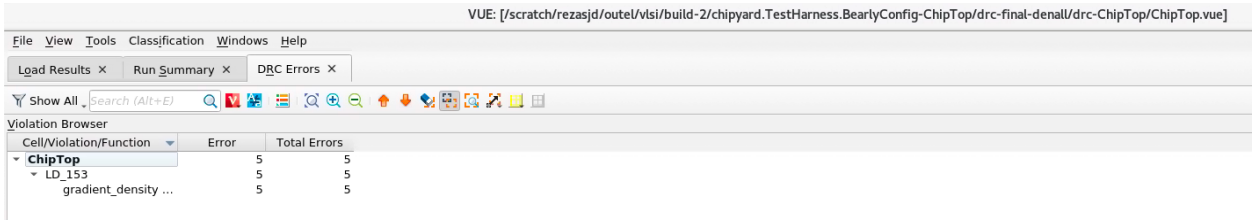


IL:

0 errors.

DENALL:

5 errors:



KB **Bhutada, Kajol** May 6, 2023 at 11:07 PM
RE: Ring PLL Desnity
To: Sajadiany, Reza

Hi Reza,

If it's LD_* then it's fine. Or you can check the DRC excel spreadsheet in the ring pll documentation to see all DRC waivers for ringpll.

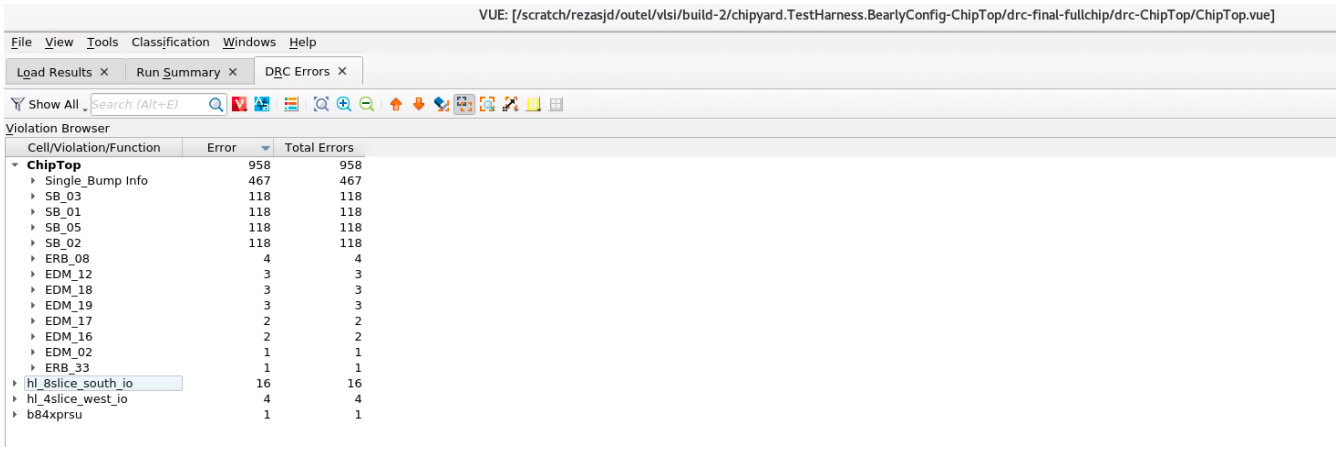
Path to dir: $INTEL_PDK/../gpio (the ring pll dir should be there)

Thanks,
Kajol

See More from Reza Sajadiany

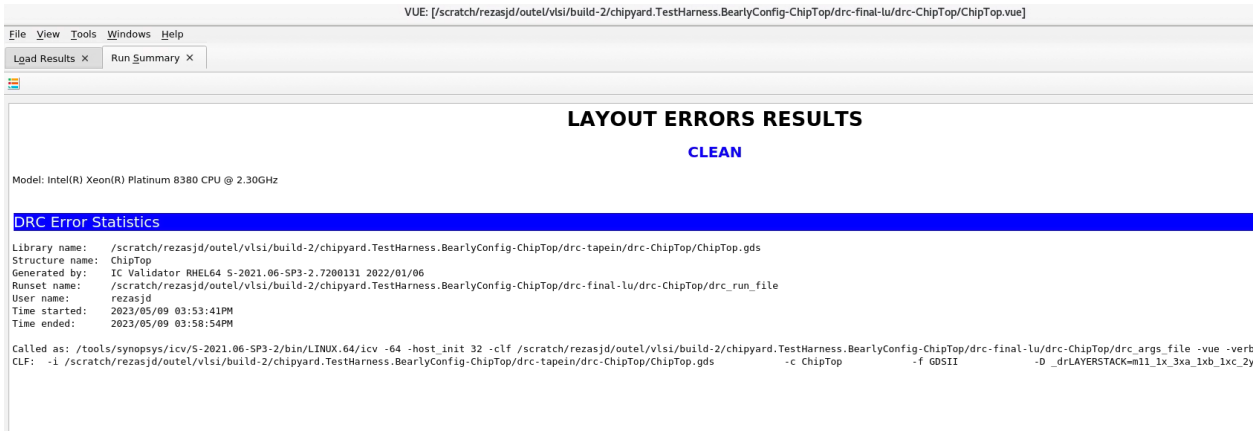
FULLCHIP:

Total of 958 errors. All can be ignored. All due to the existence of two bumps on top of each other. (one hammer/innovus inserted and one from the die ring)

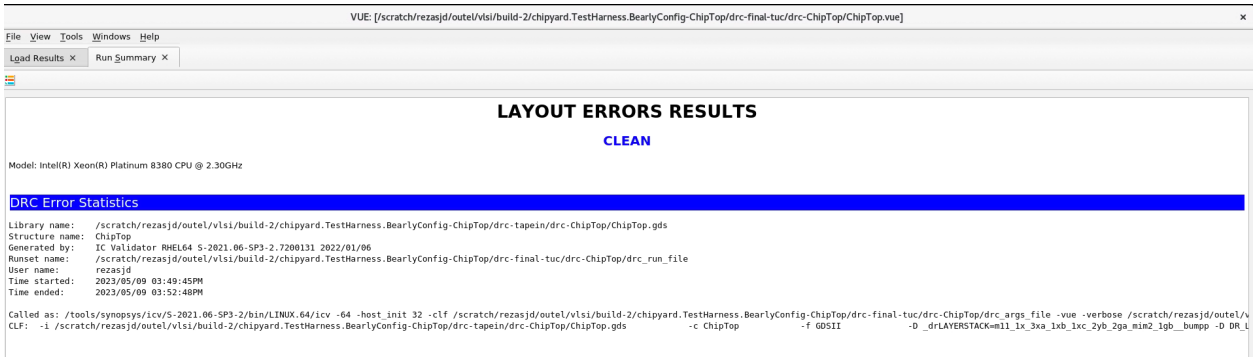


Cell/Violation/Function	Error	Total Errors
ChipTop	958	958
Single_Bump Info	467	467
SB_03	118	118
SB_01	118	118
SB_05	118	118
SB_02	118	118
ERB_08	4	4
EDM_12	3	3
EDM_18	3	3
EDM_19	3	3
EDM_17	2	2
EDM_16	2	2
EDM_02	1	1
ERB_33	1	1
hl_8slice_south_io	16	16
hl_4slice_west_io	4	4
b84xprsu	1	1

LU:

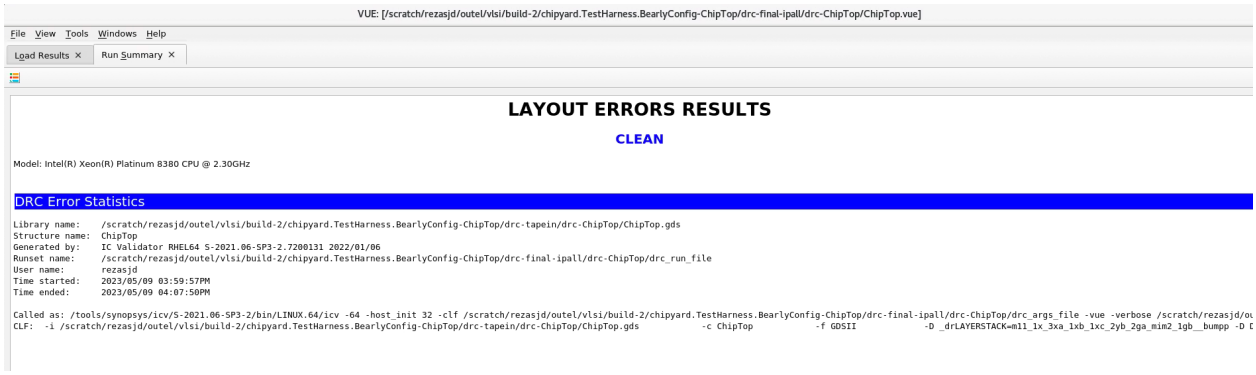


TUC:



IPALL:

This one is a relief:



LVS status