Internal Assessment 2020

Sourik Sarkar
18700118029
CSE A
Sem 4

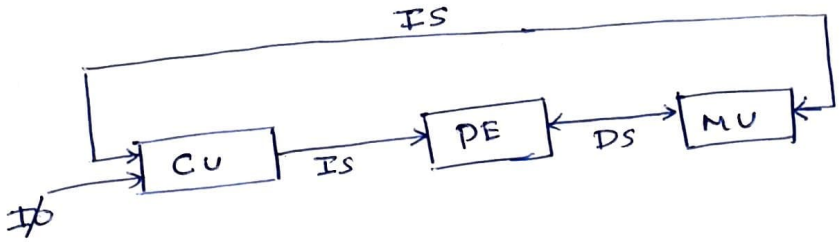
Date: 07/10/2020

1. Based on michel J. Flynn proposed the classification of computer organization. State clear block diagram of machine configuration.

Ans → Michel J. Flynn classification of parallarl computer architecture is based on no of concurrent instruction and clata stream available in architecture.

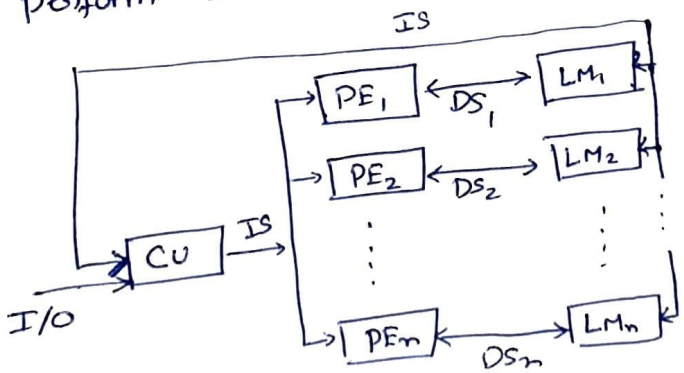
i SISD → (Single Instruction Single Data)

A single processor execute a single instruction stream to operate on data stored on single memory.



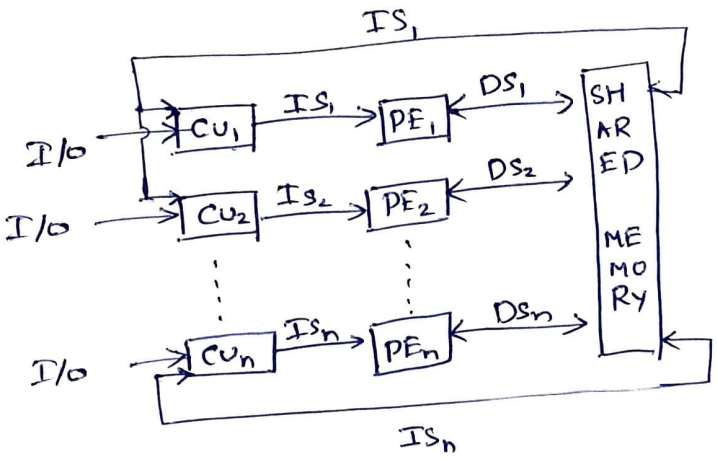
ii SIMD (Single Instruction Multiple Data)

Type of parallarl computing where multiple Processors perform same operation on different data.



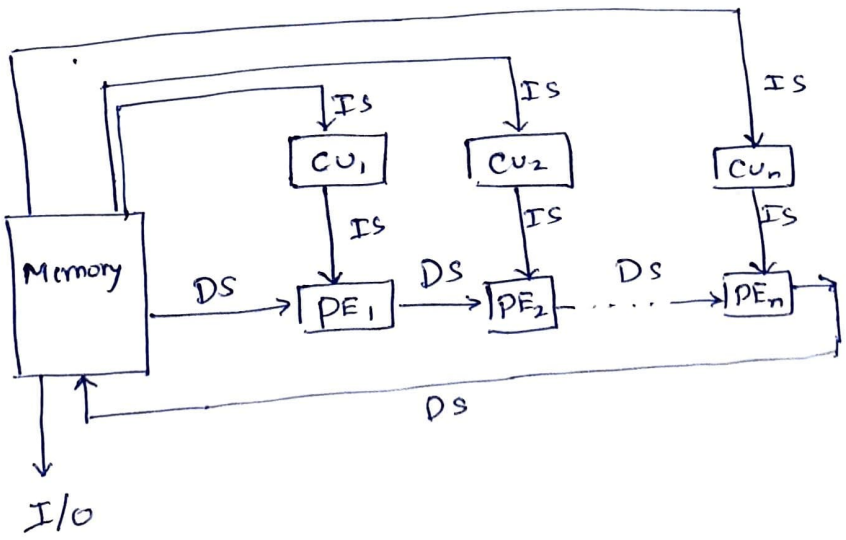
MIMD (Multiple Instruction ~~Stream~~ Multiple Data ~~Stream~~)

In MIMD multiple Control Unit is connected to a shared memory via different processor as a result different operation can be performed on different set of data independently.



MISD (Multiple Instruction ~~Stream~~ Single Data ~~Stream~~)

Here, multiple Control Unit is connected to Same memory via different processor as a result multiple process can be performed on a same data.



2. ~~Locality o~~ Discuss what you understand by locality of referance with diagram.

Ans Locality of referance is the tendency of a processor to access same set of memory location again and again over a short period of time.

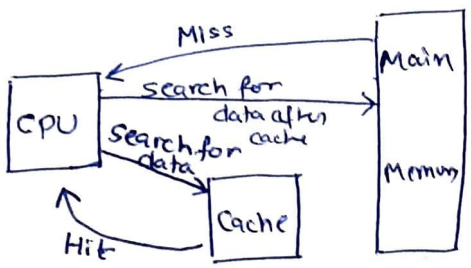
There are 3 types of locality of referance —

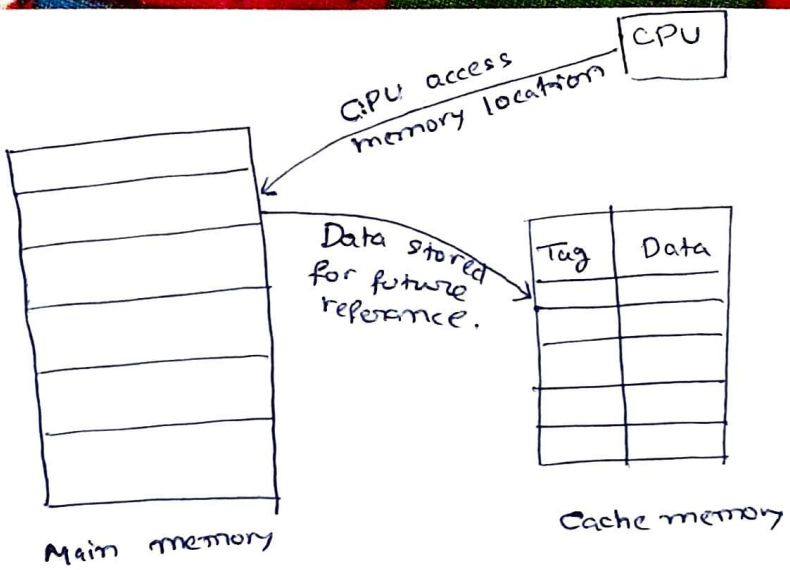
i) Temporal locality

ii) Spacial locality

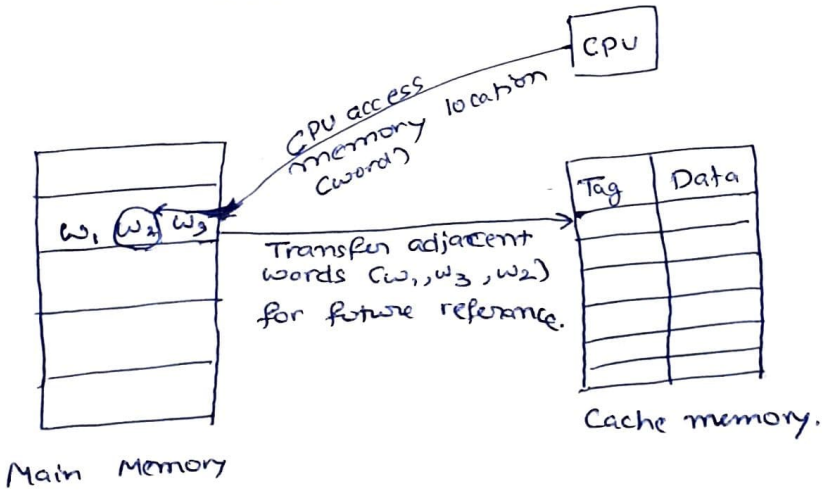
iii) Sequential locality.

In a computer main memory is devided into blocks and cache is devided into block. and the size of main memory is larger than the size of cache memory as a result for the processor to access data we have to put the data in MM to cache memory but this is not possible because of size difference. So we put some of the blocks of MM to cache memorry based either on space (spacial locality) or time (Temporal locality). So in spacial ~~the~~ if a word is transferred to the cache ~~we~~ then the word ~~else~~ with close proximity will be transferred as well. In Temporal if a word is accessed now then there is a high chance for the word to access again.





Temporal locality.



Spacial locality

3. A 50 MHz processor was used to execute a program with following instruction mix and clock cycle counts:

Instruction	Count	Clock
Integer arith	50,000	2
Data transfer	70,000	3
Floating arith	25,000	1
Branch	4000	2

$$CPI = \frac{\sum_{i=1}^{n} (count_i \times clock_i) \quad (\text{Total clock cycle})}{\sum_{i=1}^{n} count. \quad (\text{Total Instruction})}$$

$$= \frac{(50,000 \times 2) + (70,000) \times 3 + (25,000 \times 1) + (4000 \times 2)}{50,000 + 70,000 + 25,000 + 4000}$$

$$= \frac{100\,000 + 210\,000 + 25000 + 8000}{149\,000}$$

$$= \frac{343\,000}{149000} = 2.3$$

$$MIPS = \frac{f}{CPI \times 10^6} = \frac{50 \times 10^6}{2.3 \times 10^6} = 21.74 .$$

$$\text{Execution time} = \text{Total clock cycle} \times \frac{1}{f}$$

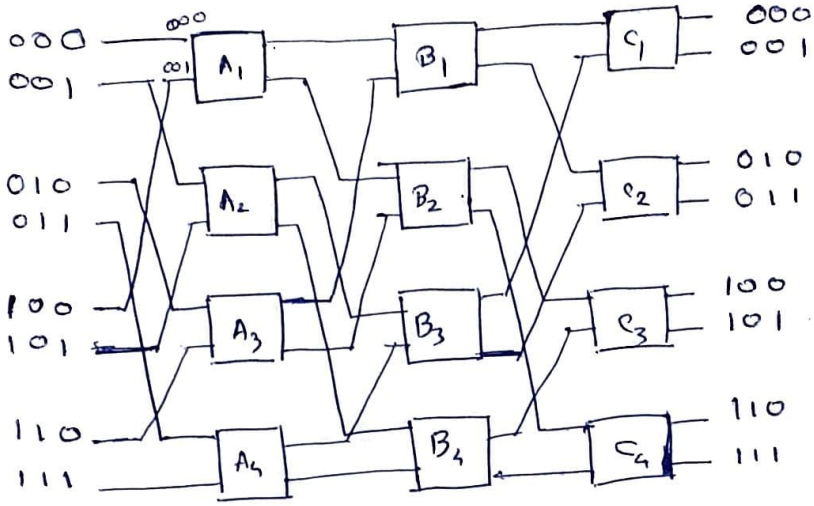
$$= 343000 \times \frac{1}{50 \times 10^6} = 0.00686 \text{ sec} .$$

(4)

Super pipeline	Super scalar	VLIW
Dividing long Stages to several shorter stages.	Dynamically issuing multiple instruction per cycle.	Combining several instruction into very long instruction.
Only one instruction issued per cycle.	N instruction per cycle. N is the degree of ~~so~~ pipeline	M instruction per cycle.
Instruction size is small.	Instruction size is small	Instruction size is large.
Compatable accross generation	Compatable accross generation.	Not compatable accross generation.
easier to design	Complex design	Complex design as well as compile is needed

5. Build 8x8 omega network.

$8 = 2^3$ so 3 stages are there.



Each A_i, B_i, C_i is a 2x2 switch

So for 8 inputs 4 such switch is needed in each stage.