A New Phase-Locked Loop (PLL) System

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Abstract

An enhanced phase-locked loop (PLL) system is presented and its properties and performance characteristics are investigated. Advantages of the proposed PLL structure over the conventional PLLs including its capability of direct estimation of amplitude and phase angle of its input signal, within a wide range of parameters, are demonstrated. Main features of the proposed PLL are structural simplicity and performance robustness. Performance of the PLL, based on both analog and digital realization, is also presented.

I. Introduction

PHASE -locked loop (PLL) is a fundamental concept widely used for different purposes in various fields of electrical engineering e.g. communications, instrumentation, control system, and multimedia apparatus [1]. The main idea of phase-locking is the ability to generate a sinusoidal signal whose phase is coherently following that of the main component of the input signal [2], [3]. PLLs have been the subject of R&D for several decades [5], [6]. The significant recent developments in microelectronics have had tremendous impact on the PLL technology [4], [2].

Figure 1 shows the block diagram of a PLL. The phase difference between the input and the output signals is measured using a phase detector (PD) and passed through a loop filter (LF) to generate an error signal driving a voltage-controlled oscillator (VCO) which generates the output signal.

An intuitive structure for PD is a multiplier. The output of LF is a measure of the total phase difference of the two input signals of PD. Ideally, the error signal is proportional to, or at least a monotonic function of, the total phase difference of the two input signals of PD. An ideal error signal cannot be achieved and this shortcoming is one of the main reasons for the ongoing theoretical and practical work on PLL.

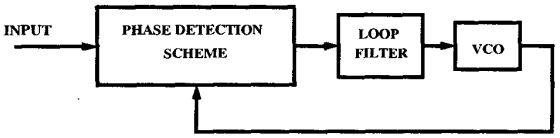

Fig. 1. Phase-locked loop (PLL) structure

This paper presents a new PLL concept based on an alternative method of phase detection [7]. Instead of phase difference between the input and the output signals, the proposed scheme directly estimates the phase of the fundamental component of the input signal the variation of which is exactly the signal that VCO requires to generate a synchronous signal with the input.

II. Proposed PLL

The main contribution in the structure of the proposed PLL is in the introduction of a novel phase detection scheme which is shown in more detail in Fig. 2. Rather than multiplying the input signal by the output of VCO to generate a signal whose phase is expected to be the phase difference of these two signals, a refined variant of the VCO signal is subtracted from the input signal to produce an intermediary signal. This intermediary signal is then multiplied by the output of VCO the same way as the input signal is multiplied by the output of VCO in conventional PLLs.

III. Features of the Proposed PLL

The output of VCO, i.e. $y(t)$ of Fig. 2, is the synthesized output. The output of the integration block of PD of Fig. 2, i.e. $A(t)$, is the estimated amplitude of such a synthesized output.

The input of the VCO, or the output of the LF, is the estimated time derivative of the total phase. Therefore, for the proposed PLL, the values of the amplitude and phase of the synthesized component are available, a fact which renders the structure an amplitude/phase

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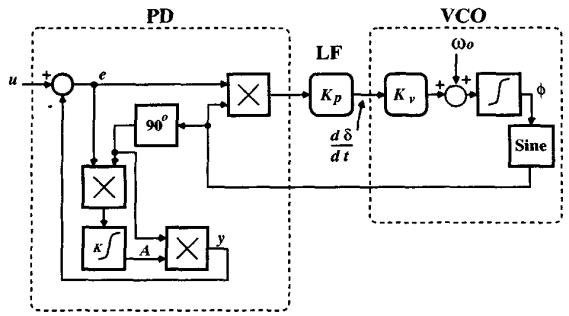

Fig. 2. Structure of the proposed PLL

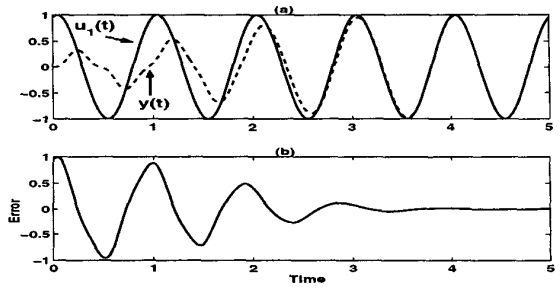

Fig. 3. Performance of the proposed PLL: (a) input and synthesized output, (b) difference between input and synthesized output.

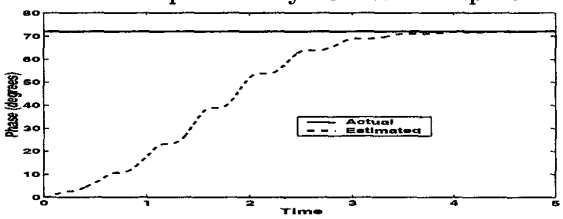

Fig. 4. Demonstration of the phase locking corresponding to the case of of Fig. 3. The input signal starts at initial phase of 72 degrees and the output estimates the phase.

estimator PLL.

One multiplication, required by conventional PLLs, is replaced by a phase-shift of 90 degrees, three multiplications, one subtraction and one integration in the proposed PLL. With today's available technology of electronic circuitry, these extra units add practically no complexity. Moreover, the structure of the loop filter may remain as simple as a gain which substantially reduces the overall complexity of the system.

One more feature of the PLL is that the output is locked both in phase and in amplitude. In contrast to a conventional PLL which provides only an output signal *coherent* with the input signal, the PLL provides an output signal *synchronous* with the input signal. In other words, the input and output phase angles are not only locked but also equal. Moreover, the PLL directly provides the estimates of the amplitude and phase of the main component of the input signal in addition to the synthesized output.

Another feature of the proposed PLL is its immunity to noise. From this aspect, the structure is very robust with respect to externally imposed conditions which may be manifested as pollution in the input signal, e.g. white noise, harmonic distortion, disturbances, etc.

The PLL is also robust with respect to its internal structure; small variations of the internal parameters such as K, K_p and the VCO's central frequency (ω_o) are tolerated without noticeable effect on the performance of the loop.

IV. Stability Analysis

The following theorem, which is proved in [12], states that the proposed PLL in addition to generating a signal coherent with its input, it directly estimates the basic characteristics of its input signal including its amplitude and phase angle.

Theorem: *(Amplitude-Phase-Locked Loop)* The PLL system shown in Fig. 2 simultaneously extracts an output signal $y(t)$ where its amplitude and phase, which are both directly estimated, are locked with the associated parameters of the fundamental component of the input signal.

V. Computer Simulations

Computer simulations are presented for performance evaluation of the introduced PLL. The input signal $u(t)$ is a single sinusoidal signal $u_1(t) = A\sin(\omega t+\theta)$ in most cases. The output signal $y(t)$ is the sinusoidal signal generated by VCO which is to coherently follow $u_1(t)$.

Figure 3 shows performance of the proposed PLL in its most basic form. The PLL is to determine the value of the phase of the input signal and to produce a signal whose phase is equal to that of the input. Similarly, the amplitude of the output signal is equal to that of the input signal. Parameters K and K_pK_v determine the speed of the loop in tracking the amplitude and phase, respectively. The loop generates a precise replica of the input; therefore, the difference between the input signal and the output approaches zero in a certain number of cycles which is controllable by the parameters. It is noteworthy that in a conventional PLL, such an error signal does not approach zero for two reasons: 1) the phases are not equal, but their difference is ideally a constant, and 2) the amplitudes need not be equal. Figure 4 shows variations of the phase of the synthesized output which tracks the input phase angle.

Figures 5 and 6 show performance of the proposed PLL when a step change of 50% in amplitude of the

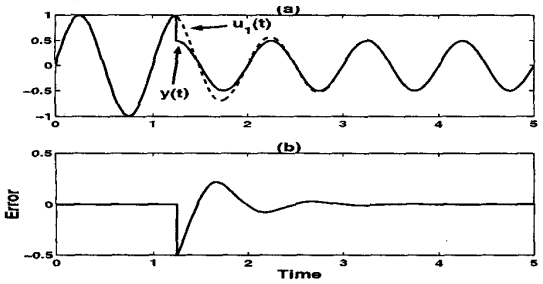

Fig. 5. Response of the PLL to a step change of 50% in the amplitude of the input signal: (a) input and output, (b) transient error.

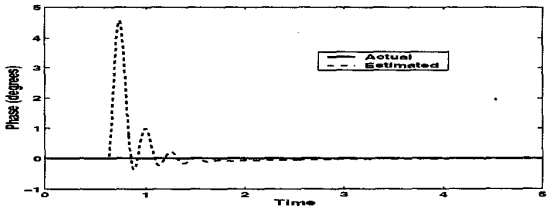

Fig. 6. Transient phase error incurred due to the step change of 50% in the amplitude. Phase angle transient rapidly damps out.

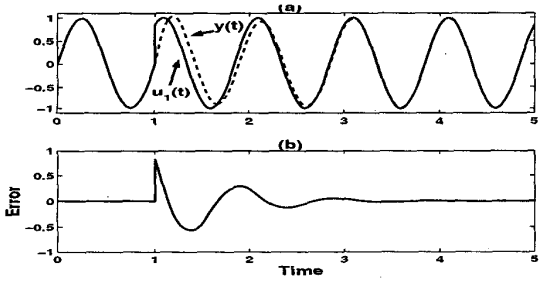

Fig. 7. Response of the PLL to a step change of one radian in the phase of the input signal: (a) input and output, (b) transient error.

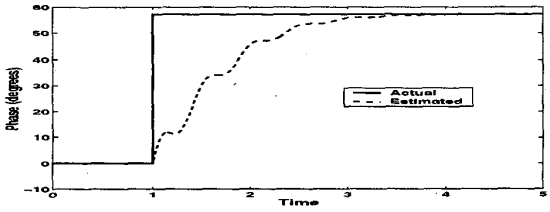

Fig. 8. Transient phase error incurred due to the step change of one radian in the phase: the change is rapidly detected by the PLL.

input signal occurs. It is observed that the structure is sufficiently robust and adapts itself to the new value of the amplitude.

Figures 7 and 8 show performance of the proposed

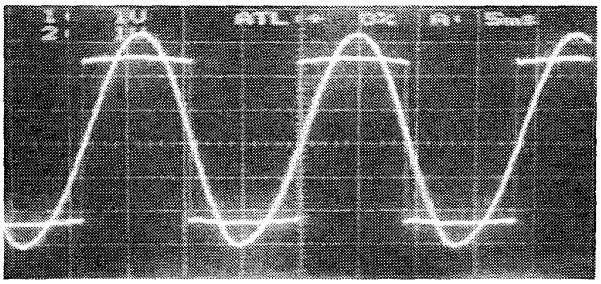

Fig. 9. A square-wave input signal and its fundamental component derived by the proposed PLL (analog implementation)

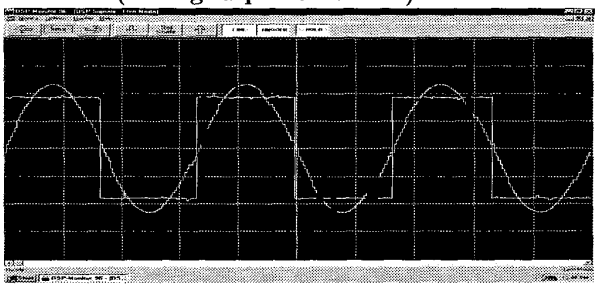

Fig. 10. A square-wave input signal and its fundamental component derived by the proposed PLL (digital implementation)

PLL in locking to the phase of the input signal when it undergoes a step change of one radian. It is observed that this change has been closely followed.

VI. Experimental Results

The proposed PLL is implemented in both analog as well as digital platforms and selected results are presented in this section. A PLL IC of CD4046 is used as VCO to generate sine wave, and the 90-degree phase shift is realized by an integration process. Different signals are applied to the filter and its performance is evaluated. As an example, Fig. 9 shows extracted fundamental component by the PLL when the input signal is a square wave.

The digital set-up includes (a) a signal generator to generate different input signals and (b) a Universal High-Performance (UHP40) controller platform [10]. The heart of the UHP40 is a floating point Texas Instrument Digital Signal Processor (DSP) TMS320C40. The output signal is the fundamental component of the input signal extracted by the PLL. The response of the PLL to a square wave voltage is shown in Fig. 10.

VII. Merits and Potential Applications

The parameters of the PLL readily control its performance e.g. speed in locking to amplitude/phase and the

incurred error while remaining insensitive with regard to exactness of their adjustment. Variations in the values of the controlling parameters K and K_pK_v in the order of 20% of their assigned values have insignificant effect on the desired performance. This can be interpreted as the robustness of the proposed structure with respect to the internal settings.

The following summarizes the main merits of the proposed PLL:

- In contrast to conventional PLLs, the proposed PLL is ideal in the sense that the phase of the output signal is the exact replica of that of the input signal under virtually any condition. In typical cases wherein a step or a ramp change occurs in the phase, the coherence achieved by the present structure is an underestimation of its performance; the phase of the output signal is *equal* to the phase of the input signal. In more complex cases, the degree of the preserved coherence is easily controlled by adjustment of few parameters.
- In addition to the phase-lock feature of the introduced PLL, the output is also amplitude-locked.
- The performance of the structure is highly immune to small variations of its internal structure and high degree of the input pollution content.
- The amplitude and phase are directly estimated and are readily available.

Since the proposed PLL offers more information than a conventional PLL, the range of applications of the introduced PLL is far wider than that of a conventional PLL. The proposed PLL extracts and directly provides the following pieces of information from the input:

- fundamental sinusoidal component of the input; this signal is synchronous with the input and is smooth and noise-free,
- amplitude of the fundamental component of the input, and
- phase angle of the fundamental component of the input; this phase can be adjusted to be its constant phase or total phase.

This information makes the proposed PLL suitable for many applications encountered in diverse areas of engineering. For example, in electrical power engineering the following list presents several potential applications of the PLL [11], [13]:

1. harmonic detection and extraction for measurement as well as active compensation,
2. disturbance detection and extraction,
3. generation of smooth noise-free reference signal synchronous with a distorted and noisy input, useful for synchronous measurement and zero-crossings detection,
4. voltage flicker detection and estimation,
5. peak detection and amplitude demodulation, and
6. phase angle estimation and phase demodulation.

A Power Signal Processor (PSP) is presented in [13]. The PSP is a unified signal processing package capable of providing a large number of signals and information for use in power systems.

VIII. Summary and Conclusion

This paper proposes an enhanced phase-locked loop system based on an alternative structure for phase detection mechanism. Its performance is demonstrated by means of numerical simulations and laboratory implementations. The main features of the proposed PLL are structural simplicity and robustness with respect to internal setting and external noise and disturbances. In contrast to the conventional PLLs, the proposed PLL directly and independently estimates phase angle and amplitude of the desired signal. This feature (1) makes the PLL a more attractive option than the conventional PLLs and (2) widens the range of applications of the PLL.

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