Junhee **Cho**

Graduate Researcher in Quantum Computing and Semiconductor Devices

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Application for Ph.D Program

Dear Prof. Sanghoon Chae,

Who Am I

I am Junhee Cho, currently pursuing a Master's degree in Electrical Engineering at Pohang University of Science and Technology (POSTECH), with an expected graduation in February 2026. I earned my Bachelor's degree in Electrical and Electronics Engineering from Hongik University, graduating with a GPA of 3.96/4.5 and a major GPA of 4.32/4.5. During my undergraduate studies, I researched GaN power devices and circuit simulations. At POSTECH, I am part of the Quantum Computing and Quantum Networks (QCQN) Laboratory, specializing in construction of cryogenic ion trap quantum computing system, which requires highly reliable system design and implementation. As a researcher, I define myself by my resourcefulness, systematically overcoming recurring challenges in the laboratory and achieving the trapping of two ion qubits. My experience in semiconductor design and quantum hardware has equipped me with the expertise to innovate in developing reliable and efficient devices, solidifying my identity as a resourceful and determined researcher.

What I Have Done

My research spans both semiconductor device optimization and quantum hardware development, providing me with a broad and interdisciplinary technical foundation. At Hongik University's Advanced Semiconductor Technology Lab (ASTL), I investigated the integration of depletion-mode AlGaN/GaN MOS-HFETs with clamp circuits to achieve normally-off operation. Using Silvaco-ATLAS, I developed a model that precisely replicated real device behavior, converting it into a SPICE model for circuit simulation. This work resulted in a DC-DC boost converter with 99.5% power conversion efficiency, earning me the Undergraduate Poster Presentation Award at the 30^{th} Korean Conference on Semiconductors.

Building upon this foundation, I shifted my focus toward quantum hardware at POSTECH. At QCQN Laboratory, I spearheaded the design and fabrication of a cryogenic ion trap system, successfully trapping two $^{40}Ca^{+}$ ion qubits for quantum computing research. Through this project, I gained hands-on experience with ion trap fabrication and electrode plating. I also designed stable electrical signal delivery systems, built laser systems with low power fluctuation and tunable frequency, and constructed ultra-high vacuum(UHV) systems. This research was awarded the On-Site Outstanding Poster Award at the 31^{st} Korean Conference on Semiconductors. Currently, I am investigating light-induced charging effects caused by oxide patches on electrodes. Based on surface photovoltage (SPV) theory, I am currently drafting a research paper on photon-induced surface charge dynamics, ultimately aiming to suppress surface-induced stray electric fields and enhance the long-term stability of trapped-ion qubits.

What I Want To Achieve

My previous research experiences have equipped me with a versatile skill set in semiconductor simulation and quantum hardware development. Drawing upon these experiences, I am certain that my acquired expertise will help me become productive within Chae Lab, contributing positively to your research efforts.

Photonic integrated circuits (PICs) have attracted considerable interest because they can address fundamental limitations of conventional electronic interconnects, such as bandwidth, transmission speed, and power consumption. Among various PIC technologies, I am especially interested in microring resonators. While exploring your recent publications, I was particularly interested in your demonstration of reducing insertion loss by integrating graphene-TMD hybrid structures onto SiN microrings, as well as introducing strong electrical tunability and nonlinearity through the

integration of ferroelectric $NbOBr_2$. These results clearly outline a roadmap toward compact, low-loss, and multifunctional photonic devices, and I have become eager to deeply explore and contribute further to this research direction.

In the short term, I hope to acquire comprehensive expertise in device fabrication techniques, characterization methods, and integration processes actively used in your lab, thereby contributing meaningfully to ongoing research projects. For the long term, I aspire to leverage 2D materials and their unique nonlinear optical properties to develop electrically tunable, highly efficient photonic architectures, ultimately enabling advanced functionalities such as chip-scale frequency conversion, optical modulation, and integrated quantum photonic processing. It would truly be an honor to have the opportunity to join your research group and receive your guidance. Thank you very much for your valuable time and consideration, and I sincerely hope to be given this precious opportunity.

Sincerely,
Junhee Cho

Attached: Curriculum Vitae