

Research Experiences

Junhee Cho

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I. Construction of cryogenic ion trap system for quantum computing

Affiliation: Quantum Computing and Quantum Networks (QCQN) laboratory, POSTECH

Supervisor: Prof. Moonjoo Lee

1. Design and fabrication of multi-layer ion trap chip

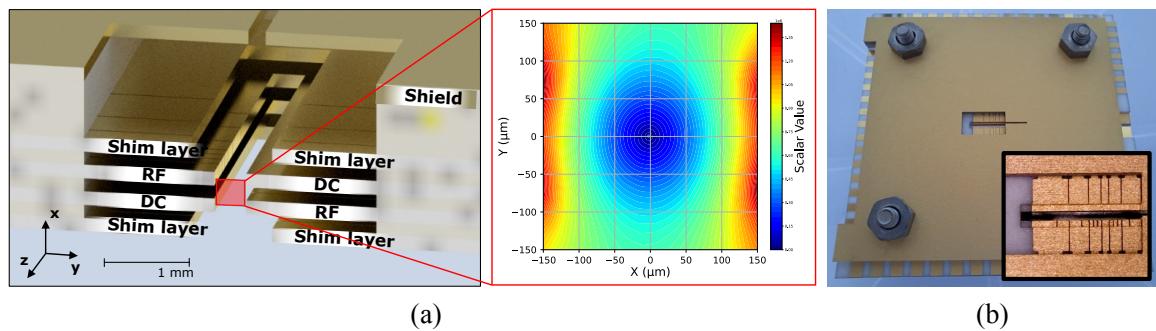


Figure 1: (a) Cross-section view of multi-layer trap and Maxwell simulation result on radial plane and (b) Fabricated multi-layer ion trap

2. Construction of cryogenic ion trap system

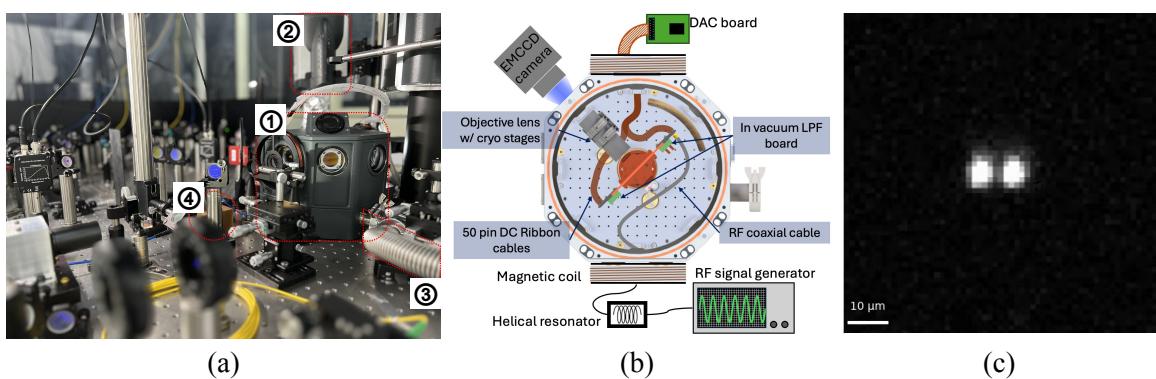


Figure 2: (a) Cross-section view of multi-layer trap and Maxwell simulation result on radial plane and (b) Fabricated multi-layer ion trap

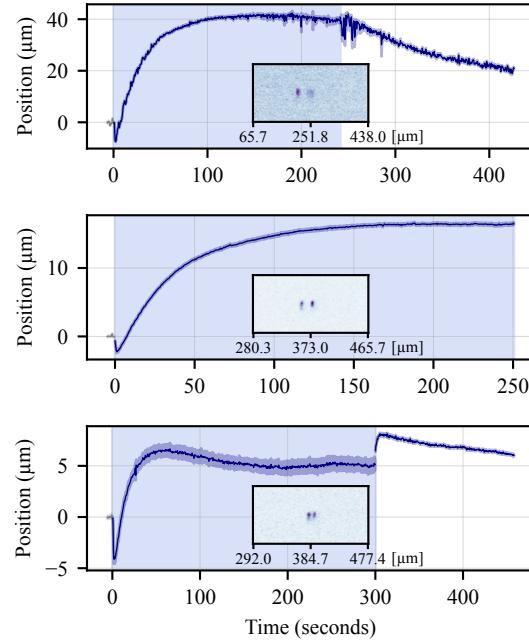


Figure 3: (a) Cross-section view of multi-layer trap and Maxwell simulation result on radial plane and (b) Fabricated multi-layer ion trap

3. Investigation of light-induced charging effect on the trap electrodes

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4. CNN-based detection program for trapped ions

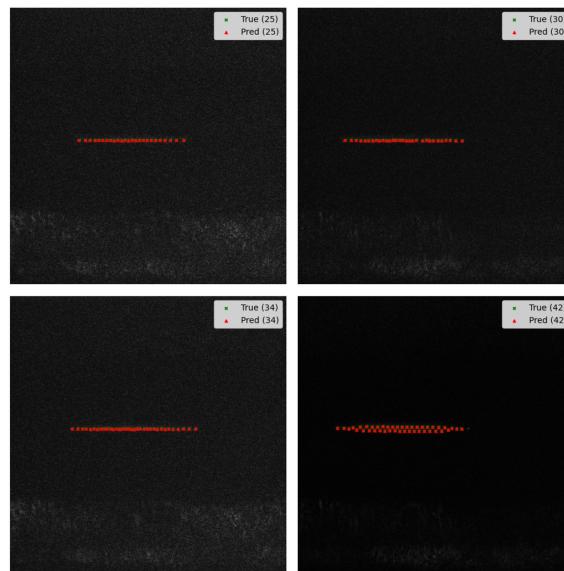


Figure 4: (a) Cross-section view of multi-layer trap and Maxwell simulation result on radial plane and (b) Fabricated multi-layer ion trap

II. Normally-off GaN MOS-HFET

Affiliation: Advanced Semiconductor Technology Lab.(ASTL) laboratory, Hongik University

Supervisor: Prof. Ho-young Cha

1. Modeling normally-on GaN/AlGaN HEMT

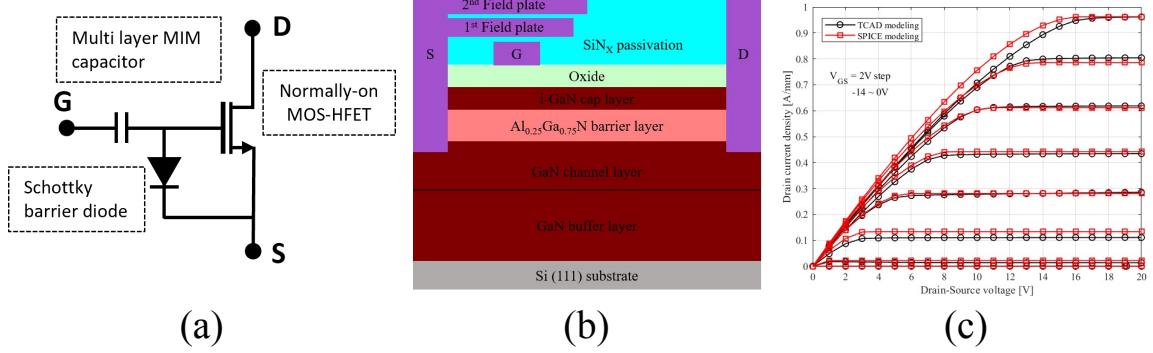


Figure 5: (a) Cross-section view of multi-layer trap and Maxwell simulation result on radial plane and (b) Fabricated multi-layer ion trap

2. Optimization of circuit

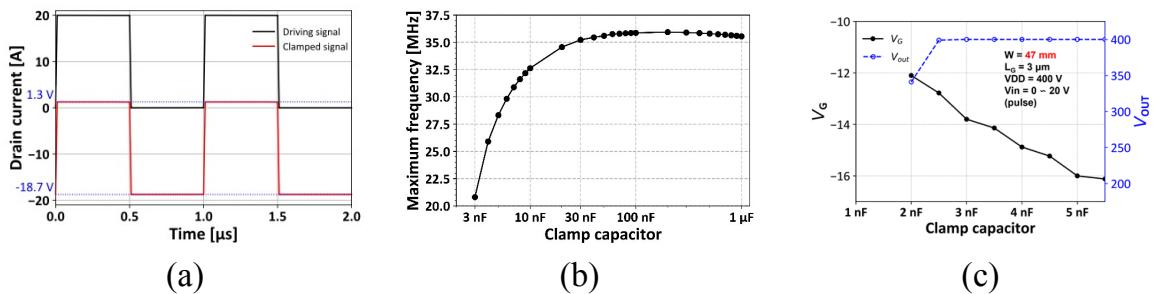


Figure 6: (a) Cross-section view of multi-layer trap and Maxwell simulation result on radial plane and (b) Fabricated multi-layer ion trap

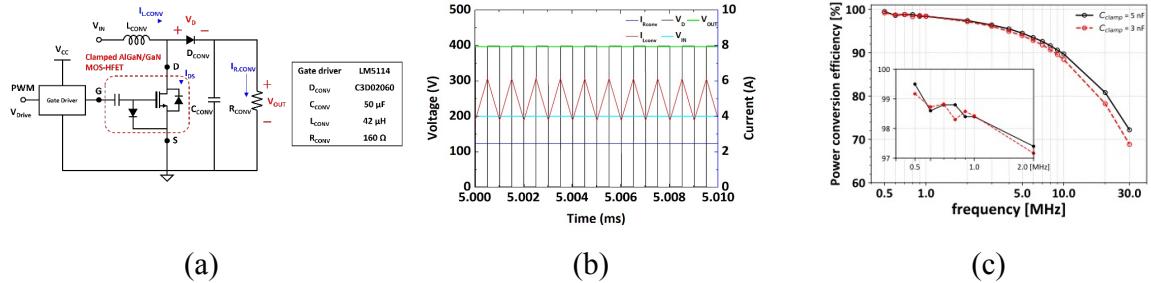


Figure 7: (a) Cross-section view of multi-layer trap and Maxwell simulation result on radial plane and (b) Fabricated multi-layer ion trap

3. DC-DC boost converter circuit

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