

Research Experiences

Junhee Cho

Email: junheecho@postech.ac.kr

I. Construction of cryogenic ion trap system for quantum computing

Affiliation: Quantum Computing and Quantum Networks (QCQN) laboratory, POSTECH

Supervisor: Prof. Moonjoo Lee

1. Design and fabrication of multi-layer ion trap chip

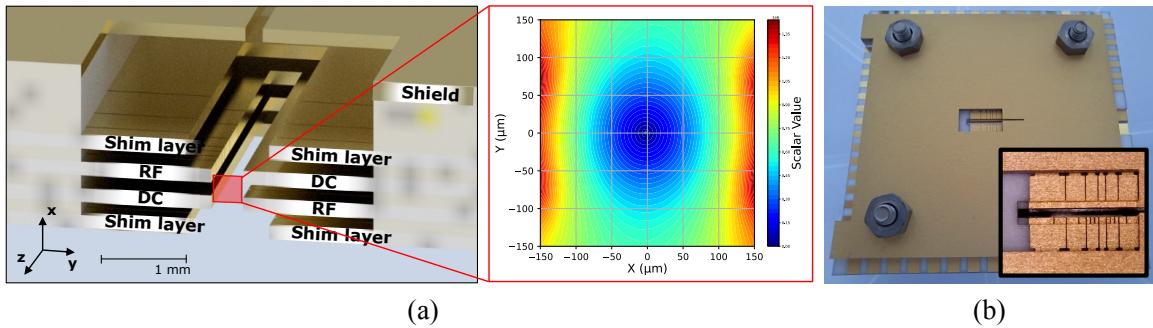


Figure 1: (a) Cross-sectional view of the designed multi-layer ion trap and simulated radial field distribution (Ansys Maxwell 3D). (b) Photograph of the fabricated multi-layer ion trap chip.

- Designed a multi-layer ion trap chip composed of nine stacked layers, including DC/RF layers that provide the trapping potential, shim layers to compensate the principal axes and micromotion, and spacer layers. A shield layer is positioned on the top of the chip to collimate the ablated atomic beam. The DC electrodes are segmented to enable ion shuttling, as depicted in Fig. 1(a, left).
- Simulated the designed structure with $\Omega_{\text{RF}} = 2\pi \cdot 20.26 \text{ MHz}$ and $V_{\text{RF}} = 75 \text{ V}$ using the Ansys Maxwell 3D electrostatic solver, as shown in Fig. 1(a, right). The simulations yield radial secular frequencies of about 3 MHz, in good agreement with the experimentally measured values.
- Laser-cut the alumina substrate using a picosecond laser, deposited a Ti adhesion layer by sputtering, and electroplated Au to form the electrodes. The fabricated multi-layer chip is shown in Fig. 1(b).

2. Construction of cryogenic ion trap system

- Constructed the entire cryogenic ion trap system, as shown in Fig. 2(a). ① is the cryogenic station that contains the ion trap and the cool-down system to reach a temperature of 4 K. ② is the ion fluorescence imaging system with a high-gain EMCCD camera. ③ is the vacuum pumping system for the ultra-high-vacuum (UHV) environment; the bellows in the figure are connected to the turbo and rotary pumps. ④ is the helical resonator connected to an RF signal generator, providing a stable, high quality factor RF delivery system. The remaining part of Fig. 2(a) shows the laser system for ablation loading, ionization, Doppler cooling, and repumping.
- In the laser system, implemented a laser power-lock scheme using a PID control loop on an FPGA board and a high-resolution frequency modulation system. All of these are integrated into the experimental sequence via a home-made PyQt-based user interface (UI).
- In Fig. 2(b), the ion trap is located at the center of the cryogenic station and is enclosed in an oxygen-

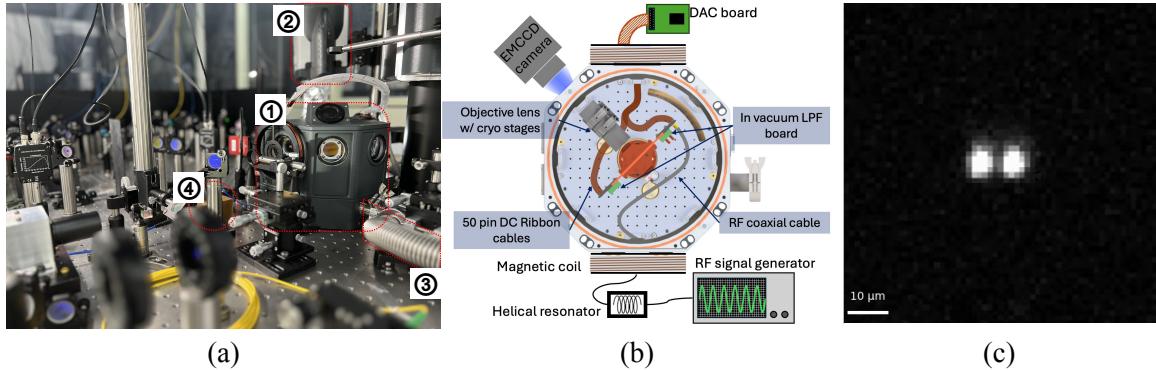


Figure 2: (a) Overall view of the cryogenic ion trap experiment and optical setup. (b) Schematic of the cryostat and the components for trapping ions. (c) Fluorescence image of two trapped ions.

free high thermal conductivity (OFHC) copper chamber with low-pass filter boards mounted on each side. A high-NA (0.38) objective lens is positioned above the trap and mounted on a cryo-compatible XYZ piezo translation stage, and the trap is connected via two DC ribbon cables and an RF coaxial cable. Outside the cryogenic station, a pair of Helmholtz coils is used to generate a 4.2 G magnetic field at the ion position.

- Demonstrated trapping of up to two ions with $(\omega_x, \omega_y) = 2\pi \cdot (2.75, 2.88)$ MHz and performed micromotion compensation by narrowing the Lorentzian linewidth in 397 nm spectroscopy, as shown in Fig. 2(c).
- Presented the progress of the cryogenic ion trap setup and preliminary results at the 2024 Korean Conference on Semiconductors and received an on-site outstanding poster award.

3. Investigation of light-induced charging effects on the trap electrodes

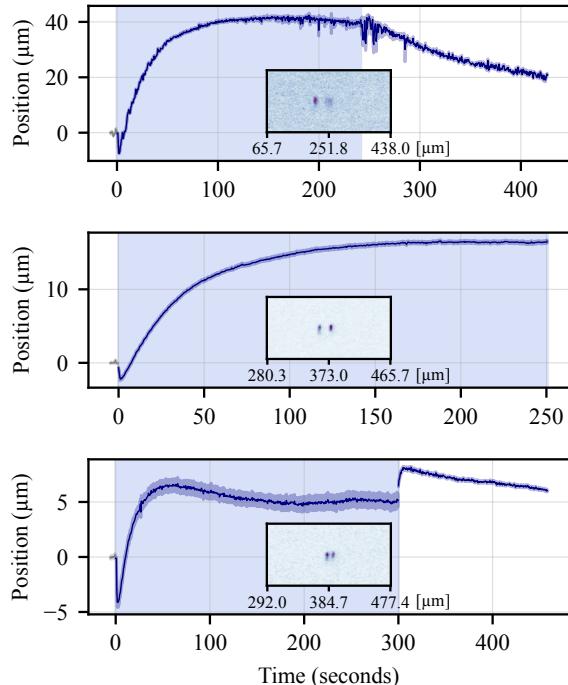


Figure 3: Axial displacement of a single trapped ion used as an in-situ probe of light-induced surface potentials.

- Used a single trapped ion as a sensitive *in-situ* probe of light-induced charging on the trap electrodes by monitoring its time-dependent axial displacement when a focused UV beam was applied to localized oxide patches on the electrode surface.
- Performed time-resolved measurements of the ion position during illumination and in the subsequent dark relaxation period, and systematically varied beam power, exposure time, and illumination geometry to observe how these parameters qualitatively modify the charging and discharging behavior.
- Identified sign-changing charging and discharging effects on the oxide surface from the ion-image data, and compared these features with expectations from a trap-limited surface photovoltaic (SPV) picture.
- Discussed how the observed photo-induced stray fields affect ion stability in our cryogenic ion-trap system, and are currently preparing a manuscript based on these preliminary results.

4. CNN-based detection program for trapped ions

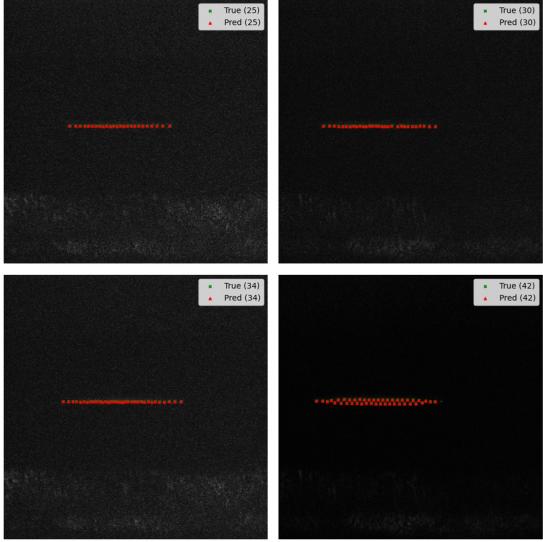


Figure 4: Example EMCCD images of trapped ions and CNN-based detection results for estimating the ion number and positions in real time.

- Developed a CNN-based detection program that takes EMCCD images as input and automatically identifies the number and positions of trapped ions in real time.
- Collected and labeled experimental ion images under varying ion numbers, fluorescence levels, and noise conditions to train and validate the model, and integrated the detection results with the experimental control software for feedback loading.
- Evaluated the model on experimental EMCCD images and confirmed that the predicted ion positions and counts agree with the labeled ground truth over 42 ions, as illustrated in Fig. 4.
- Filed a Korean patent application on November 2025 under the title "Deep learning inference device for ion qubit detection, ion qubit detection system, and ion qubit detection method" based on this CNN detection framework.

II. Normally-off GaN MOS-HFET

Affiliation: Advanced Semiconductor Technology Lab. (ASTL), Hongik University

Supervisor: Prof. Ho-young Cha

1. Modeling of a normally-on GaN/AlGaN HEMT

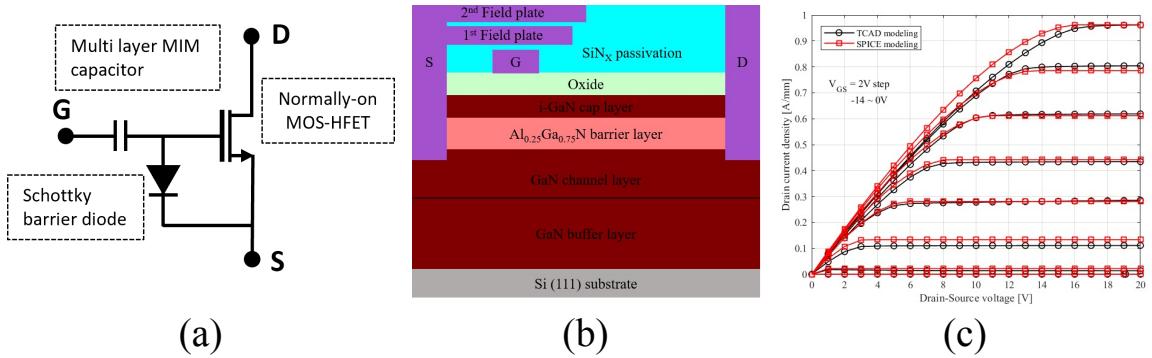


Figure 5: (a) Schematic of AlGaN/GaN MOS-HFET integrated with a clamp circuit, (b) TCAD (Silvaco) model structure, (c) I-V characteristics of TCAD and LTspice models

- Extended previous work in which a clamp circuit was combined with an AlGaN/GaN MOS-HFET to realize normally-off operation while targeting high switching speed and high power-conversion efficiency for high-power, high-frequency applications.
- Modelled an AlGaN/GaN HFET in Silvaco-ATLAS by setting parameters such as unintentional doping, polarization-induced sheet charge, and surface state density so that the simulated device reproduces the measured behaviour (2DEG concentration $4.5 \times 10^{13} \text{ cm}^{-2}$, threshold voltage $\sim -14 \text{ V}$, on-resistance $\sim 12.51 \Omega \cdot \text{mm}$ at $V_G = 0 \text{ V}$).

- Extracted channel-width-dependent I–V characteristics from DC sweep simulations and capacitance characteristics from transient simulations for use in circuit design.
- Converted the TCAD-based device model into a BSIM4-compatible SPICE library so that the GaN MOS-HFET can be used in circuit-level simulations.

2. Optimization of circuit

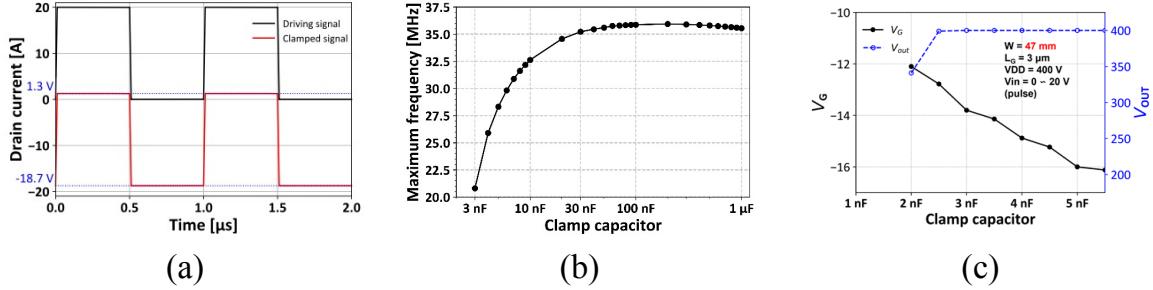


Figure 6: (a) Waveform conversion through the clamp circuit, (b) Clamp capacitance dependent maximum frequency, (c) Clamped low-side peak gate voltage and V_{ds} as a function of clamp capacitance

- Implemented normally-off operation of the D-mode GaN MOS-HFET in LTspice by adding a clamp circuit composed of a GaN Schottky barrier diode and a multilayer metal–insulator–metal capacitor, which shifts the input gate signal by about -18.7 V in peak-to-peak amplitude and enables enhancement-mode operation.
- Chose the clamp capacitance and gate capacitance to achieve high switching speed, and verified that with a clamp capacitance of 30 nF and a channel width of 47 mm the device supports switching frequencies up to 35 MHz.

3. DC-DC boost converter circuit

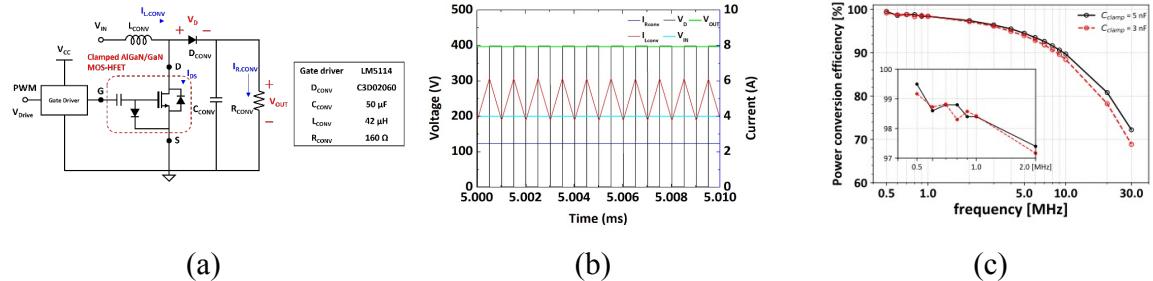


Figure 7: (a) Schematic of DC-DC boost converter, (b) switching waveforms of the boost converter, and (c) Power conversion efficiency versus frequency as a function of clamping capacitance with the device width of 47 mm.

- Verified the operation of the normally-off GaN MOS-HFET in a DC–DC boost converter and showed that, for clamp capacitances larger than 5 nF, the circuit achieves a power-conversion efficiency of up to 99.5% at a switching frequency of 1 MHz.
- Presented the results at the 2022 Conference on Semiconductor Engineering and at the 2023 Korean Conference on Semiconductors, where I received an undergraduate poster presentation award for this work.