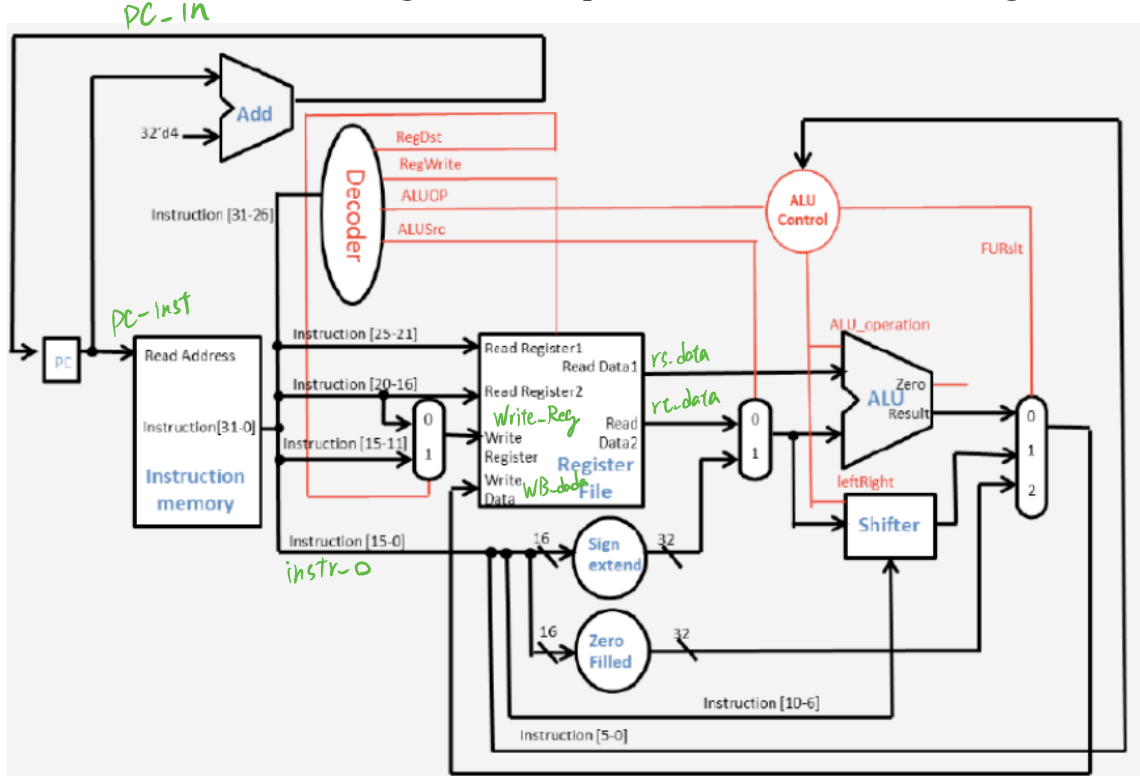# Computer Organization

Architecture diagrams:

Some modification of the diagram in the spec. Wires are noted in the diagram.

Hardware module analysis:

Every instruction executed in four stages (IF, ID, EX, ME, WB). First, instruction is decoded by the program counter and the instruction memory. Instruction is decoded by the instruction decoder. It generates the appropriate control signals, such as the opcode, register select, and ALU operation signals. ALU and shifter compute the values in EX stage. The data memory module receives the memory address and data input from the register file module or the ALU module and output the corresponding data value to the CPU.

Finished part:

I have finished the instruction decoder, the ALU control module, 2-1 MUX, 4-1 MUX, the sign extension module and wire all the modules mentioned above in "Simple_Single_CPU.v".

Problems you met and solutions:

Some problem I encounter is decoder part. I spent some time to find the right instruction op code to right operation. Since I am not familiar with Verilog, I spent some time to find how to use it.

Summary:

I have learned many implementations detail about CPU. It is cool.