**Computer Organization**

**1. The input fields of each pipeline register:**

**IF/ID :**

Pipeline\_IM -input (instr), output (IF\_instr)

**ID/EX:**

Pipeline\_Reg size(11) Pipeline\_Control:

* input {RegWrite, ALUOP, ALUSrc, RegDst, MemRead, MemWrite, MemtoReg},
* output {ID\_RegWrite, ID\_ALUOp, ID\_ALUSrc, ID\_RegDst, ID\_MemRead, ID\_MemWrite, ID\_MemtoReg}

Pipeline\_Reg size(32) Pipeline\_RS:

* input ReadData1
* output ID\_rs\_data

Pipeline\_Reg size(32) Pipeline\_RT:

* input ReadData2
* output ID\_rt\_data

Pipeline\_Reg size(32) Pipeline\_SE:

* input signextend
* ouput ID\_sign\_instr

Pipeline\_Reg size(32) Pipeline\_ZF:

* input zerofilled
* output ID\_zero\_instr

Pipeline\_Reg size(32) Pipeline\_IM\_ID\_EX:

* input IF\_instr
* output ID\_IF\_instr

**EX/MEM**

Pipeline\_Reg size(5) Pipeline\_Control\_EX:

* input {ID\_RegWrite, ID\_MemRead, ID\_MemWrite, ID\_MemtoReg}
* output {EX\_ID\_RegWrite, EX\_ID\_MemRead, EX\_ID\_MemWrite, EX\_ID\_MemtoReg}

Pipeline\_Reg size(32) Pipeline\_Write\_Data:

* input WriteData
* output EX\_Write\_Data

Pipeline\_Reg size(32) Pipeline\_RT\_EX:

* input ID\_rt\_data
* output EX\_ID\_rt\_data

Pipeline\_Reg .size(5) Pipeline\_Write\_reg:

* input WriteReg\_addr
* output EX\_Write\_reg

**MEM/WB**

Pipeline\_Reg size(3) Pipeline\_Control\_MEM:

* input {EX\_ID\_RegWrite, EX\_ID\_MemtoReg}
* output {MEM\_EX\_ID\_RegWrite, MEM\_EX\_ID\_MemtoReg}

Pipeline\_Reg size(32) Pipeline\_Write\_Data\_MEM

* input EX\_Write\_Data
* output MEM\_EX\_Write\_Data

Pipeline\_Reg size(32) Pipeline\_MEM\_Data:

* input DM\_ReadData
* output MEM\_MemReadData

Pipeline\_Reg size(5) Pipeline\_Write\_reg\_MEM:

* input EX\_Write\_reg
* output MEM\_EX\_Write\_reg

**2. Compared with lab4, the extra modules:**

**I have added new module Pipeline register.**

**Pipeline\_Reg.v:** when reset is 0, assign 0 to output, otherwise posedge of clk, assign input to output.

**3. Explain your control signals in sixth cycle (both test patterns CO\_P5\_test\_data1 and CO\_P5\_test\_data2 are needed):**

**Picture:**

|  |  |
| --- | --- |
| **CO\_P5\_test\_data1** | **CO\_P5\_test\_data2** |
| **一張含有 文字, 筆跡, 字型, 白板 的圖片  自動產生的描述** | **一張含有 文字, 筆跡, 白板, 字型 的圖片  自動產生的描述** |

**4. Problems you met and solutions:**

**The pipeline CPU needs additional module compared to the previous lab. I added new module Pipeline\_Reg.v into my work and solve the problem.**

**5. Summary:**

**I modified the single cycle cpu implemented in lab4 to pipeline cpu.**