K JITHENDRA | EE18M087

INDIAN INSTITUTE OF TECHNOLOGY, MADRAS

REGISTRATION NUMBER: 33/EE/20/087

EDUCATION

Program	Institution	CGPA/%	Completion Year	
M.Tech. (Microelectronics and VLSI Design)	IIT Madras	8.0	2020	
B.Tech. (Electronics and Comm. Engg.)	NIT Puducherry	8.64	2017	proof
Intermediate	Sri Vidya Vikas Jr. College Chittoor	97.7	2013	proof
SSC	Jawahar Navodaya Vidyalaya Chittoor	8.4	2011	proof

SCHOLASTIC ACHIEVEMENTS

- Attended India Mobile Congress(IMC), October 2019 where we exhibited Indigenous 5G Testbed Project. proof
- Secured All India Rank of 347 in Gate 2018 - Electronics and Communication Engineering. proof
- Participated in national round of INDO-US Robo League 2015 in Line Following event, conducted by Technophilia Systems and Robotics & Computer Applications Institute of USA, held at IIT Bombay during AAVRITI 2015.proof
- Recipient of Central Sector Scheme of Scholarship for College and University students for the year 2013-14 and received the scholarship for 4 consecutive years from 2013 to 2017. proof
- Secured All India Rank of 14475 in JEE-MAIN 2013. proof
- Secured rank of 2724 in EAMCET 2013. proof

KEY PROJECTS

- **Indigenous 5G Testbed Project** **May 2019 - Present**
  M. Tech Project *C++, Verilog, Vivado, Vivado HLS, MATLAB*
  - Design and implementation of 5G technologies for wireless systems and networks on integrated multi-core programmable SoCs for maximal performance.
  - Designed and Implemented Channel Decoder module for the Uplink Receiver on Xilinx Zynq UltraScale+ RFSoC.

- **Hardware accelerator for Handwritten digit recognition using MNIST database** **January - May 2019**
  Mapping Signal Processing Algorithms to DSP Architectures *C++, Vivado, Vivado HLS*
  - Implemented hardware accelerator for trained feed forward neural network model from KANN library on Xilinx Zynq-7000 SoC, to speed up the classification of handwritten digit images from MNIST database.
  - Achieved a speed improvement by a factor of (1.8).

- **In memory compute engine for Handwritten digit recognition using MNIST database** **January - May 2019**
  Advanced Topics in VLSI *Electric, LTSpice, MATLAB*
  - Designed 4×2 array of 8T SRAM Cells and associated peripheral circuitry that computes multiply and accumulate(MAC) operations for fully connected layer of trained neural network model from KANN library.

- **8 bit carry save multiplier with single stage pipeline** **July - November 2018**
  Digital IC Design *Electric, LTSpice*
  - Designed schematic and layout of signed 8 bit carry save multiplier and then RC extracted netlist of Layout is used for simulations.
  - Achieved 93% improvement in the maximum frequency of operation of the pipelined multiplier when compared with the unpipelined multiplier.

- **Performance evaluation and implementation of SVM Classifier for speech emotion recognition using Berlin database** **January - April 2017**proof
  B. Tech Project *MATLAB*
  - Trained SVM classifier using training data of 4-dimensional feature vectors. The resultant hyperplane was used as a decision boundary to classify the test data.
  - Achieved an average classification accuracy of 72.04%.

PROFESSIONAL EXPERIENCE

- Worked as Associate Software Engineer in Mphasis Pvt. Ltd. *July 2018 - July 2019* proof
  - Worked as a team member in a project to fix vulnerabilities present in Centive, an Incentive Application based on Java Applets.
  - Developed a bank web application that can be used by bank employees to carryout transactions & process customer needs and by customers to use internet banking facilities, as a part of full stack web development training in Java programming language.

COURSE WORK

- Computer architecture
- Mapping signal processing algorithms to DSP architectures
- Digital IC design
- Digital system testing and testable design
- Advanced topics in VLSI
- Pattern recognition proof
- Networks and protocols proof
- VLSI technology
- Semiconductor device modelling
- Microprocessors and microcontrollers proof

LABORATORIES

- VLSI design laboratory proof
- Microprocessors and microcontrollers laboratory proof
- Electronic circuits laboratory proof
- Digital Electronics laboratory proof

TECHNICAL SKILLS

- **Programming languages** : C, C++, Java(intermediate), TCL(novice).
- **HDL** : Verilog.
- **Software packages** : Vivado, Vivado HLS, Cachegrind, LTSpice, Electric, Eclipse, MATLAB, Git, CACTI, Ramulator(novice).

POSITIONS OF RESPONSIBILITY

- Teaching assistant - Computer organization course *August - November 2019*
  - Mentored and evaluated students in the design and implementation of a pipelined CPU that supports RV32I Base Instruction Set of RISC-V ISA.
  - Assisted in creating the testbenches for assignments.
- Teaching assistant - NPTEL - Mapping signal processing algorithms to architectures *August - November 2019* proof
  - Resolved doubts that were asked in the discussion forum of this online course.
- Teaching assistant - Digital systems and Lab *January - May 2019*
  - Coordinated weekly lab sessions and assisted students during these lab sessions.
  - Evaluated lab assignments and exam papers.

EXTRA CURRICULAR ACTIVITIES

- Achieved second position in Volleyball Tournament during schroeter 2018-19, held at IIT madras. proof
- Achieved second position in Chess competition in Annual Sports meet 2016-17, held at NIT Puducherry. proof
- Participated and completed Sports for mental health run (5KM running competition) conducted by Shaastra Sports Tech Summit and Decathlon on October 28, 2018 in IIT Madras. proof

OBJECTIVE

To leverage my VLSI design skills and problem solving abilities to work on challenging problems and contribute towards the development of society.