K JITHENDRA

RTL Design Engineer at Intel, IIT Madras, NIT Puducherry, Ex-Mphasis
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PROFESSIONAL EXPERIENCE(4 YEARS)

- **RTL Design Engineer at Intel Corporation(Power Management(PM) Unit)** **February 2022 - Present**
  Synopsis VCS MX, Verdi, SpyGlass for Lint, CDC and RDC *Verilog, System Verilog, Perl, Make files, Tcsh scripting, Git*
  - Ownership of Dispatcher controller: Sequence and send power related work points to various IPs present in the GPU.
    - Implemented Dispatcher FSM that sends work points to IP driver sequencers parallelly and with standardized commands so that the power management actions on the IPs are made more modular.
    - Implemented unit level tests for this design to check basic functional correctness.
    - Implemented DVFS workpoint handling in Dispatcher along with firmware override capability.
    - Fixed identified bugs and supported validation team throughout the project life cycle.
    - Analyzed equivalence checks for a functional improvement in the dispatcher module to decide whether to proceed with ECO (Engineering change Order).
  - Parameterization of features in PM Unit: Addition or Removal of a feature from the IP with a parameter value.
    - Updated necessary changes in the design flow. Collaborated with Tools and Flows team to make the necessary changes in the used tools and its configurations.
    - Demonstrated POC by generating two different PM Units that have differences in their features.
    - Included it in the latest project to speed up the design timeline of the project.

- **Power Management Architect at Intel Corporation** **July 2020 - February 2022**
  Github, Microsoft Visio, Gitlab, *Multi markdown, UML, Python, Tcsh scripting, Git*
  - Created High level Architecture specification(HAS) for Arbitration logic between Xtensa Micro controller and TAP logic such that the requests from the micro controller are prioritized to maximize overall performance of the micro controller.
  - Created HAS for SVID(Serial voltage ID) protocol related power management that is used by the firmware team to transition its source code base from Foxton assembly code to C++.
  - HBM debug in Data center GPU debug
    - Automated various stages of HBM emulation runs like preprocessing input files, launching emulation runs for various tests in parallel, generating the statistics such as bandwidth, latency and transactions, and generating spreadsheets with summary of the finished emulation runs.
    - Reduced time required to do the above tasks by approximately 10 times.
    - Ran various scenarios of the workloads and generated the summary for these runs.
  - Modelled Adaptive clock modulation and Proportional-Integral-Derivative(PID) controller loop in python which can be used to find the best parameters that generate optimal performance.

- **FPGA Design Engineer at Indigenous 5G Testbed, IIT Madras** **May 2019 - June 2020**
  Vivado, Vivado HLS, Xilinx Zynq UltraScale+ RFSoC, Gitlab *Vivado HLS, C++, Verilog, Git*
  - Designed and tested Channel Decoder module for the Uplink Receiver of 5G NR on Xilinx Zynq UltraScale+ RFSoC.
  - Worked on end to end design flow that includes design using Vivado HLS(High Level Synthesis), Verification using verilog testbenches, synthesis, place and route, and programming FPGA in Xilinx Vivado tool.
  - Integrated Channel decoder into Uplink Receiver and tested the integrated design for functional correctness.
  - Supported integration team during up-revisions of the receiver.

EDUCATION

Program	Institution	CGPA/%	Completion Year
M.Tech. (Microelectronics and VLSI Design)	IIT Madras	8.85	2020
B.Tech. (Electronics and Comm. Engg.)	NIT Puducherry	8.64	2017
Intermediate	Sri Vidya Vikas Jr. College Chittoor	97.7	2013
SSC	Jawahar Navodaya Vidyalaya Chittoor	8.4	2011

KEY PROJECTS

- **Analysis of bigLittle systolic array design using Scale-Sim** **January - June 2020**
  Systems Engineering for Deep Learning *Python, Pytorch*
  - Implemented various big little compute clusters instead of uniform symmetric compute clusters to increase utilization of the compute resources with focus on increase in performance.
  - The concept of big little architectures from CPUs are used to implment in the systolic arrays used for Deep learning/AI accelerators.

- **Hardware accelerator for Handwritten digit recognition using MNIST database** **January - May 2019**
  Mapping Signal Processing Algorithms to DSP Architectures *C++, Vivado, Vivado HLS*
  - Implemented hardware accelerator for trained feed forward neural network model from KANN library on Xilinx Zynq-7000 SoC, to speed up the classification of handwritten digit images from MNIST database.
  - Achieved a speed improvement by a factor of (1.8).

TECHNICAL SKILLS

- **HDL** : Verilog, System Verilog, Vivado HLS (High Level Synthesis).
- **Programming languages** : Python, Perl(intermediate), tcsh scripting, Multi Markdown, C, C++, TCL(novice)
- **Software packages** : Synopsys Verdi, VCS MX, Spyglass, Git, Jira, Vivado, Vivado HLS, LTSpice, Electric, Eclipse, MATLAB, Pytorch

POSITIONS OF RESPONSIBILITY

- Teaching assistant - Mapping signal processing algorithms to architectures course *August 2019 - June 2020*
  - Prepared verilog testbenches and multiple choice questions for assignments.
  - Organized quiz sessions and evaluated assignment submissions and its demonstrations by the students.
  - Documented assignment submission guidelines and procedure for vivado project exporting and importing.

- Teaching assistant - Computer organization course *August - November 2019*
  - Mentored and evaluated students in the design and implementation of a pipelined CPU that supports RV32I Base Instruction Set of RISC-V ISA.
  - Prepared verilog testbenches and questions for assignments.
  - Organized and assisted lab sessions for this course.