K JITHENDRA

RTL DESIGN ENGINEER, INTEL CORPORATION

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PROFESSIONAL EXPERIENCE(3 YEARS AND 10 MONTHS)

- **RTL Design Engineer at Intel Corporation(Power Management(PM) Unit)** **February 2022 - Present**
  Synopsis VCS MX, Verdi and SpyGlass for Lint, CDC and RDC *Verilog, System Verilog, Perl, Make file, TCSH scripting, Git*
  - Owned PM Unit's Dispatcher module that sequences and sends power related work points to various domains and partitions in the SOC. Implemented DVFS handling with firmware override capability that support post silicon fixes for unseen bugs in BattleMage GPU. Fixed bugs and supported validation team till the Tape in.
  - Implemented a central repository for the PM Unit git repository from which multiple PM Units can be generated. Made necessary changes required in the RTL design flow, collaborated with Tools and flows team to make the necessary changes in the tools used. Demonstrated POC of it, made the incremental changes based on the feedback received and included in the latest project to speed up the design time-line of the project.
  - Excellent team member who constantly questions the approach, provides constructive feedback to team members, keeps the workspace active and energetic with active interactions and fun events. Actively grows professional network and improves interpersonal skills.

- **Power Management Architect at Intel Corporation** **July 2020 - February 2022**
  Github, Microsoft Visio *Multi markdown, UML, Pyhton, Tcsh scripting, Git*
  - Created High level Architecture specification(HAS) for Arbitration logic between Xtensa Micro controller and TAP logic such that the requests from the micro controller are prioritized to maximize overall performance of the micro controller.
  - Created HAS for SVID(Serial voltage ID) protocol related power management that is used by the firmware team to transition its source code base from Foxton assembly code to C++.
  - Automated various stages of HBM Emulation runs in Ponte Vechio Server GPU like preprocessing input files, launching emulation runs for various tests at once in parallel, generating the statistics such as bandwidth, latency and transactions by running the corresponding scripts and generating summaries of the finished emulation runs into spreadsheets and thereby reduced corresponding time required to do these tasks by approximately 10 times. Debugged and helped to improve HBM performance by running various scenarios of work loads.
  - Modelled Adaptive clock modulation and PID loop in python that can be used to find the best parameters to generate optimal performance.

- **FPGA Desing Engineer at Indigenous 5G Testbed, IIT Madras** **May 2019 - June 2020**
  Vivado, Vivado HLS, Xilinx Zynq UltraScale+ RFSoC, Gitlab *Vivado HLS, C++, Verilog, Git*
  - Designed and Implemented Channel Decoder module for the Uplink Receiver on Xilinx Zynq UltraScale+ RFSoC.
  - worked on end to end VLSI design flow for Channel Decoder module like module design using HLS, verification, synthesis to place and route, testing on the Xilinx Zync FPGA.
  - Integrated this module into the Uplink Receiver and supported the integration team during the up-revisions of the receiver.

- **Associate Software Engineer at Mphasis Pvt. Ltd** **July 2018 - July 2019**
  Full Stack Web development based on Java *Java, Java applets, Spring MVC*
  - Researched and proposed solutions to the vulnerabilities present in Centive, an incentive application based on Java applets. These proposals are accepted for implementation. Did set up the development environment as it was developed on old software stack based on Java applets.
  - Made regular interactions with the team members and with the topic experts from USA branch to clear the roadblocks and finish setting up the development environment.

- Developed a bank web application that can be used by bank employees to carryout transactions & process customer needs and by customers to use internet banking facilities, as a part of full stack web development training in Java programming language.

EDUCATION

Program	Institution	CGPA/%	Completion Year
M.Tech. (Microelectronics and VLSI Design)	IIT Madras	8.85	2020
B.Tech. (Electronics and Comm. Engg.)	NIT Puducherry	8.64	2017
Intermediate	Sri Vidya Vikas Jr. College Chittoor	97.7	2013
SSC	Jawahar Navodaya Vidyalaya Chittoor	8.4	2011

TECHNICAL SKILLS

- **HDL** : Verilog, System Verilog.
- **Programming languages** : Python, Perl(intermediate), tcsh scripting, Java(intermediate), markdown, C, C++, TCL(novice).
- **Software packages** : Verdi, Spyglass, GIT, Vivado, Vivado HLS, Cachegrind, LTSpice, Electric, Eclipse, MATLAB, CACTI, Ramulator(novice).

SCHOLASTIC ACHIEVEMENTS

- Attended India Mobile Congress(IMC), October 2019 where we exhibited Indigenous 5G Testbed Project.
- Secured All India Rank of 347 in Gate 2018 - Electronics and Communication Engineering.
- Participated in national round of INDO-US Robo League 2015 in Line Following event, conducted by Technophilia Systems and Robotics & Computer Applications Institute of USA, held at IIT Bombay during AAVRITI 2015.
- Recipient of Central Sector Scheme of Scholarship for College and University students for the year 2013-14 and received the scholarship for 4 consecutive years from 2013 to 2017.
- Secured All India Rank of 14475 in JEE-MAIN 2013.
- Secured rank of 2724 in EAMCET 2013.

BACKUP

KEY PROJECTS

- **Scale Sim** **<date> - <date>**
  SysDL *Python, Pytorch*
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- **Hardware accelerator for Handwritten digit recognition using MNIST database** **January - May 2019**
  Mapping Signal Processing Algorithms to DSP Architectures *C++, Vivado, Vivado HLS*
  - Implemented hardware accelerator for trained feed forward neural network model from KANN library on Xilinx Zynq-7000 SoC, to speed up the classification of handwritten digit images from MNIST database.
  - Achieved a speed improvement by a factor of (1.8).

- **In memory compute engine for Handwritten digit recognition using MNIST database** **January - May 2019**
  Advanced Topics in VLSI *Electric, LTSpice, MATLAB*
  - Designed 4×2 array of 8T SRAM Cells and associated peripheral circuitry that computes multiply and accumulate(MAC) operations for fully connected layer of trained neural network model from KANN library.

- **8 bit carry save multiplier with single stage pipeline** **July - November 2018**
  Digital IC Design *Electric, LTSpice*
  - Designed schematic and layout of signed 8 bit carry save multiplier and then RC extracted netlist of Layout is used for simulations.
  - Achieved 93% improvement in the maximum frequency of operation of the pipelined multiplier when compared with the unpipelined multiplier.

- **Performance evaluation and implementation of SVM Classifier for speech emotion recognition using Berlin database** **January - April 2017**
  B. Tech Project *MATLAB*
  - Trained SVM classifier using training data of 4-dimensional feature vectors. The resultant hyperplane was used as a decision boundary to classify the test data.
  - Achieved an average classification accuracy of 72.04%.

COURSE WORK

- Computer architecture
- Mapping signal processing algorithms to DSP architectures
- Digital IC design
- Digital system testing and testable design
- Advanced topics in VLSI
- Pattern recognition
- Networks and protocols
- VLSI technology
- Semiconductor device modelling
- Microprocessors and microcontrollers

LABORATORIES

- VLSI design laboratory
- Microprocessors and microcontrollers laboratory
- Electronic circuits laboratory
- Digital Electronics laboratory

POSITIONS OF RESPONSIBILITY

- Teaching assistant - Computer organization course *August - November 2019*
  - Mentored and evaluated students in the design and implementation of a pipelined CPU that supports RV32I Base Instruction Set of RISC-V ISA.
  - Assisted in creating the testbenches for assignments.

- Teaching assistant - NPTEL - Mapping signal processing algorithms to architectures *August - November 2019*
  - Resolved doubts that were asked in the discussion forum of this online course.

- Teaching assistant - Digital systems and Lab *January - May 2019*
  - Coordinated weekly lab sessions and assisted students during these lab sessions.
  - Evaluated lab assignments and exam papers.

EXTRA CURRICULAR ACTIVITIES

- Achieved second position in Volleyball Tournament during schroeter 2018-19, held at IIT madras.
- Achieved second position in Chess competition in Annual Sports meet 2016-17, held at NIT Puducherry.
- Participated and completed Sports for mental health run (5KM running competition) conducted by Shaastra Sports Tech Summit and Decathlon on October 28, 2018 in IIT Madras.

OBJECTIVE

To leverage my VLSI design skills and problem solving abilities to work on challenging problems and contribute towards the development of society.