K JITHENDRA

RTL Design Engineer at Intel | IIT Madras | NIT Puducherry | Ex-Mphasis | Exp: VLSI-5Y, IT-1Y
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PROFESSIONAL EXPERIENCE — VLSI - 5 YEARS, IT - 1 YEAR

- **RTL Design Engineer - Power Management(PM) Unit, at Intel Corporation** **February 2022 - Present**
  Synopsis VCS MX, Verdi, SpyGlass for Lint, CDC, RDC, and DFT, MS Excel *Verilog, System Verilog, Perl, Make files, ijtag, Git, UPF, IOSF and MC Protocols , Tcsh scripting, CRI intf*
  - **Ownership of Dispatcher controller**
    - Designed Dispatcher FSM which is responsible for controlling the frequency, voltage, & power state changes and DVFS in various sub systems of the SoC.
    - Implemented unit level tests for this design to check basic functional correctness.
    - Checked the design for Lint, CDC, RDC violations during RTL design and made sure that the design is clean form these violations.
    - Supported functional verification team throughout the project life cycle
    - Conducted design and RTL code review meetings for the designed modules.
  - **Ownership of PFET Controller and Fuse Store units**
    - Integrated PG FSM IP into PFET controller unit. Added logic that interacts with Power Muxes and Power Switches. Added new fuses required for the fuse Store Unit.
    - Created test plans for the designed features.
    - Reviewed the designs for code coverage, with a focus on FSM, branch, and other coverages.
    - Simultaneously worked on RTL design of these units for various projects and delivered the designs.
  - **Parameterization of features in PM Unit**
    - Implemented parameter based feature addition automation into the VLSI design flow to easily add or remove a feature into a project just by updating parameter.
    - Integrated it into RTL design signoff flow for it to be used in each project.

- **Architect - SoC Power Management and Reset, at Intel Corporation** **July 2020 - February 2022**
  Github, Microsoft Visio, Gitlab, *Multi markdown, UML, Python, Tcsh scripting, Git*
  - Created High level Architecture specification(HAS) for Arbitration logic between Xtensa Micro controller and TAP logic with more priority given to uC requests to maximize overall performance.
  - Created HAS for SVID(Serial voltage ID) protocol related power management that is used by the firmware team to transition its source code base from Foxton assembly code to C++.
  - Modelled Adaptive clock modulation and Proportional-Integral-Derivative(PID) controller loop in python which can be used to find the best parameters that generate optimal performance.

- **FPGA Design Engineer at Indigenous 5G Testbed, IIT Madras** **May 2019 - June 2020**
  Vivado, Vivado HLS, Xilinx Zynq UltraScale+ RFSoC, Gitlab *Vivado HLS, AMBA AXI, C++, Verilog, Git*
  - Designed and tested Channel Decoder module for the Uplink Receiver of 5G NR on Xilinx Zynq UltraScale+ RFSoC FPGA.
  - Worked on end to end design flow that includes design using Vivado HLS(High Level Synthesis), Verification using verilog testbenches, synthesis, place and route, and programming FPGA in Xilinx Vivado.
  - Integrated Channel decoder into Uplink Receiver and tested the integrated design for functional correctness.
  - Supported integration team during up-revisions of the receiver.

- **Associate Software Engineer at Mphasis Pvt. Ltd** **July 2017 - July 2018**
  Full Stack Web development, Eclipse *Java, Java servlets & applets, Spring MVC, OOPs*
  - Researched and proposed solutions to the vulnerabilities present in Centive, an incentive application based on Java applets. These proposals are accepted for implementation.
  - Developed a basic bank web application that can be used by bank employees and customers as per their needs, as part of full stack web development training in Java programming language.

EDUCATION

Program	Institution	CGPA/%	Completion Year
M.Tech. (Microelectronics and VLSI Design)	IIT Madras	8.85	2020
B.Tech. (Electronics and Comm. Engg.)	NIT Puducherry	8.64	2017
Intermediate	Sri Vidya Vikas Jr. College Chittoor	97.7	2013
SSC	Jawahar Navodaya Vidyalaya Chittoor	8.4	2011

TECHNICAL SKILLS

- **HDL** : Verilog, System Verilog, Vivado HLS (High Level Synthesis).
- **Programming languages** : UPF, Python, Perl(intermediate), tcsh scripting, Multi Markdown, C, C++, TCL(novice), UML(Unified Modeling Language), Java(intermediate)
- **Software packages** : Synopsys Verdi, VCS MX, Spyglass, Git, Jira, Vivado, Vivado HLS, LTSpice, Electric, Eclipse, MATLAB, Pytorch, Spring MVC framework
- **Other** : AMBA AXI Protocol, IOSF protocol, Message channel protocol, IJTAG, CRI intf.

KEY PROJECTS

- **Analysis of bigLittle systolic array design using Scale-Sim** **January - June 2020**
  Systems Engineering for Deep Learning course *Python, Pytorch*
  - Implemented various big little compute clusters instead of uniform symmetric compute clusters, in Python, to increase utilization of the compute resources and to increase power to performance ratio for Deep learning applications.
  - The concept of big little architectures from CPUs are used to implement in the systolic arrays used for Deep learning/AI accelerators.

- **Hardware accelerator for Handwritten digit recognition using MNIST database** **January - May 2019**
  Mapping Signal Processing Algorithms to DSP Architectures course *C++, Vivado, Vivado HLS*
  - Implemented hardware accelerator for trained feed forward neural network model from KANN library on Xilinx Zynq-7000 SoC, to speed up the classification of handwritten digit images from MNIST database.
  - Achieved a speed improvement by a factor of (1.8).

POSITIONS OF RESPONSIBILITY

- Teaching assistant - Mapping signal processing algorithms to DSP architectures course *August 2019 - June 2020*
  - Prepared verilog testbenches and multiple choice questions for assignments.
  - Organized quiz sessions and evaluated assignment submissions and its demonstrations by the students.
  - Demonstrated and documented assignment submission guidelines and procedure for vivado project exporting and importing.

EXTRA CURRICULAR AND CO-CURRICULAR ACTIVITIES

- Secured All India Rank of 347 out of 1,25,000 candidates in GATE 2018 - Electronics and Communication Engineering exam.
- Won gold medal in Smash Wars - Volleyball tournament in Intel, held from February to March, 2023. Played as Outside hitter.
- Achieved (9-16)th position, among 260 participants, in Intel India Blitz Chess tournament, 2023.

ADDITIONAL

- **Related Course work**: Systems engineering for deep learning | Computer architecture | Mapping signal processing algorithms to DSP architectures | Advanced topics in VLSI (SRAM and eDRAM)
- **Hobbies**: Volleyball | Gym | Foosball | Sudoku
- **VISA Sponsorship**: Need VISA sponsorship to work outside of India. I am an Indian.