K JITHENDRA

RTL Design Engineer at Intel | IIT Madras | NIT Puducherry | Ex-Mphasis | Exp: VLSI-5.2Y, IT-1Y

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PROFESSIONAL EXPERIENCE — VLSI - 5.2 YEARS, IT - 1 YEAR

- **RTL Design Engineer at Intel Corporation** — **February 2022 - Present**

  Synopsis VCS MX, Verdi, SpyGlass for Lint, CDC, RDC, and DFT, MS Excel — *Verilog, System Verilog, Perl, Make files, ijtag, Git, UPF, IOSF and MC Protocols , Tcsh scripting, CRI intf*

  - Owned 3 IPs in power management unit.
  - Designed FSMs that control the frequency, voltage, power state changes and DVFS of various sub systems in the SOC.
  - Implemented unit level tests for the designs to check functional correctness
  - Delivered RTL with quality by regularly doing RTL quality checks. i.e., Lint, CDC, RDC, Synthesis checks, DFT.
  - Supported functional verification, post silicon validation, Boot bring-up teams regularly with respect to the owned IPs throughout the project life cycle, across multiple projects.
  - Conducted RTL code reviews for the designed modules across the owned modules.
  - Worked on multi clock domain systems and delivered IPs that support clock domain crossing.
  - Worked on multi voltage domain systems and delivered controller units that control the voltage rails
  - Worked on Power multiplexes, power switches to control the power delivery to various voltage domains.
  - Worked on asynchronous resets which are used in the owned IPs.
  - Delivered controllers that control the ramp-up and ramp-down of voltage rails based on the various SOC power states.
  - Added and supported fuses that are used by the IPs that control the configuration of the GPU core.
  - Created test plans for the designed features
  - Reviewed the RTL designs for code coverage using synopsys verdi tool. Done FSM, branch, related code coverages.
  - Regularly maintained the clean code. Identified the unwanted/unused RTL code and cleaned them up.
  - Supported Integration, UPF and DFT teams related to the owned modules.
  - Simultaneously worked on RTL design of the owned units for various projects across integrated, discrete and Data Center GPU cores.
  - Implemented parameter based feature addition into the IPs so that the features can be easily added or removed based on the requirements, with just a parameter change.
  - Automated parameterization of features and included it into the VLSI design flow at pre RTL stage.

- **Architect at Intel Corporation** — **July 2020 - February 2022**

  Github, Microsoft Visio, Gitlab, — *Multi markdown, UML, Python, Tcsh scripting, Git*

  - Created High level Architecture specification(HAS) for arbitration logic, SVID(Serial voltage ID) protocol related power management for discrete GPU.
  - Modelled Adaptive clock modulation(used to control voltage droops) in python which can be used to find the best parameters that generate optimal performance.
  - Reviewed and updated the IO registers that are used for communication between the PM micro controller and other IPs on the SOC for discrete GPU.

- **FPGA Design Engineer at Indigenous 5G Testbed IIT Madras, DOT India** — **May 2019 - June 2020**

  Vivado, Vivado HLS, Xilinx Zynq UltraScale+ RFSoC, Gitlab — *Vivado HLS, AMBA AXI, C++, Verilog, Git*

  - Designed, verified, and tested Channel Decoder IP for the 5G NR uplink receiver on Xilinx FPGA.
  - Worked on end to end design flow that includes design using Vivado HLS(High Level Synthesis), Verification using verilog testbenches, synthesis, place and route, and programming FPGA in Xilinx Vivado.
  - Integrated Channel decoder IP into Uplink Receiver and tested the integrated design for functional correctness.
  - Supported integration team during the project life cycle.

EDUCATION

Program	Institution	CGPA/%	Completion Year
M.Tech. (Microelectronics and VLSI Design)	IIT Madras	8.85	2020
B.Tech. (Electronics and Comm. Engg.)	NIT Puducherry	8.64	2017
Intermediate	Sri Vidya Vikas Jr. College Chittoor	97.7	2013
SSC	Jawahar Navodaya Vidyalaya Chittoor	8.4	2011

TECHNICAL SKILLS

- **HDL** : Verilog, System Verilog, Vivado HLS (High Level Synthesis).
- **Programming languages** : UPF, Python, Perl(intermediate), tcsh scripting, Multi Markdown, C, C++, TCL(novice), UML(Unified Modeling Language), Java(intermediate)
- **Software packages** : Synopsys Verdi, VCS MX, Spyglass, Git, Jira, Vivado, Vivado HLS, LTSpice, Electric, Eclipse, MATLAB, Pytorch, Spring MVC framework
- **Other** : AMBA AXI Protocol, IOSF protocol, Message channel protocol, IJTAG, CRI intf.

KEY PROJECTS

- **Analysis of bigLittle systolic array design using Scale-Sim** **January - June 2020**
  Systems Engineering for Deep Learning course *Python, Pytorch*
  - Implemented various big little compute clusters instead of uniform symmetric compute clusters, in Python, to increase utilization of the compute resources and to increase power to performance ratio for Deep learning applications.
  - The concept of big little architectures from CPUs are used to implement in the systolic arrays used for Deep learning/AI accelerators.

- **Hardware accelerator for Handwritten digit recognition using MNIST database** **January - May 2019**
  Mapping Signal Processing Algorithms to DSP Architectures course *C++, Vivado, Vivado HLS*
  - Implemented hardware accelerator for trained feed forward neural network model from KANN library on Xilinx Zynq-7000 SoC, to speed up the classification of handwritten digit images from MNIST database.
  - Achieved a speed improvement by a factor of (1.8).

POSITIONS OF RESPONSIBILITY

- Teaching assistant - Mapping signal processing algorithms to DSP architectures course *August 2019 - June 2020*
  - Prepared verilog testbenches and multiple choice questions for assignments.
  - Organized quiz sessions and evaluated assignment submissions and its demonstrations by the students.
  - Demonstrated and documented assignment submission guidelines and procedure for vivado project exporting and importing.

EXTRA CURRICULAR AND CO-CURRICULAR ACTIVITIES

- Secured All India Rank of 347 out of 1,25,000 candidates in GATE 2018 - Electronics and Communication Engineering exam.
- Won gold medal in Smash Wars - Volleyball tournament in Intel, held from February to March, 2023. Played as Outside hitter.
- Achieved (9-16)th position, among 260 participants, in Intel India Blitz Chess tournament, 2023.

ADDITIONAL

- **Related Course work**: Systems engineering for deep learning | Computer architecture | Mapping signal processing algorithms to DSP architectures | Advanced topics in VLSI (SRAM and eDRAM)
- **Hobbies**: Volleyball | Gym | Foosball | Sudoku
- **VISA Sponsorship**: Need VISA sponsorship to work outside of India. I am an Indian.