K JITHENDRA

RTL DESIGN ENGINEER, INTEL CORPORATION

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PROFESSIONAL EXPERIENCE(4 YEARS)

- **RTL Design Engineer at Intel Corporation(Power Management(PM) Unit)** **February 2022 - Present**
  Synopsis VCS MX, Verdi, SpyGlass for Lint, CDC and RDC *Verilog, System Verilog, Perl, Make files, Tcsh scripting, Git*
  - Owned PM Unit's Dispatcher module that sequences and sends power related work points to various domains and partitions in the GPU. Implemented DVFS handling with firmware override capability. Fixed bugs and supported validation team throughout the project life cycle.
  - Implemented Modular IP driver in Dispatcher which makes the addition or removal of an IP easy and the system to be more modular. This make the work point actions by various IPs more parallel and independent.
  - Implemented Parameterization in the PM Unit repository to make it a central repository from which multiple PM units, with different features, can be generated. Made necessary changes required in the RTL design flow, collaborated with Tools and Flows team to make the necessary changes in the tools used. Demonstrated POC of it, made the incremental changes based on the feedback received. Introduced it in the latest project to speed up the design time-line of the project.

- **Power Management Architect at Intel Corporation** **July 2020 - February 2022**
  Github, Microsoft Visio, Gitlab, *Multi markdown, UML, Python, Tcsh scripting, Git*
  - Created High level Architecture specification(HAS) for Arbitration logic between Xtensa Micro controller and TAP logic such that the requests from the micro controller are prioritized to maximize overall performance of the micro controller.
  - Created HAS for SVID(Serial voltage ID) protocol related power management that is used by the firmware team to transition its source code base from Foxton assembly code to C++.
  - Automated various stages of HBM Emulation runs in Data center GPU like preprocessing input files, launching emulation runs for various tests at once in parallel, generating the statistics such as bandwidth, latency and transactions by running the corresponding scripts, and generating summaries of the finished emulation runs into spreadsheets. Reduced corresponding time required to do these tasks by approximately 10 times. Debugged and helped to improve HBM performance by running various scenarios of work loads.
  - Modelled Adaptive clock modulation and Proportional-Integral-Derivative(PID) controller loop in python which can be used to find the best parameters that generate optimal performance.

- **FPGA Design Engineer at Indigenous 5G Testbed, IIT Madras** **May 2019 - June 2020**
  Vivado, Vivado HLS, Xilinx Zynq UltraScale+ RFSoC, Gitlab *Vivado HLS, C++, Verilog, Git*
  - Designed and Implemented Channel Decoder module for the Uplink Receiver on Xilinx Zynq UltraScale+ RFSoC.
  - worked on end to end VLSI design flow for Channel Decoder module like module design using HLS, verification by writing testbenches, synthesis, place and route, and testing on the Xilinx Zync FPGA.
  - Integrated this module into the Uplink Receiver and supported the integration team during the up-revisions of the receiver.

EDUCATION

Program	Institution	CGPA/%	Completion Year
M.Tech. (Microelectronics and VLSI Design)	IIT Madras	8.85	2020
B.Tech. (Electronics and Comm. Engg.)	NIT Puducherry	8.64	2017
Intermediate	Sri Vidya Vikas Jr. College Chittoor	97.7	2013
SSC	Jawahar Navodaya Vidyalaya Chittoor	8.4	2011

KEY PROJECTS

- **Analysis of bigLittle systolic array design using Scale-Sim** **January - June 2020**
  Systems Engineering for Deep Learning *Python, Pytorch*
  - Implemented various big little compute clusters instead of uniform symmetric compute clusters to increase utilization of the compute resources with focus on increase in performance.
  - The concept of big little architectures from CPUs are used to implment in the systolic arrays used for Deep learning/AI accelerators.

- **Hardware accelerator for Handwritten digit recognition using MNIST database** **January - May 2019**
  Mapping Signal Processing Algorithms to DSP Architectures *C++, Vivado, Vivado HLS*
  - Implemented hardware accelerator for trained feed forward neural network model from KANN library on Xilinx Zynq-7000 SoC, to speed up the classification of handwritten digit images from MNIST database.
  - Achieved a speed improvement by a factor of (1.8).

TECHNICAL SKILLS

- **HDL** : Verilog, System Verilog.
- **Programming languages** : Python, Perl(intermediate), tcsh scripting, Java(intermediate), Multi Markdown, C, C++
- **Software packages** : Synopsys Verdi, VCS MX, Spyglass, Git, Vivado, Vivado HLS, LTSpice, Electric, Eclipse, MATLAB, Pytorch, Jira

POSITIONS OF RESPONSIBILITY

- Teaching assistant - Mapping signal processing algorithms to architectures *August 2019 - June 2020*
  - Prepared verilog testbenches and multiple choice questions for assignments.
  - Organized quiz sessions and evaluated assignment submissions and its demonstrations by the students.
  - Documented assignment submission guidelines and procedure for vivado project exporting and importing.

- Teaching assistant - Computer organization course *August - November 2019*
  - Mentored and evaluated students in the design and implementation of a pipelined CPU that supports RV32I Base Instruction Set of RISC-V ISA.
  - Prepared verilog testbenches and questions for assignments.
  - Organized and assisted lab sessions for this course.