**实验报告**

## 基本门电路及门电路综合实验

**一、实验目的**

1. 了解基本门电路的主要用途以及验证它们的逻辑功能。

2. 熟悉数字电路实验箱的使用方法。

3. 掌握利用基本门电路来实现具体电路的方法。

4. 掌握电路变换的方法。

**二、实验仪器及元器件**

1. 数字逻辑与系统设计实验箱。

2. 元器件：与非门74HC00、或非门74HC02、非门74HC04、与门74HC08、或门74HC32、异或门74HC86。

**三、实验原理**

数字电路研究的对象是电路的输入与输出之间的逻辑关系，这些逻辑关系是由逻辑门电路的组合来实现的。门电路是数字电路的基本逻辑单元。要实现基本逻辑运算和复合逻辑运算可用这些单元电路（门电路）进行搭建。门电路以输入量作为条件，输出量作为结果，输入与输出量之间满足某种逻辑关系（即“与、或、非、异或”等关系）。

电路输入与输出量均为二值逻辑的1和0两种逻辑状态。实验中用高低电平分别表示为正逻辑的1和0两种状态。

输出端的1和0两种逻辑状态可用两种方法判定：①将电路的输出端接实验箱的某一位LED，当某一位的LED灯亮时，该位输出高电平，表示逻辑“1”；LED灯不亮时，输出低电平，表示逻辑“0”。②用逻辑笔功能区可以测量输出端的逻辑值。

**四、实验结果和数据处理**

请将实验数据填到表1至表9中，**并将对应的接线情况拍照及运行情况拍视频，在下课前发至老师的微信中。**

表1 74HC00输入输出状态

|  |  |  |  |
| --- | --- | --- | --- |
| 输入端 | | 输出端Y | |
| A | B | LED（亮/灭） | 逻辑状态 |
| 0 | 0 | 亮 | 1 |
| 0 | 1 | 亮 | 1 |
| 1 | 0 | 亮 | 1 |
| 1 | 1 | 灭 | 0 |

表2 74HC02输入输出状态

|  |  |  |  |
| --- | --- | --- | --- |
| 输入端 | | 输出端Y | |
| A | B | LED（亮/灭） | 逻辑状态 |
| 0 | 0 | 亮 | 1 |
| 0 | 1 | 灭 | 0 |
| 1 | 0 | 灭 | 0 |
| 1 | 1 | 灭 | 0 |

表3 74HC04输入输出状态

|  |  |  |
| --- | --- | --- |
| 输入端 | 输出端Y | |
| A | LED（亮/灭） | 逻辑状态 |
| 0 | 亮 | 1 |
| 1 | 灭 | 0 |

表4 74HC08输入输出状态

|  |  |  |  |
| --- | --- | --- | --- |
| 输入端 | | 输出端Y | |
| A | B | LED（亮/灭） | 逻辑状态 |
| 0 | 0 | 灭 | 0 |
| 0 | 1 | 灭 | 0 |
| 1 | 0 | 灭 | 0 |
| 1 | 1 | 亮 | 1 |

表5 74HC32输入输出状态

| 输入端 | | 输出端Y | |
| --- | --- | --- | --- |
| A | B | LED（亮/灭） | 逻辑状态 |
| 0 | 0 | 灭 | 0 |
| 0 | 1 | 亮 | 1 |
| 1 | 0 | 亮 | 1 |
| 1 | 1 | 亮 | 1 |

表6 74HC86输入输出状态

|  |  |  |  |
| --- | --- | --- | --- |
| 输入端 | | 输出端Y | |
| A | B | LED（亮/灭） | 逻辑状态 |
| 0 | 0 | 灭 | 0 |
| 0 | 1 | 亮 | 1 |
| 1 | 0 | 亮 | 1 |
| 1 | 1 | 灭 | 0 |

表7 举重比赛裁判表决电路输入输出状态（方案一）

|  |  |  |  |
| --- | --- | --- | --- |
| 输入端 | | | 输出端 |
| A | B | C | Y |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

表8 举重比赛裁判表决电路输入输出状态（方案二）

|  |  |  |  |
| --- | --- | --- | --- |
| 输入端 | | | 输出端 |
| A | B | C | Y |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

表9 交通灯故障检测电路输出状态

|  |  |  |  |
| --- | --- | --- | --- |
| R | Y | G | Z |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

**五、问题与讨论（记录实验过程中的问题及解决办法）**

## 问题：对试验箱的操作不熟悉，容易出现接错线的问题。

## 解决办法：先将芯片的输入引脚以及输出引脚搞清楚再去操作。组合逻辑电路

**一、实验目的**

1. 了解和掌握编码器的工作原理，并测试其逻辑单元。

2. 了解和掌握译码器的工作原理，并测试其逻辑功能。

3. 了解和掌握数据选择器的工作原理及逻辑功能。

4. 了解和掌握数值比较器的工作原理及如何比较大小。

5. 了解全加器的工作原理及其典型的应用，并验证4位全加器功能。

6. 了解集成数码显示译码器的工作原理及其典型的应用，并实现七段数码管的驱动。

**二、实验仪器及元器件**

1. 数字逻辑与系统设计实验箱。

2. 元器件：8-3编码器74HC148、3-8译码器74HC138、4选1数据选择器74HC153、4位数值比较器74HC85、4位全加器74HC283、集成数码显示译码器74HC4511、4数字共阴极八段显示数码管LN3461Ax。

**三、实验结果和数据处理**

请将实验数据填到表10至表15中，**并将对应的接线拍照及运行情况拍视频，在下课前发至老师的微信中。**

表10 74HC148输入/输出状态

| 控制 | 十进制数字信号输入 | | | | | | | | 二进制数码输出 | | | 状态输出 | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 1 | X | X | X | X | X | X | X | X | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 0 | X | X | X | X | X | X | X | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | X | X | X | X | X | X | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | X | X | X | X | X | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 0 | X | X | X | X | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | X | X | X | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | X | X | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| 0 | X | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |

注：X为任意状态

表11 74HC138输入/输出状态

| 使能输入 | | | 数据输入 | | | 译码输出 | | | | | | | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  | E3 | A2 | A1 | A0 |  |  |  |  |  |  |  |  |
| 1 | X | X | X | X | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| X | 1 | X | X | X | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| X | X | 0 | X | X | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

注：X为任意状态

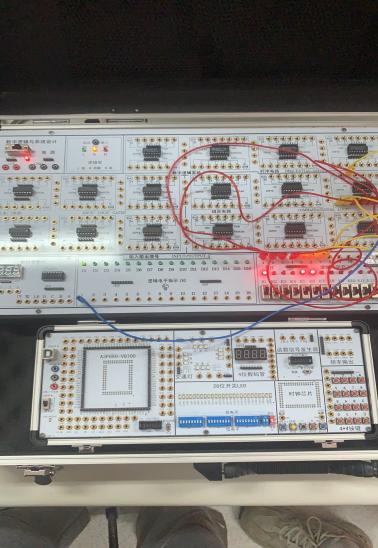
 74HC153接线图

表12 74 HC153输入/输出状态

| 选择输入 | | 数据输入 | | | | 输出使能输入 | 输出 |
| --- | --- | --- | --- | --- | --- | --- | --- |
| S1 | S0 | 1I0 | 1I1 | 1I2 | 1I3 |  | 1Y |
| X | X | X | X | X | X | 1 | 0 |
| 0 | 0 | 0 | X | X | X | 0 | 0 |
| 0 | 0 | 1 | X | X | X | 0 | 1 |
| 1 | 0 | X | X | 0 | X | 0 | 0 |
| 1 | 0 | X | X | 1 | X | 0 | 1 |
| 0 | 1 | X | 0 | X | X | 0 | 0 |
| 0 | 1 | X | 1 | X | X | 0 | 1 |
| 1 | 1 | X | X | X | 0 | 0 | 0 |
| 1 | 1 | X | X | X | 1 | 0 | 1 |

注：X为任意状态

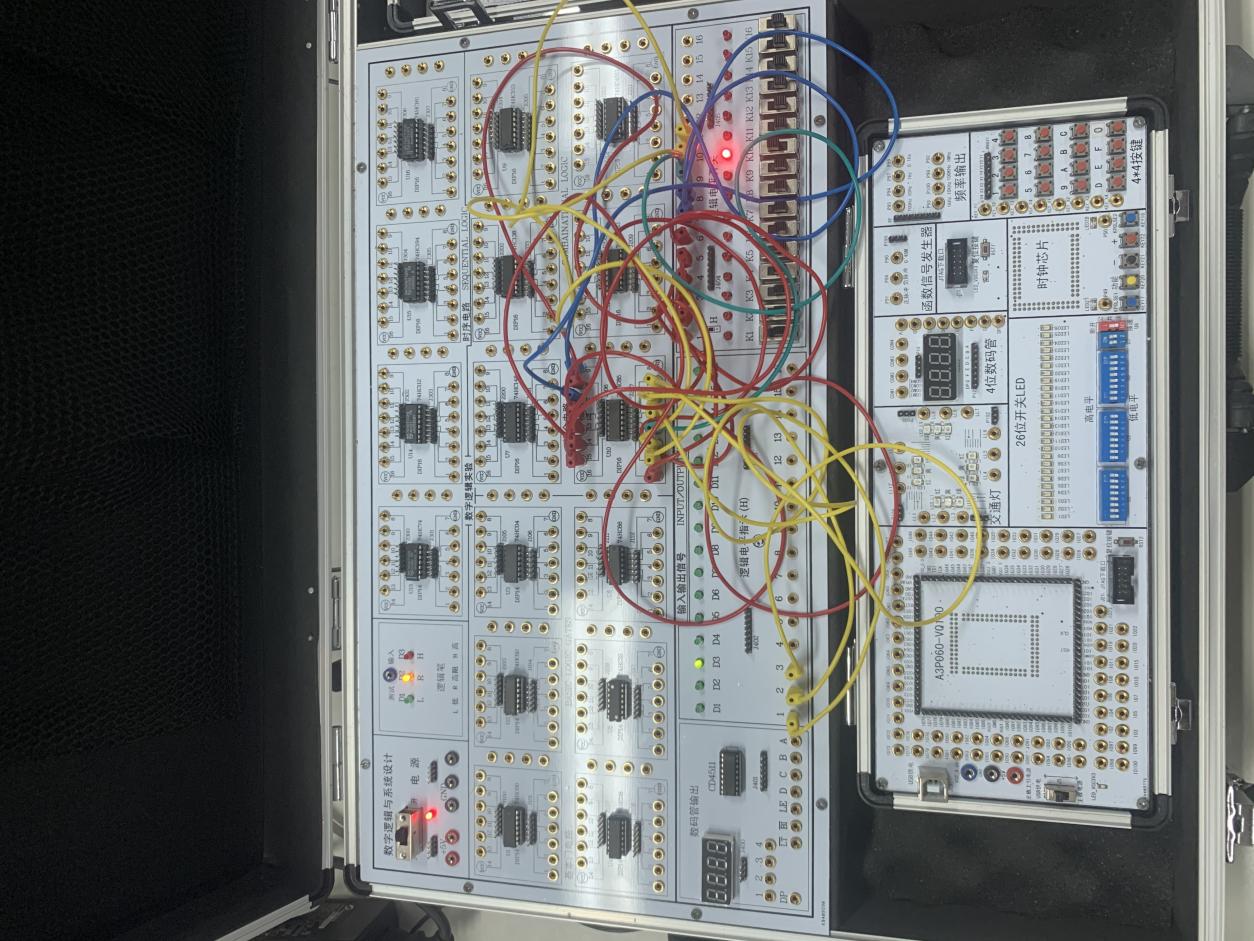
 74HC85

表13 74HC85输入/输出状态

| 比较输入 | | | | | | | | 级联输入 | | | 输出 | | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| A3 | A2 | A1 | A0 | B3 | B2 | B1 | B0 | IA>B | IA=B | IA<B | OA>B | OA=B | OA<B |
| 1 | X | X | X | 0 | X | X | X | X | X | X | 1 | 0 | 0 |
| 0 | X | X | X | 1 | X | X | X | X | X | X | 0 | 0 | 1 |
| 1 | 1 | X | X | 1 | 0 | X | X | X | X | X | 1 | 0 | 0 |
| 0 | 0 | X | X | 0 | 1 | X | X | X | X | X | 0 | 0 | 1 |
| 1 | 0 | 1 | X | 1 | 0 | 0 | X | X | X | X | 1 | 0 | 0 |
| 0 | 0 | 0 | X | 0 | 0 | 1 | X | X | X | X | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | X | X | X | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | X | X | X | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | X | 1 | X | 0 | 1 | 0 |

注：X为任意状态

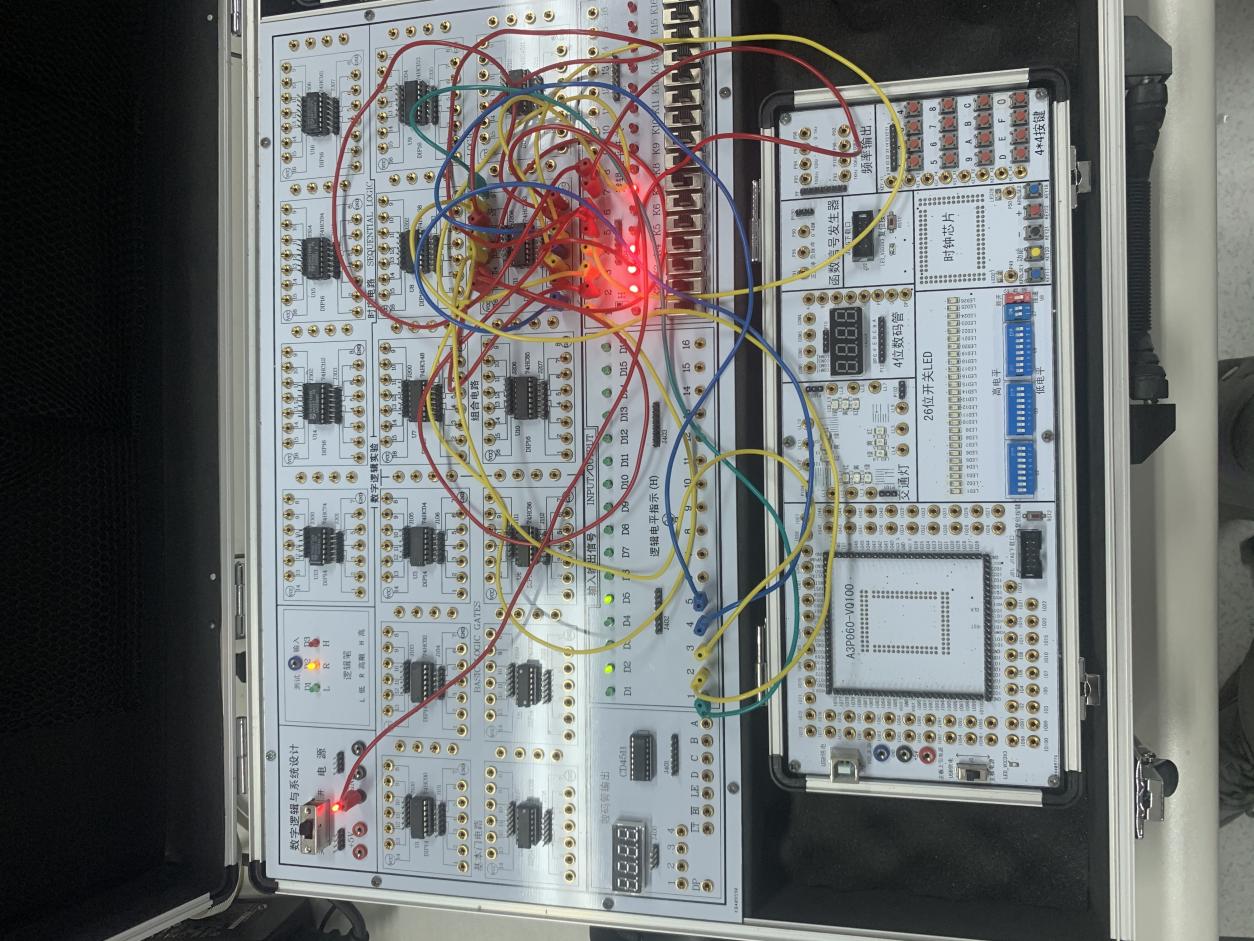
74HC283

表14 74HC283输入/输出状态

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 4位被加数输入 | | | | 4位加数输入 | | | | 输出加法结果和进位 | | | | |
| A4 | A3 | A2 | A1 | B4 | B3 | B2 | B1 | COUT | S4 | S3 | S2 | S1 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |

思考：如增加Cin，输出结果会如何？请自行在表上增加，并验证其他取值的加法结果，填入表中。

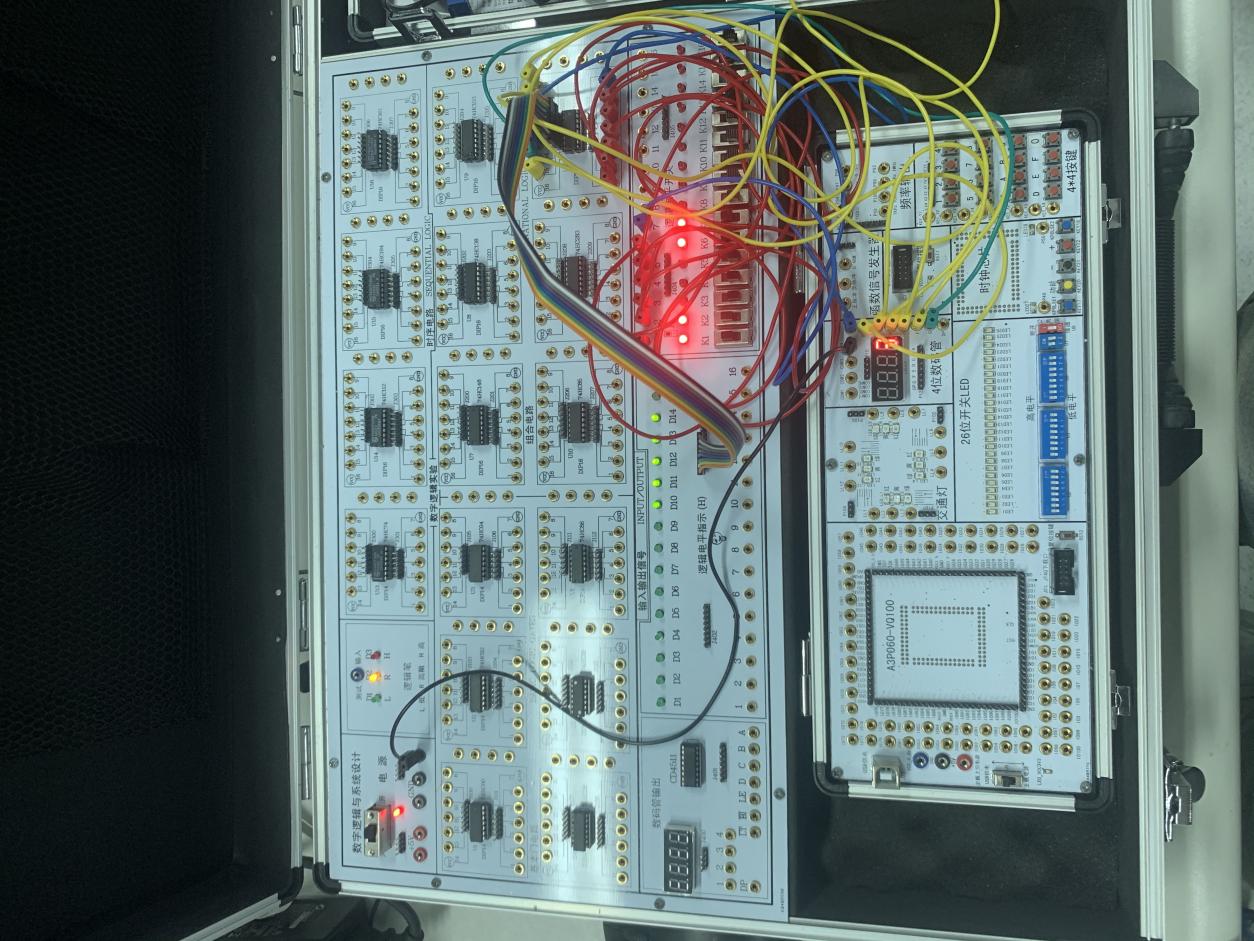
74HC4511

表15 74HC4511输入/输出状态

| 使能输入 | | | 数据输入 | | | | 译码输出 | | | | | | | 字形 |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  | LE | D | C | B | A | a | b | c | d | e | f | g |
| 0 | X | X | X | X | X | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 8 |
| 1 | 0 | X | X | X | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 无显示 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 2 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 3 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 4 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 5 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 6 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 7 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 8 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 9 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 无显示 |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 无显示 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 无显示 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 无显示 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 无显示 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 无显示 |

注：X为任意状态

思考：如果要同时显示4个数字，应如何处理？

答：从芯片的输出端引出三条导线，分别接到其他三个LED数码管的端口。

1. **问题与讨论（记录实验过程中的问题及解决办法）**

问题：实验过程中从芯片引出的导线越来越多，很容易混杂，而且还会存在接触不良导致数码管显示不准确的问题。

解决办法：接线要有条理，并且接线时要检查好是否存好接触不良的问题。

## 时序逻辑电路

**一、实验目的**

1. 掌握D触发器的逻辑功能和测试方法，熟悉74HC74的引脚排列及其功能。

2. 掌握JK触发器的逻辑功能和测试方法，熟悉74HC112的引脚排列及其功能。

3 掌握移位寄存器的工作原理及其应用，熟悉74HC194的逻辑功能及实现各种移位功能的方法。

4 掌握计数电路的工作原理和各控制端的作用，测试并验证74HC161的逻辑功能。

**二、实验仪器及元器件**

1. 数字逻辑与系统设计实验箱。

2. 元器件：双D触发器74HC74、双JK触发器74HC112、双向移位寄存器74HC194、计数器74HC161。

**三、实验结果和数据处理**

请将实验数据填到表16至表19中，**并将对应的接线情况拍照（161的运行情况拍视频），在下课前发至老师的微信中。**

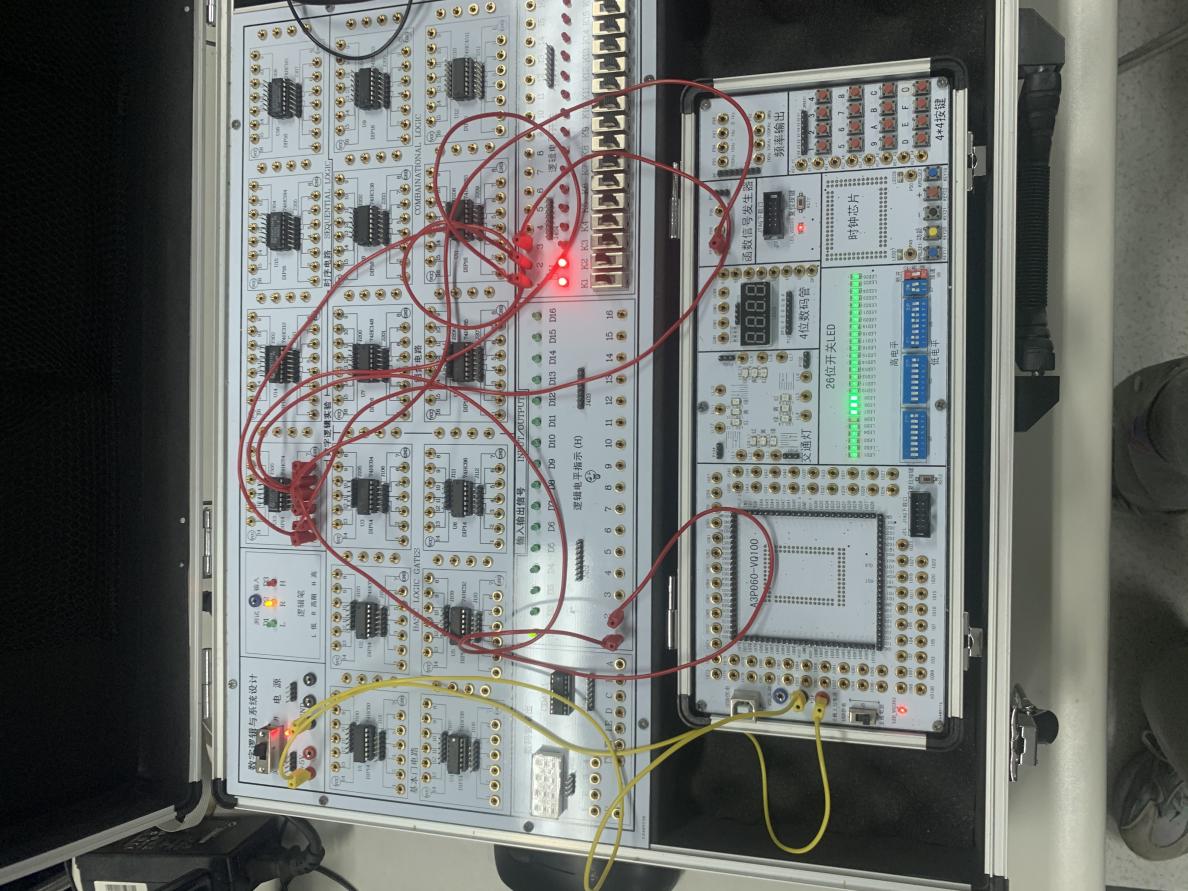
74HC74

表16 D触发器74HC74输入/输出状态

| 输入 | | | | 输出 | | 功能说明 |
| --- | --- | --- | --- | --- | --- | --- |
| 置位输入 | 复位输入 | CP | D | Qn+1 |  |
| 0 | 1 | X | X | 1 | 0 | 异步置1 |
| 1 | 0 | X | X | 0 | 1 | 异步置0 |
| 1 | 1 | ↑ | 0 | 0 | 1 | 同步置0 |
| 1 | 1 | ↑ | 1 | 1 | 0 | 同步置1 |
| 0 | 0 | X | X | 1 | 1 | 未定义 |

注：X为任意状态

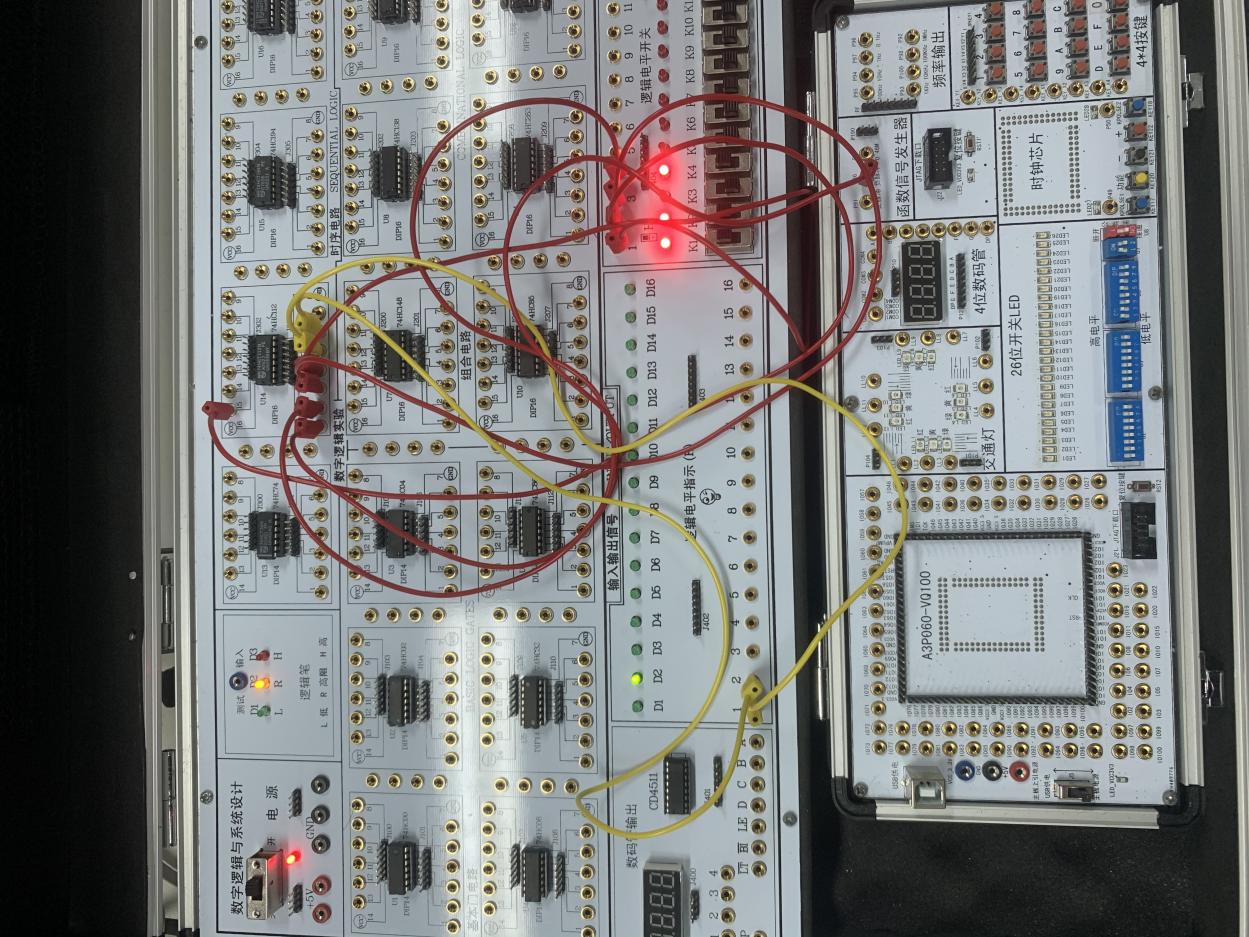
74HC112

表17 JK触发器74HC112输入/输出状态

| 输入 | | | | | 输出 | | 功能说明 |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 置位输入 | 复位输入 |  | 1J | 1K | Qn+1 |  |
| 0 | 1 | X | X | X | 1 | 0 | 异步置1 |
| 1 | 0 | X | X | X | 0 | 1 | 异步置0 |
| 1 | 1 | ↓ | 1 | 1 |  | Qn | 翻转 |
| 1 | 1 | ↓ | 0 | 1 | 0 | 1 | 置0 |
| 1 | 1 | ↓ | 1 | 0 | 1 | 0 | 置1 |
| 0 | 0 | X | X | X | 1 | 0 | 未定义 |
| 1 | 1 | ↓ | 0 | 0 | Qn |  | 保持不变 |

注：X为任意状态

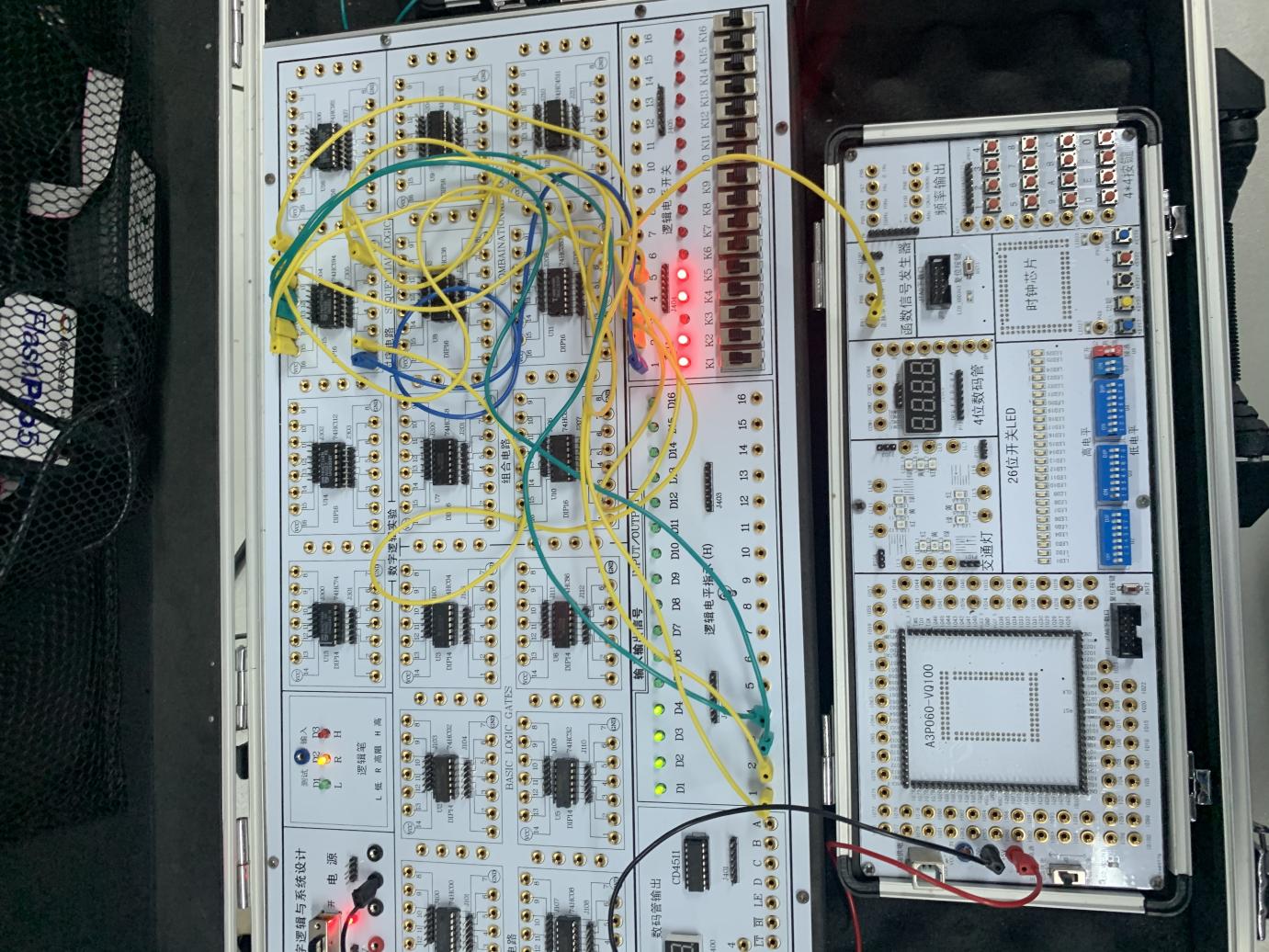
74HC194

表18 74HC194输入/输出状态

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 输入 | | | | | | | | | | 输出 | | | | 功能说明 |
|  | 模式 | | 串行 | | CP | 并行 | | | |
| S1 | S0 | DSR | DSL | D0 | D1 | D2 | D3 | Q0n+1 | Q1n+1 | Q2n+1 | Q3n+1 |
| 0 | X | X | X | X | X | X | X | X | X | 0 | 0 | 0 | 0 | 异步清零 |
| 1 | 1 | 1 | X | X | ↑ | D0 | D1 | D2 | D3 | D0 | D1 | D2 | D3 | 并行输入 |
| 1 | 0 | 0 | X | X | ↑ | X | X | X | X | Q0n | Q1n | Q2n | Q3n | 保持 |
| 1 | 0 | 1 | 0 | X | ↑ | X | X | X | X | 0 | Q0n | Q1n | Q2n | 串行右移输入 |
| 1 | 0 | 1 | 1 | X | ↑ | X | X | X | X | ·1 | Q0n | Q1n | Q2n | 串行右移输入 |
| 1 | 1 | 0 | X | 0 | ↑ | X | X | X | X | Q1n | Q2n | Q3n | 0 | 串行左移输入 |
| 1 | 1 | 0 | X | 1 | ↑ | X | X | X | X | Q1n | Q2n | Q3n | 1 | 串行左移输入 |

注：X为任意状态

思考：输出值跟哪些输入量有关？CP接单个脉冲或连续的时钟信号有何区别？

答：输出值跟、S1 、S0 、DSR、DSL 以及D0、D1、D2、D3有关。CP接单个脉冲时钟信号，那么只能看到当前状态的次态，接连续的时钟信号则会看到一系列的输出结果。

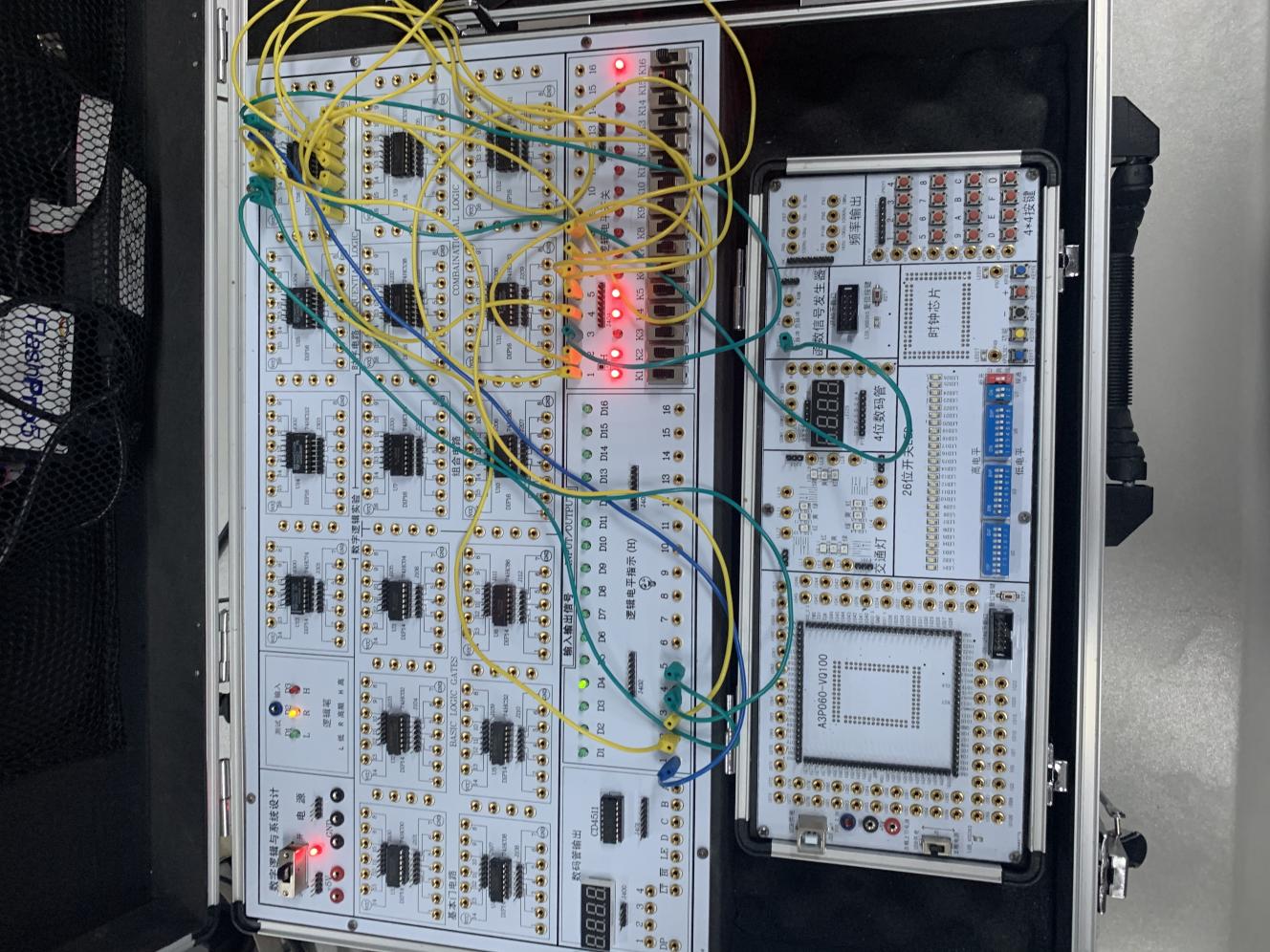
74HC161

表19 74HC161输入/输出状态

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 输入 | | | | | | | | | 输出 | | | | | 功能说明 |
|  | CP | CEP | CET |  | D3 | D2 | D1 | D0 | Q3 | Q2 | Q1 | Q0 | TC |
| 0 | X | X | X | X | X | X | X | X | 0 | 0 | 0 | 0 | 0 | 异步清零 |
| 1 | ↑ | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 并行输 |
| 1 | ↑ | 1 | 1 | 0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | 1 | 并行输入 |
| 1 | ↑ | 1 | 1 | 1 | X | X | X | X | Q3 | Q2 | Q1 | Q0 | 1 | 计数 |
| 1 | X | 0 | X | 1 | X | X | X | X | Q3n | Q2n | Q1n | Q0n | 0 | 保持 |
| 1 | X | X | 0 | 1 | X | X | X | X | Q3n | Q2n | Q1n | Q0n | 0 | 保持 |

注：X为任意状态

思考：接连续的时钟信号中任何一路有何区别？

答：时钟信号的频率会影响一个周期的时间长短。

1. **问题与讨论（记录实验过程中的问题及解决办法）**

暂无记录。

## 组合及时序逻辑综合实验

**一、译码器扩展实验**

设计要求：设计一个电路，通过改变输入，令显示数码管的4个数位轮流显示数字。本实验需要一个3-8译码器74HC138、一个数码显示译码器74HC4511、一个共阴极8段显示数码管LN3461Ax（4位数字轮流显示），电路连接图具体引脚编号请查阅实验指导书。

按照表20的要求，通过拨动输入信号的开关改变输入的状态，观察显示数码管的输出数码，将实验结果填入表中。**将对应的接线拍照及运行情况拍视频，在下课前发至老师的微信中。**

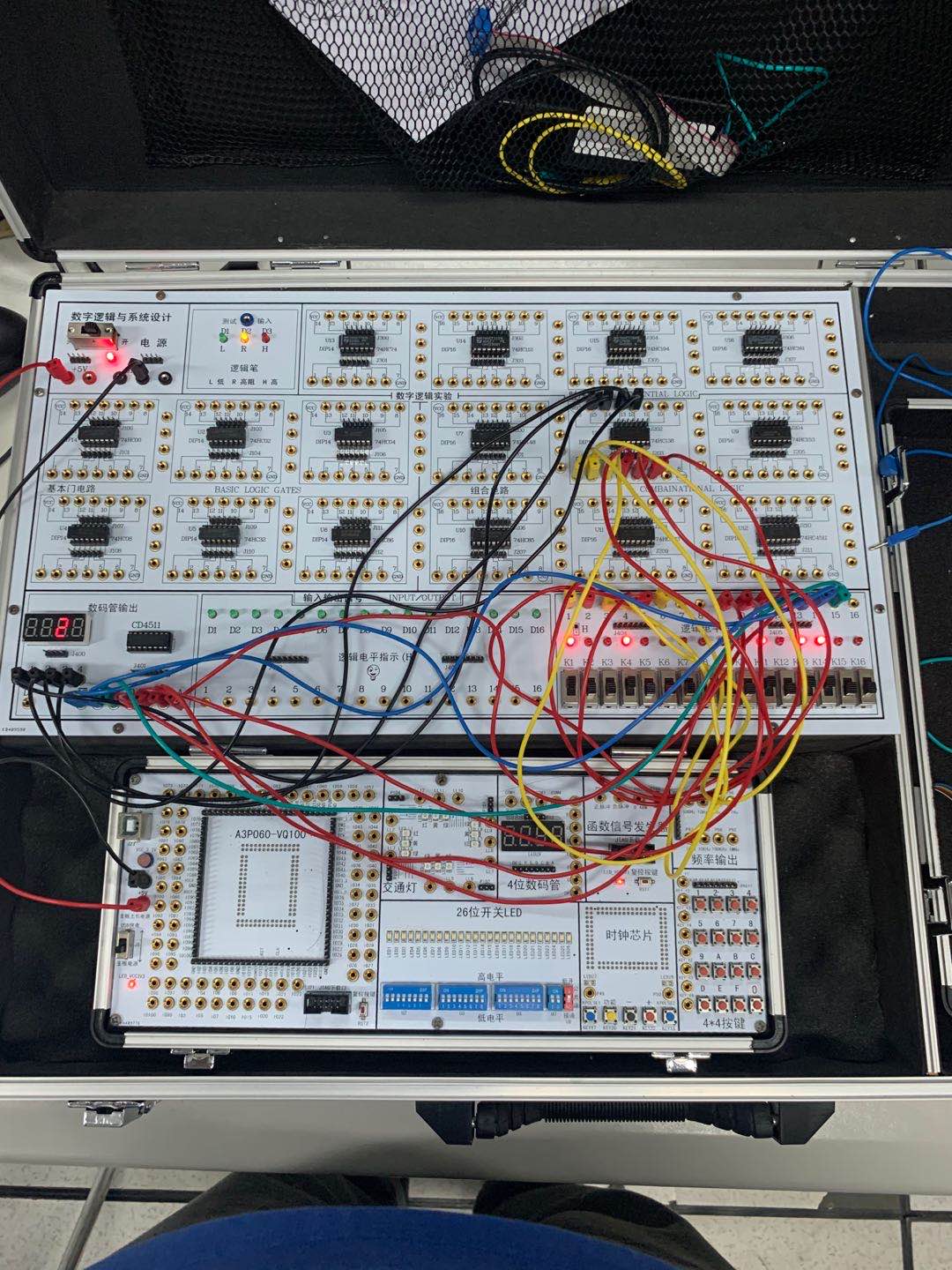


表20 译码器扩展实验结果记录表

| 74HC138使能输入 | | | 74HC138数据输入 | | | 74HC138译码输出 | | | | 数码管显示数字的位置（1~4） |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  | E3 | A2 | A1 | A0 |  |  |  |  |
| 1 | X | X | X | X | X | 0 | 0 | 0 | 0 | 无显示 |
| X | 1 | X | X | X | X | 0 | 0 | 0 | 0 | 无显示 |
| X | X | 0 | X | X | X | 0 | 0 | 0 | 0 | 无显示 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 2 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 3 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 4 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 无显示 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 无显示 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 无显示 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 无显示 |

注：X为任意状态

**二、时序逻辑综合实验**

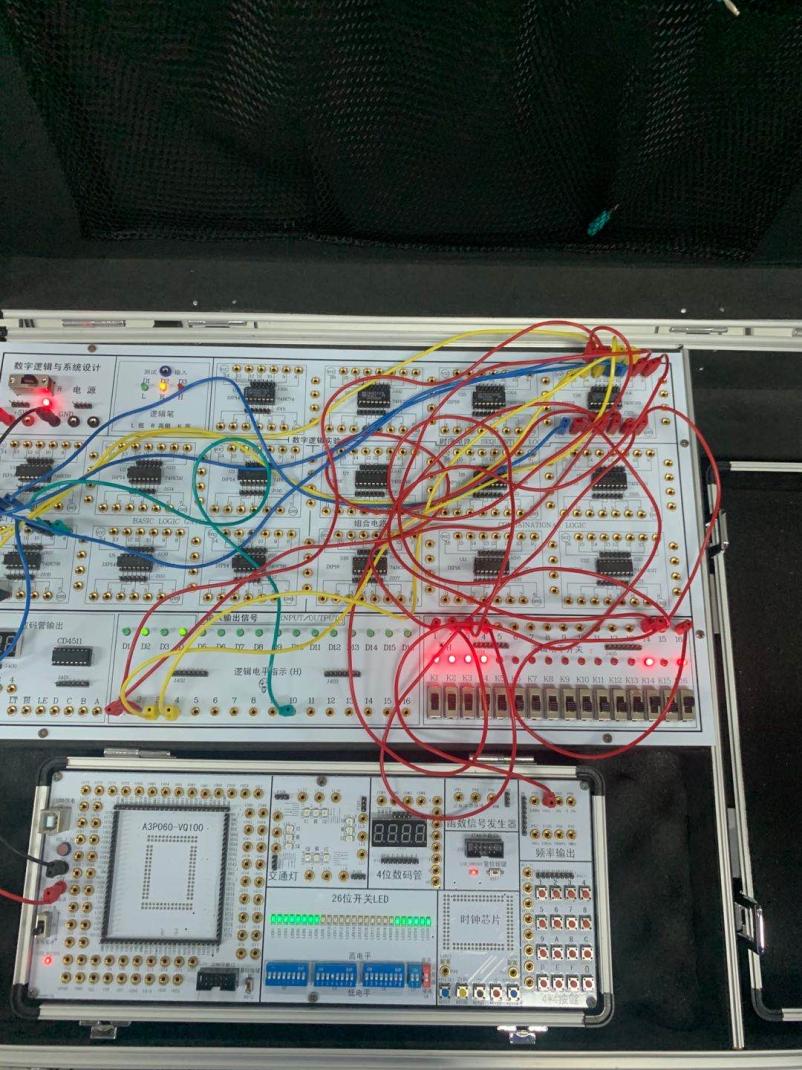
用74HC161设计十二进制计数器，并将计数值显示在显示数码管上（值“10”、“11”可在显示时不做额外处理）。

设计要求：使用4位二进制计数器74HC161设计十二进制计数器，可采用清零法或置数法来实现。画出对应的时序图。**将对应的接线拍照及运行情况拍视频，在下课前发至老师的微信中。**

方法一：利用异步清零方式清零。

图1 用74HC161构造十二进制计数器方法一连线图

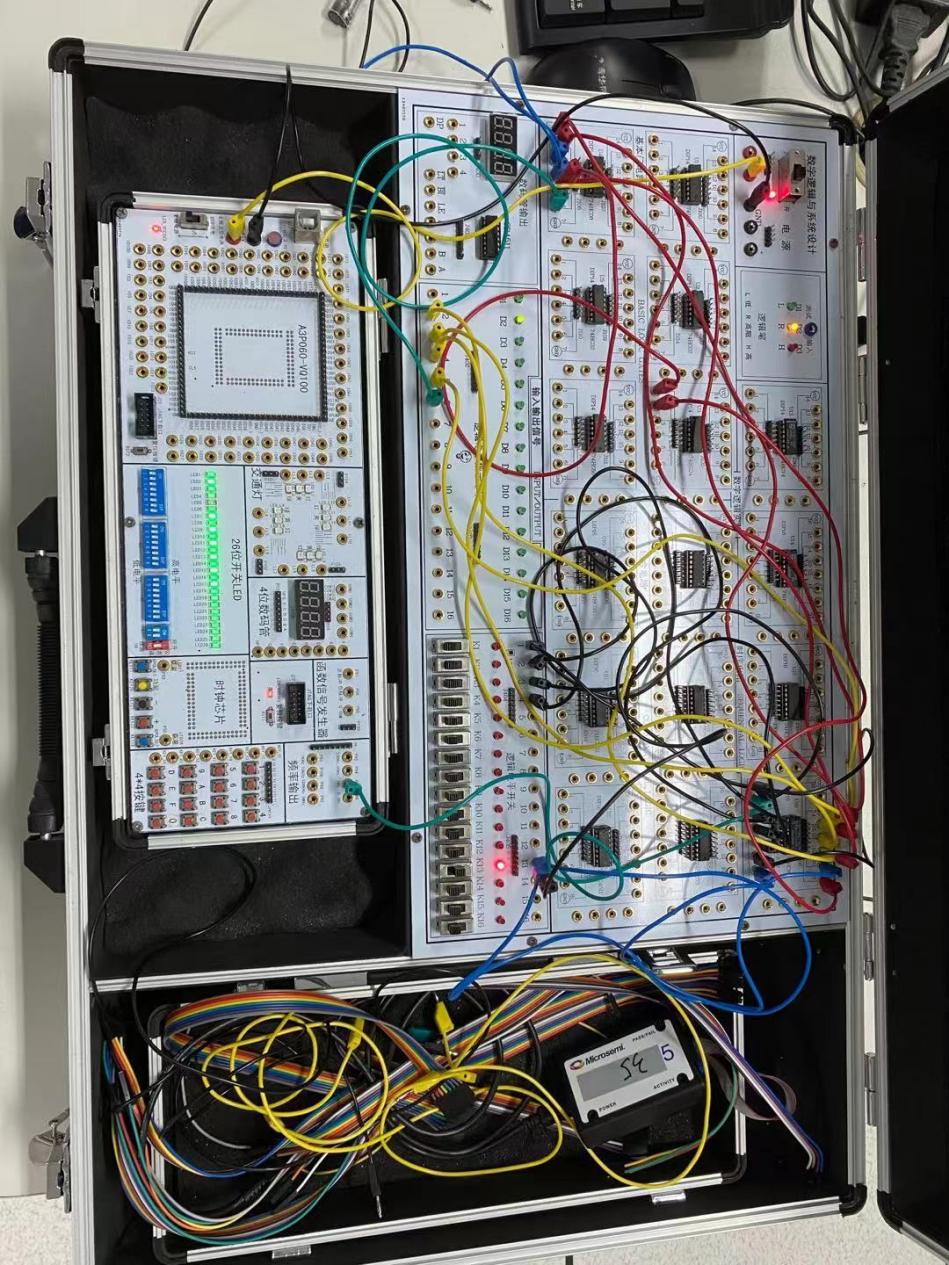




方法二：利用同步置位方式置零。

图2 用74HC161构造十二进制计数器方法二连线图

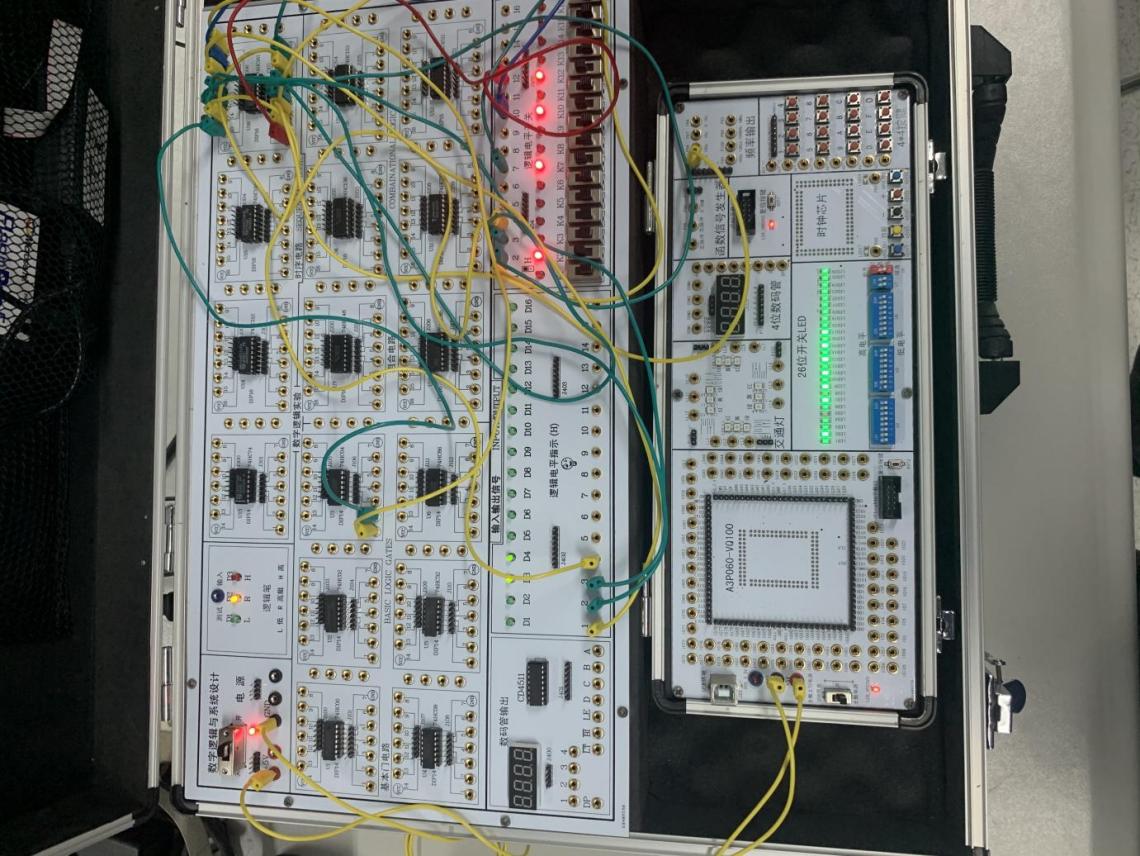




方法三：利用置数法构造。

图3-9 由74HC161构造十二进制计数器方法三连线图





**五、问题与讨论（记录实验过程中的问题及解决办法）**

**无记录。**

**小考核**

请在规定时间内按老师布置的题目要求，完成设计并连线验证，将设计及运行结果记录下来。下课时请提交本实验报告。

