ECE-586

COMPUTER ARCHITECTURE

PROJECT REPORT

MIPS- LITE 5 STAGE PIPELINE SIMULATOR

TEAM 18:

KUMAR DURGA MANOHAR KARNA (912527531) – kkarna@pdx.edu

SAI ROHITH REDDY YERRAM (909940739) – yerram@pdx.edu

NIKHITHA VADNALA (941449738) – vadnala@pdx.edu

1. **Total number of instructions and a breakdown of instruction frequencies for the following instruction types: Arithmetic, Logical, Memory Access, Control Transfer.**

INSTRUCTION TYPE	NUMBER OF INSTRUCTIONS
Arithmetic Instructions	375
Logical Instructions	61
Memory Access Instructions	300
Control Transfer Instructions	175
Total Number of Instructions	911

2. **Final state of program counter, general purpose registers and memory.**

    a. Final State of the program counter is 112.
    b. Final State of general-purpose registers:

GENERAL PURPOSE REGISTERS	FINAL STATE
R0	0
R11	1044
R12	1836
R13	2640
R14	25
R15	-188
R16	213
R17	29
R18	3440
R19	-1
R20	-2
R21	-1
R22	76
R23	3
R24	-1
R25	3

- **Final State of Memory:**

Contents of Memory Address[2400] is : 2

Contents of Memory Address[2404] is : 4

Contents of Memory Address[2408] is : 6

Contents of Memory Address[2412] is : 8

Contents of Memory Address[2416] is : 10

Contents of Memory Address[2420] is : 12

Contents of Memory Address[2424] is : 14

Contents of Memory Address[2428] is : 16

Contents of Memory Address[2432] is : 18

Contents of Memory Address[2436] is : 29

Contents of Memory Address[2440] is : 22

Contents of Memory Address[2444] is : 24

Contents of Memory Address[2448] is : 26

Contents of Memory Address[2452] is : 28

Contents of Memory Address[2456] is : 30

Contents of Memory Address[2460] is : 32

Contents of Memory Address[2464] is : 34

Contents of Memory Address[2468] is : 36

Contents of Memory Address[2472] is : 38

Contents of Memory Address[2476] is : 59

Contents of Memory Address[2480] is : 42

Contents of Memory Address[2484] is : 44

Contents of Memory Address[2488] is : 46

Contents of Memory Address[2492] is : 48

Contents of Memory Address[2496] is : 50

Contents of Memory Address[2500] is : 52

Contents of Memory Address[2504] is : 54

Contents of Memory Address[2508] is : 56

Contents of Memory Address[2512] is : 58

Contents of Memory Address[2516] is : 89

Contents of Memory Address[2520] is : 62

Contents of Memory Address[2524] is : 64

Contents of Memory Address[2528] is : 66

Contents of Memory Address[2532] is : 68

Contents of Memory Address[2536] is : 70

Contents of Memory Address[2540] is : 72

Contents of Memory Address[2544] is : 74

Contents of Memory Address[2548] is : 76

Contents of Memory Address[2552] is : 78

Contents of Memory Address[2556] is : 119

Contents of Memory Address[2560] is : 82

Contents of Memory Address[2564] is : 84

Contents of Memory Address[2568] is : 86

Contents of Memory Address[2572] is : 88

Contents of Memory Address[2576] is : 90

Contents of Memory Address[2580] is : 92

Contents of Memory Address[2584] is : 94

Contents of Memory Address[2588] is : 96

Contents of Memory Address[2592] is : 98

Contents of Memory Address[2596] is : 149

Contents of Memory Address[2600] is : 2

Contents of Memory Address[2604] is : 4

Contents of Memory Address[2608] is : 6

Contents of Memory Address[2612] is : 8

Contents of Memory Address[2616] is : 10

Contents of Memory Address[2620] is : 12

Contents of Memory Address[2624] is : 14

Contents of Memory Address[2628] is : 16

Contents of Memory Address[2632] is : 18

Contents of Memory Address[2636] is : 29

3. Describe the stall conditions in both the "no forwarding" and "forwarding" cases and how long you stalled the pipeline for each stall condition.

a) No-Forwarding:

- If any instruction is dependent and follows right after the producer instruction, then we need two stall cycles in no-forwarding case. Hence, the stall penalty is 2 in such scenario.
- If any instruction is dependent and followed right after one intermediate instruction, then we require one stall cycle. Hence, the stall penalty is 1 in such cases.
- If two instructions are present in between the dependent instruction and producer and if there is no dependency between the instruction, then the stall penalty=0 in such scenario.
- If the instruction is branch and if the jump register instruction is executed and branch is taken. Then, the stall penalty is 2.

b) Forwarding:

- If any instruction is dependent and follows right after the producer instruction, then no stalls are required and therefore the stall penalty is 0 and if producer instruction is load instruction, then we need to stall for one cycle. Hence, in this case the stall penalty is 1.

4. **In the case of "no forwarding", the total number of data hazards and the average stall penalty per hazard.**

   The total number of data hazards: 307
   The total number of stalls: 554
   Average stall penalty per hazard = (Total number of data hazards/total number of stalls).
   = 554/307
   = 1.804

5. **In the case of "forwarding", the number of data hazards which could not be fully eliminated by forwarding.**

   The number of data hazards: 60

6. **Execution time in terms of number of clock cycles for the "no forwarding" and the "forwarding" scenarios.**

   Total number of clock cycles without forwarding : 1707
   Total number of clock cycles with forwarding : 1213

7. **Speedup achieved by "forwarding" as compared to "no forwarding".**

   Speedup achieved = Execution time(no-forwarding) / Execution time(forwarding).
   = 1707/1213
   =1.40725

TRANSCRIPT OUTPUT:

```
# ********** Without Pipeline Statistics **********
# ____________________________________________________________
# Total Number of Instructions : 911
# Arithmetic Instructions : 375
# Logical Instructions : 61
# Memory Access Instructions : 300
# Control Tranfer Instructions : 175
```

```
#
# Final Register Stage:
#
# Program Counter                    :       112
#
# The data of R0              :         0
# The data of R11             :      1044
# The data of R12             :      1836
# The data of R13             :      2640
# The data of R14             :        25
# The data of R15             :      -188
# The data of R16             :       213
# The data of R17             :        29
# The data of R18             :      3440
# The data of R19             :        -1
# The data of R20             :        -2
# The data of R21             :        -1
# The data of R22             :        76
# The data of R23             :         3
# The data of R24             :        -1
# The data of R25             :         3
#
# The number of Branches taken          :       119
# The number of clock cycles            :       911
# Contents of Memory Address[2400] is :         2
# Contents of Memory Address[2404] is :         4
# Contents of Memory Address[2408] is :         6
# Contents of Memory Address[2412] is :         8
# Contents of Memory Address[2416] is :        10
# Contents of Memory Address[2420] is :        12
# Contents of Memory Address[2424] is :        14
# Contents of Memory Address[2428] is :        16
# Contents of Memory Address[2432] is :        18
# Contents of Memory Address[2436] is :        29
# Contents of Memory Address[2440] is :        22
# Contents of Memory Address[2444] is :        24
# Contents of Memory Address[2448] is :        26
# Contents of Memory Address[2452] is :        28
```

Contents of Memory Address[2456] is : 30
Contents of Memory Address[2460] is : 32
Contents of Memory Address[2464] is : 34
Contents of Memory Address[2468] is : 36
Contents of Memory Address[2472] is : 38
Contents of Memory Address[2476] is : 59
Contents of Memory Address[2480] is : 42
Contents of Memory Address[2484] is : 44
Contents of Memory Address[2488] is : 46
Contents of Memory Address[2492] is : 48
Contents of Memory Address[2496] is : 50
Contents of Memory Address[2500] is : 52
Contents of Memory Address[2504] is : 54
Contents of Memory Address[2508] is : 56
Contents of Memory Address[2512] is : 58
Contents of Memory Address[2516] is : 89
Contents of Memory Address[2520] is : 62
Contents of Memory Address[2524] is : 64
Contents of Memory Address[2528] is : 66
Contents of Memory Address[2532] is : 68
Contents of Memory Address[2536] is : 70
Contents of Memory Address[2540] is : 72
Contents of Memory Address[2544] is : 74
Contents of Memory Address[2548] is : 76
Contents of Memory Address[2552] is : 78
Contents of Memory Address[2556] is : 119
Contents of Memory Address[2560] is : 82
Contents of Memory Address[2564] is : 84
Contents of Memory Address[2568] is : 86
Contents of Memory Address[2572] is : 88
Contents of Memory Address[2576] is : 90
Contents of Memory Address[2580] is : 92
Contents of Memory Address[2584] is : 94
Contents of Memory Address[2588] is : 96
Contents of Memory Address[2592] is : 98
Contents of Memory Address[2596] is : 149
Contents of Memory Address[2600] is : 2
Contents of Memory Address[2604] is : 4

```
# Contents of Memory Address[2608] is :         6
# Contents of Memory Address[2612] is :         8
# Contents of Memory Address[2616] is :        10
# Contents of Memory Address[2620] is :        12
# Contents of Memory Address[2624] is :        14
# Contents of Memory Address[2628] is :        16
# Contents of Memory Address[2632] is :        18
# Contents of Memory Address[2636] is :        29
# ____________________________________________________________
# ********Pipelined MIPS without forwarding statistics********
# ____________________________________________________________
# Total number of clock cycles without forwarding :       1707
# Total stall cycles without forwarding          :        554
# Total number of Data Hazards                   :        307
# ____________________________________________________________
# *********Pipelined MIPS with forwarding statistics**********
# ____________________________________________________________
# Total number of clock cycles with forwarding    :       1213
# Total number of stalls with forwarding          :         60
# Total number of Data Hazards                    :         60
# End time: 15:36:08 on Jun 05,2024, Elapsed time: 0:00:02
```