

Roles and Responsibility (Team - 15):

Sai Rohith Reddy Yerram:

- Worked on the development and coding of the data cache.
- Understood the requirements and specifications for the data cache, including its size, associativity, replacement policy, write policies (write-through and write-back).
- Performed functional simulations and tested to validate cache hits, misses, replacements, writebacks, and corner cases.
- Have developed the hardware description code in Verilog to implement the data cache logic.

Bhoomika Kilari:

- Understood why casting out a victim is necessary and got to know about policies to implement this.
- Read about different replacement policies and the need for replacement policies.
- Implemented a 1-bit LRU using the SV constructs successfully.

Vadnala Nikhitha:

- Have understood the requirements and specifications for cache coherence in the system.
- Designed the overall architecture and flow of the MESI protocol implementation.
- Defined the state transitions, cache line states and coherence actions for the protocol.
- Handled the cache line replacements, writebacks and coherence transactions between caches and main memory.
- Integrated the MESI protocol implementation with the overall system.

Kumar Durga Manohar Karna:

- Understood the requirements and specifications for the instruction cache, including its size, associativity and required optimizations.
- Implement the cache controller, cache tag arrays, cache data arrays and associated control signals.
- Perform functional simulations and testing to validate cache hits, misses, and their ratios.
- Identify and fix any bugs or issues discovered during verification