Kai Karadi

650-564-7023 | kaick2@illinois.edu | linkedin.com/in/kai-karadi-a68340226/ | kkaradi.github.io/projects.html

Education

University of Illinois Urbana-Champaign Expected May 2027
B.S. in Computer Engineering *GPA 4.00*
Honors: O. Thomas and Martha S. Purl Scholarship, Illinois Engineering Achievement Scholarship, James Scholar
Coursework: Computer Organization & Design, Adv. VLSI System Design, FPGA Laboratory, Intro to VLSI System Design, ECE Honors Lab, Analog Signal Processing, Data Structures (C++)

Experience

Synchrony Financial Jan 2025 – Present
Full Stack Software Engineering Intern *Champaign, IL*
- Designed an AWS arch. diagram for 100% automated PGP key rotation using AWS Secrets Manager, Lambda, S3
- Secured 1st of 490 participants (116 teams) at Synchrony's international hackathon, engineering an intelligent Agentic AI workflow with Claude Models and AWS Bedrock to redefine Agile project management
- Developed a compliance dashboard using Spring Boot, MySQL, Java, streamlining compliance for 440+ teams

National Center for Supercomputing Applications Feb 2024 – May 2025
SPIN Research Intern *Urbana, IL*
- Engineered a secure personalized AI nutrition chatbot, to incorporate user meal histories with less than 1 second response times, by leveraging ChatGPT Assistants, RAG, few-shot prompting, AWS Lambda, GraphQL in Python
- Led the design of a food recommender engine (2.5 million foods), utilizing embeddings, health indices in Python

University of Illinois Urbana-Champaign Aug 2024 – Dec 2024
ECE Honors Lab Course Assistant *Champaign, IL*
- Mentored honors students in designing analog/digital circuits, such as an Audio Equalizer and Wireless Controller
- Taught students how to use the oscilloscope, wavefunction generator, and hardware debugging principles

University of Illinois Urbana-Champaign Jan 2024 – May 2024
Introduction to Computing Grading Assistant *Champaign IL*
- Graded students on digital logic fundamentals in K-map, Comb/Sequential Logic, FSM, Datapaths, Control Units

Projects

Real-time Xilinx FPGA 3D Renderer | *SystemVerilog, C, Vivado, Vitis* Nov 2024 - Dec 2024
- Designed and implemented an FPGA-based SoC for real-time 3D voxel rendering with user camera inputs
- Integrating a MicroBlaze softcore, custom triangle rasterization FSM, double frame buffer and HDMI video output
- Developed C firmware to accept user input from MAX3421E, allowing for translation/rotation matrix transforms
- Validated the design through comprehensive assert-based simulations and visual verification using bitmap outputs

Superscalar Out of Order RISCV Core | *SystemVerilog, Synopsys DC, Verdi* Mar 2025 - May 2025
- Engineered an out-of-order RISC-V 32IM processor, feat. ERR, GShare perdictor, and a split Load-Store unit
- Secured 5th (50 teams) in design comp with a 1.13 IPC, $33mW$ pwr, 241135 μm^2 area on compression benchmark
- Designed a 2-way superscalar microarchitecture, improved IPC of all benchmarks by $\sim 50\%$ by optimizing a multi-word fetch, enabling simultaneous dispatch, multi-commit ROB, pipelined banked icache, and age order issue
- Verified and designed a 4-way set-associative cache by building a custom golden model, DUT driver, scoreboard

Custom SAT Solving ASIC Tapeout | *SystemVerilog, Synoposis tools, Cadence tools* May 2025 - Present
- Proposed a SAT Solving ASIC based on mesh Network-on-Chip/Boolean Constrain Propogation in a team of 6
- Currenlty early stages: will eventually work on algorithm design, RTL and Physical Design: Plan to tape out

Pulse Weaver DIP Chip Gesture Audio | *Analog Circuit Design, Oscilloscope* Jan 2024 - May 2024
- Developed a gesture based electronic instrument, using capacitive touch, bend sensors, VCA, VCO, and speaker
- Engineered a long-range capacitive hand distance sensor, using 555 timer, op-amps to generate a control voltage
- Verified functionality by employing oscilloscopes, function generators to analyze signal across all sub-circuits

Skills

Languages: SystemVerilog, Verilog RTL, C, C++, Python, Java, JavaScript, SQL, Assembly, HTML/CS,
Dev Tools: Xilinx Vivado, Xilinx Vitis, Synposis DC, Cadence Innovus, Cadence Virtuoso, Git, Docker, VCS, Verdi, Node.js, Bash, Linux, GDB, AWS Lambda, AWS S3, Azure
Libraries: React, Spring Boot, Next.js, Django, Flutter, Jest