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iMCP HTLRBL – SiP LoRa/BLE

LoRa® and Bluetooth Low Energy RF Transceivers System-in-Package

OVERVIEW

iMCP – HTLRBL32L-xx is a Multicomponent Integrated Circuit (MCO) designed to provide a ready-to-use connectivity solution for Internet of Things (IoT) applications. The product merges two widely used IoT technologies, LoRa and Bluetooth Low Energy. The system features a BlueNRG-LP (ARM Cortex M0+ 32bit with BLE radio in a SoC) and Semtech's SX1262 LoRa transceiver. Combining advanced semiconductor packaging technology advantages, integration, and convenience into a single chip.

FEATURES

- Key features
  - LoRaWAN™ compliant
  - Bluetooth Low Energy 5.2 compliant
  - 32-bit ARM Cortex M0+
  - 256 KB flash
  - 64 KB RAM
  - 7 KB ROM
  - TX output power (LoRa): +22 dBm
  - RX sensitivity (LoRa): -132 dBm
  - TX output power (BLE): +7 dBm
  - RX sensitivity level (BLE): -99 dBm @ 1 Mbps, -104 dBm @ 125 kbps (long range)
- Power consumption: 2 uA (DeepSleep with RAM retained)
- Single power supply: 2.7 to 3.6V
- Operating temperature range: -20°C to +75°C
- External antenna
- 13x13x1.08 LGA – 32 pads package
- RF
  - STMicroelectronics BlueNRG-LP
  - Semtech SX1262
- LoRaWAN Frequency plans:
  - EU863-870
  - US902-928
  - AU915-928
  - AS923
  - KR920-923
  - IN865-867
  - RU864-870
  - EU433
  - CN470-510
- Modulation schemes (SX1262):
  - FSK, GFSK, MSK, GMSK and LoRa

INTERFACES

- 1x DMA controller with 8 channels supporting ADC, SPI, I2C, USART and LPUART
- 1x SPI/I2S
- 1x I2C (SMBus/PMBus)
- 1x PDM (digital microphone interface)
- 1x LPUART
- 1x USART (ISO 7816 smartcard mode, IrDA, SPI Master and Modbus)
- 1x independent WDG
- 1x real time clock (RTC)
- 1x independent SysTick
- 1x 16-bit, 6 channel advanced timer
- Up to 19 fast I/Os: 17 of them with wake-up capability
- 12-bit ADC with 5 input channels
- Battery monitoring
- Analog watchdog
- Analog Mic I/F with PGA

APPLICATIONS

- Smart home
- Wireless alarm systems
- Manufacturing
- Agriculture
- Building automation
- Smart metering
- Smart lighting system

SUMMARY

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DOCUMENT INFO

This document provides information about iMCP HTLRBL32L-xx – LoRa® and BLE® System-in-package (SiP) family. There are three main components integrated within the SIP, each with their own characteristics and features. The HTLRBL32L-xx datasheet will provide general information about the integration of the components. If you need more information on each individual feature, you can access their datasheets:

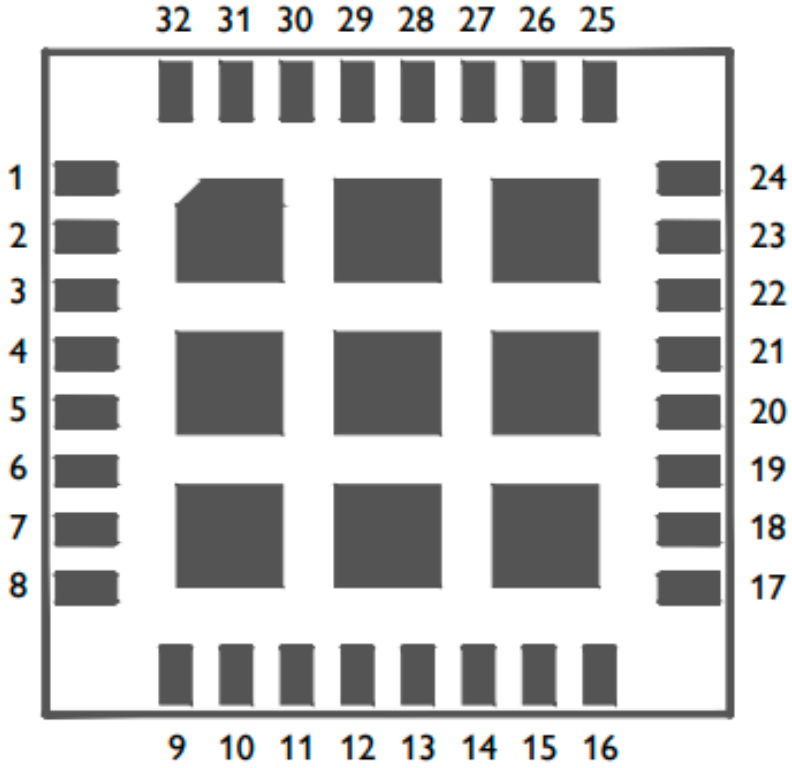
- BlueNRG-LP - MCU.
- SX1262 - LoRa Radio.
- STSAFE-A110 - Hardware Secure Element (HSE).

To find the most recent information access our GitHub page.

1 PIN DIAGRAM

This document section provides a detailed pin diagram, illustrating the configuration and connectivity of the pins on the MCO.

Figure 1: Pin Diagram



1.1 PIN DESCRIPTION

The following section provides a comprehensive description of each pin on the chip, encompassing its functionality, type, and recommended usage.

Table 1: Legend/Abbreviations Used in Pin Description Table

Name	Abbreviation	Definition
Pin Type	S	Supply pin
	I	Input only pin
	I/O	Input/Output pin
I/O Structure	FT	5V tolerant I/O
	TT	3.6V tolerant I/O
	RF	RF I/O
	RST	Bidirectional reset pin with embedded weak pull-up resistor
	Options for TT or FT I/Os	
	_f	I/O, Fm+ capable
	_a	I/O, with analog switch function supplied by IO BOOSTER[1]

[1]. Refer to the BlueNRG-LP reference Manual (RM0479) for more details.

Table 2: Pinout Description

Number	Pin Name	Functions	Pin Type	I/O Structure	Additional Feature
1	BLE Antenna	-	I/O	RF	-
2	GND	-	Ground	-	-
3	PA3	SWCLK, USART_RTS_DE, TIM_BKIN2, SPI3_SCK, TIM1_CH6, I2S3_SCK	I/O	FT	Wakeup
4	PA2	SWDIO, USART_CK, TIM_BKIN, SPI3_MCK, TIM1_CH5, I2S3_MCK	I/O	FT	Wakeup
5	PA8	USART_RX, SPI1_MOSI, RX_SEQUENCE, SPI3_MISO, TIM1_CH3, I2S3_MISO	I/O	FT	Wakeup, GPIO in DEEPSTOP, RTC_OUT
6	PA9	USART_TX, SPI1_SCK, RTC_OUT, SPI3_NSS, TIM1_CH4, I2S3_WS	I/O	FT	Wakeup, GPIO in DEEPSTOP, LCO
7	GND	-	S	-	-
8	GND	-	S	-	-
9	LoRa Antenna	-	RF I/O	-	-
10	GND	-	S	-	-
11	PB2	USART_RTS_DE, PDM_DATA, TIM1_CH3	I/O	FT_a	ADC_VINM0, wakeup
12	RSTN	RSTN	I	RST	-
13	PB5	LPUART_RX, SPI2_MOSI, PDM_CLK, I2S2_SD	I/O	TT	PGA_VBIAS_MIC, wakeup
14	PB1	SPI1_NSS, PDM_CLK, TIM1_ETR	I/O	FT_a	ADC_VINP1, wakeup
15	PB3	USART_CTS, LPUART_TX, TIM1_CH4	I/O	FT_a	ADC_VINP0, wakeup
16	GND	-	S	-	-
17	GND	-	S	-	-
18	PB6	I2C2_SCL, SPI2_NSS, LPUART_TX, TIM1_CH1, I2S2_WS	I/O	FT_f	Wakeup
19	PB7	I2C2_SDA, SPI2_SCK, LPUART_RX, TIM1_CH2, I2S2_SCK	I/O	FT_f	Wakeup
20	VDD 3V3	-	S	-	-
21	PB9	USART_TX, LPUART_CTS, SPI2_MCK, TIM1_CH1N, TIM1_CH2N, I2S2_MCK	I/O	FT	Wakeup
22	PB12	SPI1_SCK, LCO, PDM_DATA, TIM1_BKIN, TIM1_CH3	I/O	FT	SXTAL0
23	PB13	SPI1_MISO, I2C2_SCL, PDM_CLK, TIM1_BKIN2, TIM1_CH4	I/O	FT	SXTAL1
24	GND	-	S	-	-
25	PA15	I2C2_SMBA, SPI1_MOSI, TIM1_BKIN2	I/O	FT_a	ADC_VINP2, wakeup
26	PA12	I2C1_SMBA, SPI1_NSS, SPI2_MOSI, TIM1_CH1, I2S2_SD	I/O	FT_a	ADC_VINM3, wakeup
27	PA4	LCO, SPI2_NSS, LPUART_TX, TIM1_CH1, I2S2_WS	I/O	FT	Wakeup, GPIO in DEEPSTOP, LCO
28	PA10	LCO, SPI1_MISO, TX_SEQUENCE, SPI3_MCK, TIM1_CH5, I2S3_MCK	I/O	FT	BOOT, wakeup, GPIO in DEEPSTOP, LCO
29	PA7	LPUART_RTS_DE, SPI2_MISO, SPI2_SCK, TIM1_CH2, I2S2_MISO, I2S2_SCK	I/O	FT	Wakeup, GPIO in DEEPSTOP, RTC_OUT
30	GND	-	S	-	-
31	PA5	MCO, SPI2_SCK, LPUART_RX, TIM1_CH2, I2S2_SCK	I/O	FT	Wakeup, GPIO in DEEPSTOP, LCO
32	GND	-	S	-	-

*SPI1 use is discouraged, as it is already routed internally in the SiP. Its use will conflict with LoRa Radio.

1.1.1 ALTERNATE FUNCTIONS

Table 3: Alternate Function List

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA2	TMS_SWDIO	USART_CK	TIM_BKIN	SPI3_MCK/ I2S3_MCK	TIM1_CH5	TMS_SWDIO	-	TMS_SWDIO
PA3	TCK_SWCLK	USART_RTS_ DE	TIM_BKIN2	SPI3_SCK/ I2S3_SCK	TIM1_CH6	TCK_SWCLK	-	TCK_SWCLK
PA4	LCO	SPI2_NSS/ I2S2_WS	-	LPUART_TX	TIM1_CH1	-	-	-
PA5	MCO	SPI2_SCK/ I2S2_SCK	-	LPUART_RX	TIM1_CH2	-	-	-
PA8	USART_RX	SPI1_MOSI	-	SPI3_MISO/ I2S3_MISO	TIM1_CH3	-	-	-
PA9	USART_TX	SPI1_SCK	RTC_OUT	SPI3_NSS/ I2S3_WS	TIM1_CH4	-	-	-
PA10	LCO	SPI1_MISO	-	SPI3_MCK/ I2S3_MCK	TIM1_CH5	-	-	-
PA12	I2C1_SMBA	TMS_SWDIO	SPI1_NSS	SPI2_MOSI/ I2S2_SD	TIM1_CH1	-	-	-
PA15	I2C2_SMBA	-	SPI1_MOSI	-	TIM1_BKIN2	-	-	-
PB1	SPI1_NSS	PDM_CLK	-	TIM1_ETR	-	-	-	-
PB2	USART_RTS_ DE	PDM_DATA	-	TIM1_CH3	-	-	-	-
PB3	USART_CTS	LPUART_TX	-	TIM1_CH4	-	-	-	-
PB5	LPUART_RX	SPI2_MOSI/ I2S2_SD	-	PDM_CLK	-	-	-	-
PB6	I2C2_SCL	SPI2_NSS/ I2S2_WS	-	LPUART_TX	TIM1_CH1	-	-	-
PB7	I2C2_SDA	SPI2_SCK/ IS2S_SCK	-	LPUART_RX	TIM1_CH2	-	-	-
PB9	USART_TX	LPUART_CT S	SPI2_MCK/ I2S2_MCK	TIM1_CH1N	TIM1_CH2N	-	-	-
PB12	SPI1_SCK	LCO	PDM_DATA	TIM1_BKIN	TIM1_CH3	-	-	-
PB13	SPI1_MISO	I2C2_SCL	PDM_CLK	TIM1_BKIN2	TIM1_CH4	-	-	-

2 HARDWARE SECURE ELEMENT - HSE

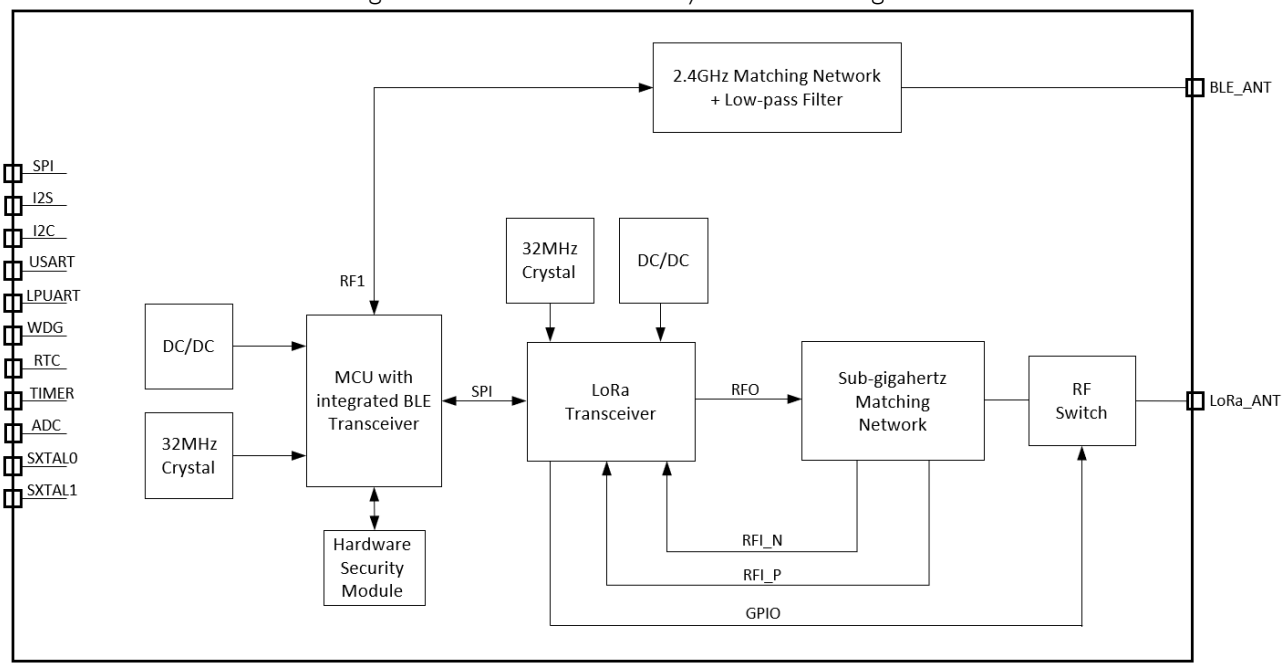
The device offers an optional integrated hardware secure element (STSAFE-A110), providing advanced security capabilities for enhanced protection of sensitive data and secure communication.
The secure element acts as a tamper-resistant microcontroller that safeguards private LoRaWAN keys within HTLRBL32L-xx, maintaining the integrity of the device and enabling secure communication with the network server.
A crypto library is provided with our SDK, which integrates the hardware secure element with the LoRaWAN stack, so you can easily implement the security features on your application.
The secure element being an optional feature, it doesn't interfere with any other functionality of the device having it enabled or disabled.

3 SYSTEM ARCHITECTURE

The HTLRBL32L-xx is a dual protocol wireless communication System-in-Package based on the Semtech SX1262 LoRa transceiver and the STMicroelectronics BlueNRG-LP, an ultra-low power programmable Bluetooth Low Energy transceiver that embeds an ARM Cortex-M0+ microcontroller.

Besides the chipsets, the system integrates all the bypass and decoupling capacitors, the large inductors, and capacitors from the DC-DC regulators of the power supply circuits, and 32MHz crystals for LoRa and BLE. The system-in-package also integrates the 2.4GHz and the sub-gigahertz RF matching networks, RF switch and low-pass filter included.
The iMCP HTLRBL32L-xx system block diagram is shown below:

Figure 2: iMCP HTLRBL32L System Block Diagram



4 ELECTRICAL CHARACTERISTICS

4.1 GENERAL OPERATING RANGE

Table 4: General Operating range

Parameter	Min	Typ.	Max	Unit
Supply Voltage	2.7	3.3	3.6	V
Operating Temperature	-20	-	+75	°C

4.2 MCU I/O PORT CHARACTERISTICS

Table 5: MCU I/O Port Characteristics

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
$\mathbf{V_{IL}}$	I/O Input low level voltage	1.62 < V_{DD} < 3.6	-	-	$0.3V_{DD}$	V
$\mathbf{V_{IH}}$	I/O Input high level voltage		$0.7V_{DD}$	-	-	
$\mathbf{I_{lkg}}$	Input leakage current	$0 \le \mathrm{V_{IN}} \le MAX(V_{DD_x})^{(1)}$	-	-	+/- 100	nA
		$MAX(V_{DD_x})^{(1)} \le \mathrm{V_{IN}} \le MAX(V_{DD_x})^{(1)} + 1\mathrm{V}$	-	-	650	
		$MAX(V_{DD_x})^{(1)} + 1\mathrm{V} < \mathrm{V_{IN}} \le 5.5\mathrm{V}$	-	-	200	
$\mathbf{R_{PU}}$	Pull-up resistor	$\mathrm{V}_{IN} = GND$	25	40	55	kΩ
$\mathbf{R_{PD}}$	Pull-down resistor	$\mathrm{V}_{IN} = V_{DD}$	25	40	65	kΩ

[1]. $MAX(V_{DD_x})$ is the maximum value among all the I/O supplies.

Table 6: Output Voltage Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$\mathbf{V_{OL}}$	Output low level voltage for an I/O pin	CMOS port[1] $I_{IO} = +8\mathrm{mA}$ $\mathrm{V}_{DD} \ge 2.7V$	-	0.4	V
$\mathbf{V_{OH}}$	Output high level voltage for an I/O pin		V_{DD}-0.4	-	
$\mathbf{V_{OL}}$	Output low level voltage for an I/O pin	$I_{IO} = +20\mathrm{mA}$ $\mathrm{V}_{DD} \ge 2.7V$	-	1.3	
$\mathbf{V_{OH}}$	Output high level voltage for an I/O pin		V_{DD}-1.3	-	
$\mathbf{V_{OL}}$	Output low level voltage for an I/O pin	$I_{IO} = +4\mathrm{mA}$ $\mathrm{V}_{DD} \ge 1.62V$	-	0.4	
$\mathbf{V_{OH}}$	Output high level voltage for an I/O pin		V_{DD}-0.45	-	

[1]. CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.

4.3 POWER CONSUMPTION

Characteristics measured over recommended operating conditions unless otherwise specified. Typical values are referred to 25 °C temperature and VDD = 3.3 V.

Table 7: LoRa Mode - Power Consumption TA = 25 °C, VDD = 3.3 V.

Parameter	Condition	Typ.	Unit
LoRa receive mode @Sensitivity Level, RX boosted, DC-DC enabled	Freq = 433MHz, SF = 12, BW = 125kHz	9.6	mA
	Freq = 470MHz, SF = 12, BW = 125kHz	9.5	
	Freq = 868MHz, SF = 12, BW = 125kHz	4.6	
	Freq = 915MHz, SF = 12, BW = 125kHz	4.6	
	Freq = 923MHz, SF = 12, BW = 125kHz	9.5	
LoRa receive mode @Sensitivity Level, RX power saving, DC-DC enabled	Freq = 433MHz, SF = 12, BW = 125kHz	9.1	
	Freq = 470MHz, SF = 12, BW = 125kHz	9	
	Freq = 868MHz, SF = 12, BW = 125kHz	4.6	
	Freq = 915MHz, SF = 12, BW = 125kHz	4.6	
	Freq = 923MHz, SF = 12, BW = 125kHz	9	
LoRa transmit mode at maximum output power @22dBm optimal setting, DC-DC enabled	Freq = 433MHz, SF = 7, BW = 500kHz	121	
	Freq = 470MHz, SF = 7, BW = 500kHz	121	
	Freq = 868MHz, SF = 7, BW = 500kHz	118	
	Freq = 915MHz, SF = 7, BW = 500kHz	112	
	Freq = 923MHz, SF = 7, BW = 500kHz	112	
LoRa transmit mode at maximum output power @14dBm optimal setting, DC-DC enabled	All frequency range, SF = 7, BW = 500kHz	40	

Table 8: BLE Mode - Power Consumption TA = 25 °C, VDD = 3.3 V.

Parameter	Condition	Typ	Unit
BLE peak current on Receive mode, SMPS ON	1Mbps @Sensitivity Level	7	mA
	125kbps @Sensitivity Level	7.6	
BLE peak current on Transmit mode, SMPS ON	1Mbps @0dBm	4.8	
	1Mbps @4dBm	5	
	1Mbps @7dBm	6	

Table 9: Sleep Mode - Power Consumption TA = 25 °C, VDD = 3.3 V.

Parameter	Condition	Typ	Unit
DeepStop Mode	LoRa & BLE radios on sleep mode, RAM retention, RTC and Watchdog enabled	2	uA

4.4 INTERNAL CRYSTAL OSCILLATOR

The integrated crystal oscillators are used as the frequency reference for the RF transceivers and their choice was based on the LoRa and BLE chipsets requirements.

4.4.1 LORA HIGH-SPEED CRYSTAL OSCILLATOR

Table 10: LoRa High-Speed XTAL Oscillator Specification

Parameter	Min	Typ.	Max	Unit
Oscillator frequency		32		MHz
Frequency tolerance	-10		10	ppm
Equivalent series resistance		50		Ω
Crystal load capacitance		10		pF
Drive Level			100	μW

4.4.2 BLE HIGH-SPEED CRYSTAL OSCILLATOR

Table 11: BLE High-Speed XTAL Oscillator Specification

Parameter	Min	Typ.	Max	Unit
Oscillator frequency		32		MHz
Frequency tolerance	-10		10	ppm
Equivalent series resistance		50		Ω
Crystal load capacitance		8		pF
Drive Level			100	μW

4.5 EXTERNAL CRYSTAL OSCILLATOR

Low-speed clock can be supplied with an external 32.768 kHz crystal oscillator. Requirements for the external 32.768 kHz crystal are shown in the table below.

Table 12: BLE Low-Speed XTAL Oscillator Specification

Parameter	Min	Typ.	Max	Unit
Oscillator frequency		32.768		kHz
Equivalent series resistance			90	kΩ
Drive Level			0.1	μW

5 RF CHARACTERISTICS

5.1 LORA RADIO SPECIFICATIONS

Table 13: LoRa Transceiver and Receiver Characteristics

Parameter	Condition	Min	Typ.	Max	Unit
Frequency	LoRaWAN communication	433		928	MHz
LoRa RX sensitivity level for BER < 1%, RX boosted mode	Freq = 433MHz, SF = 12, BW = 125kHz	-116			dBm
	Freq = 470MHz, SF = 12, BW = 125kHz	-118			
	Freq = 868MHz, SF = 12, BW = 125kHz	-120			
	Freq = 915MHz, SF = 12, BW = 125kHz	-132			
	Freq = 923MHz, SF = 12, BW = 125kHz	-130			
LoRa RX sensitivity level for BER < 1%, RX power saving mode	Freq = 433MHz, SF = 12, BW = 125kHz	-114			
	Freq = 470MHz, SF = 12, BW = 125kHz	-116			
	Freq = 868MHz, SF = 12, BW = 125kHz	-120			
	Freq = 915MHz, SF = 12, BW = 125kHz	-132			
	Freq = 923MHz, SF = 12, BW = 125kHz	-132			
LoRa maximum output power @22dBm optimal setting	All frequency range	21		+22	
LoRa maximum output power @14dBm optimal setting	433-470MHz	11		12	
	868-928MHz	12.5		14	

TA = 25°C based on characterization; VDD = 3.3V; All measurements made at the antenna connector, with the external RF track losses compensated.

5.2 BLE RADIO SPECIFICATIONS

Table 14: BLE Transceiver and Receiver Characteristics

Parameter	Condition	Min	Typ.	Max	Unit
Frequency	BLE communication	2402		2480	MHz
RF channel spacing	0 to 39		2		
BLE RX sensitivity level for BER < 1%	1Mbps	-94			dBm
	125kbps	-99			
BLE TX output power	@1Mbps	-20		+7	
RF power accuracy	@27 °C	-1.5		1.5	dB
Data Rate		0.125		2	Mbps

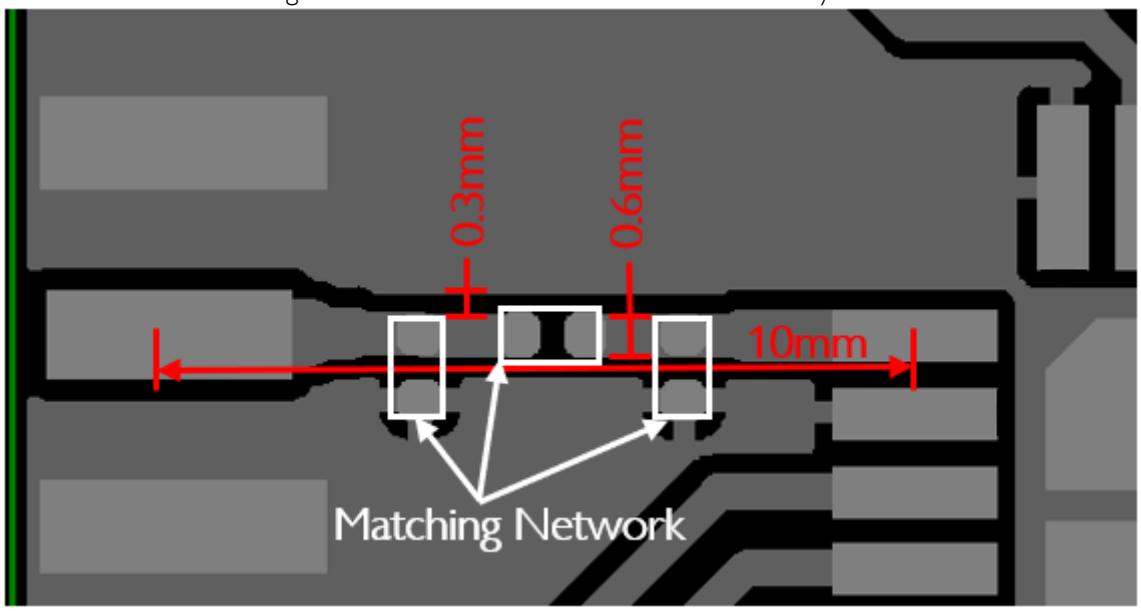
TA = 25°C based on characterization; VDD = 3.3V; all measurements are made at the antenna connector, with the external RF track losses compensated.

5.3 EXTERNAL TRANSMISSION LINES

With a short transmission line, a roughly 50 ohms impedance can be achieved, therefore, the RF performances are granted without the need for a matching network. However, if the antenna or device connected to the antenna pin has a -input impedance different from 50 ohms, a matching network can be assembled in the spaces available to avoid performance loss. A reference for the transmission lines in a 2 layers FR4 1.6 mm PCB is shown below:

- Width = 0.6mm
- Length = 10mm
- Clearance = 0.3mm
- 1 Oz copper

Figure 3: Reference for the Transmission Line Layout.



The antenna's 50 ohms matching can also be optimized by increasing the width of the transmission line of the reference above.

6 PACKAGE OUTLINE

Figure 4: Package Outline

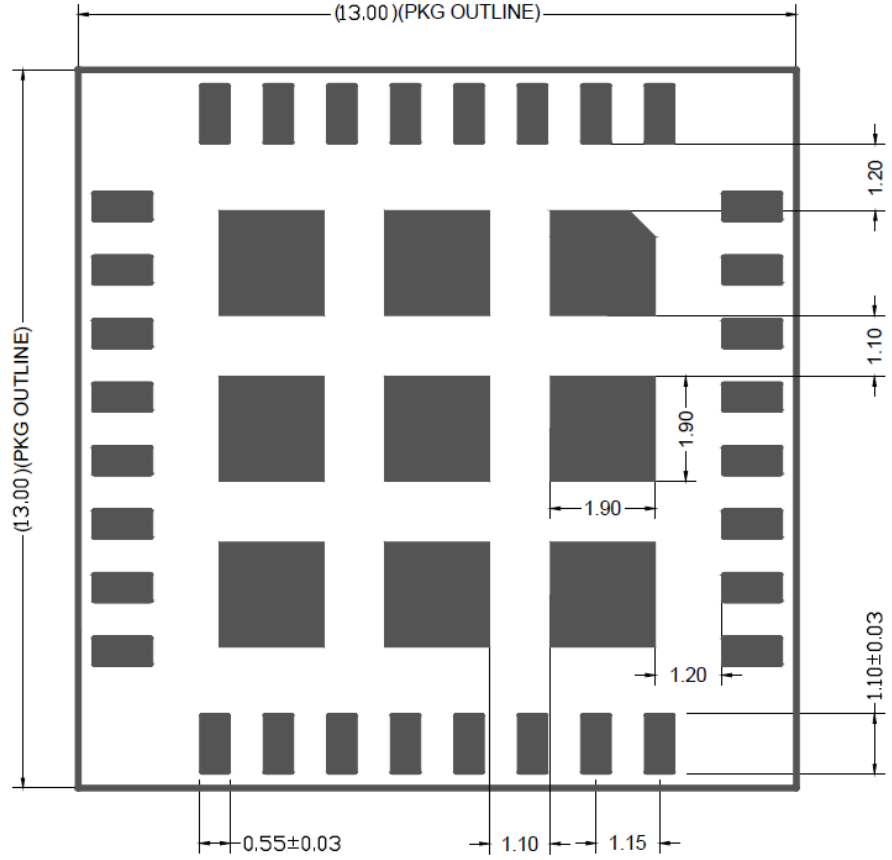
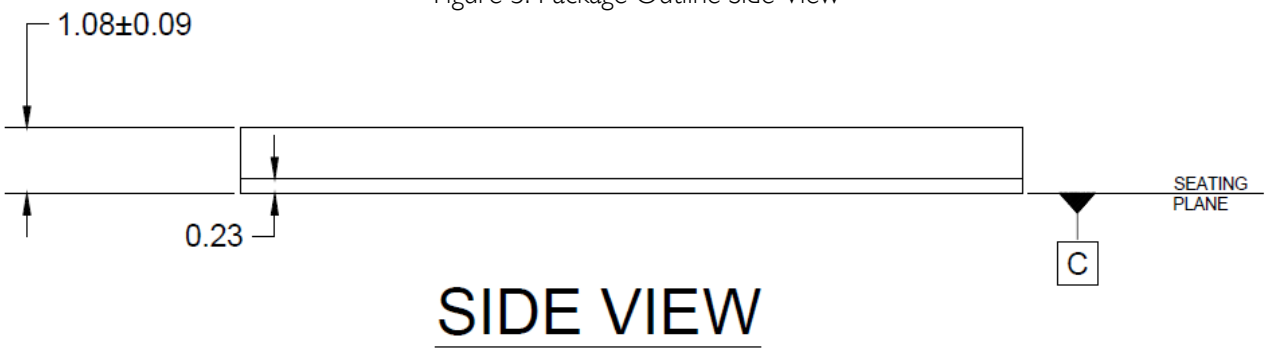


Figure 5: Package Outline Side View



7 RECOMMENDED PCB FOOTPRINT

Figure 6: Recommended PCB Footprint

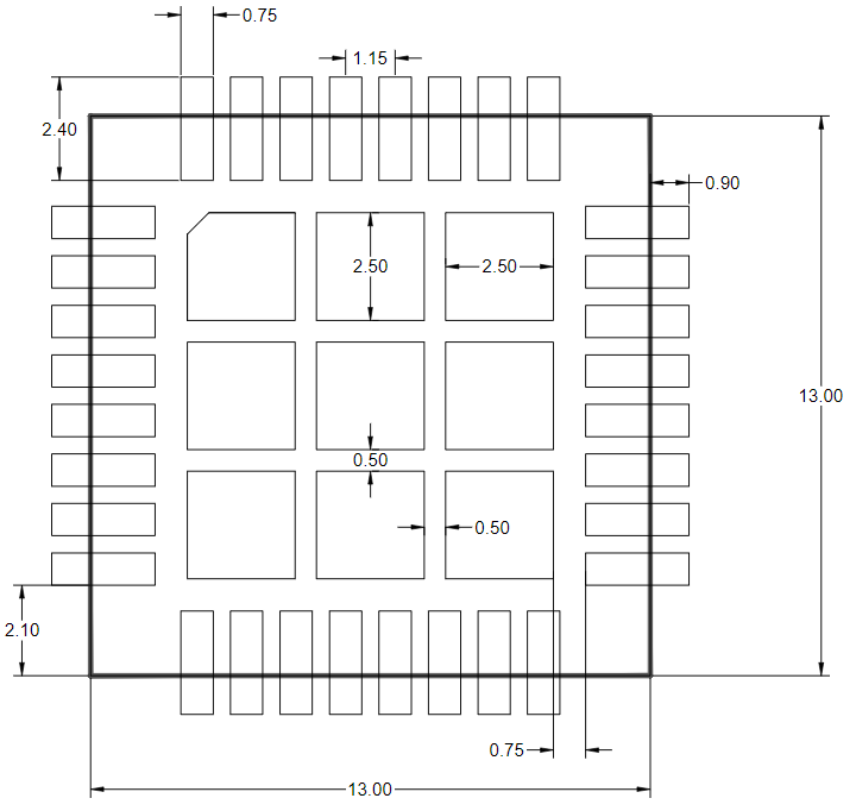
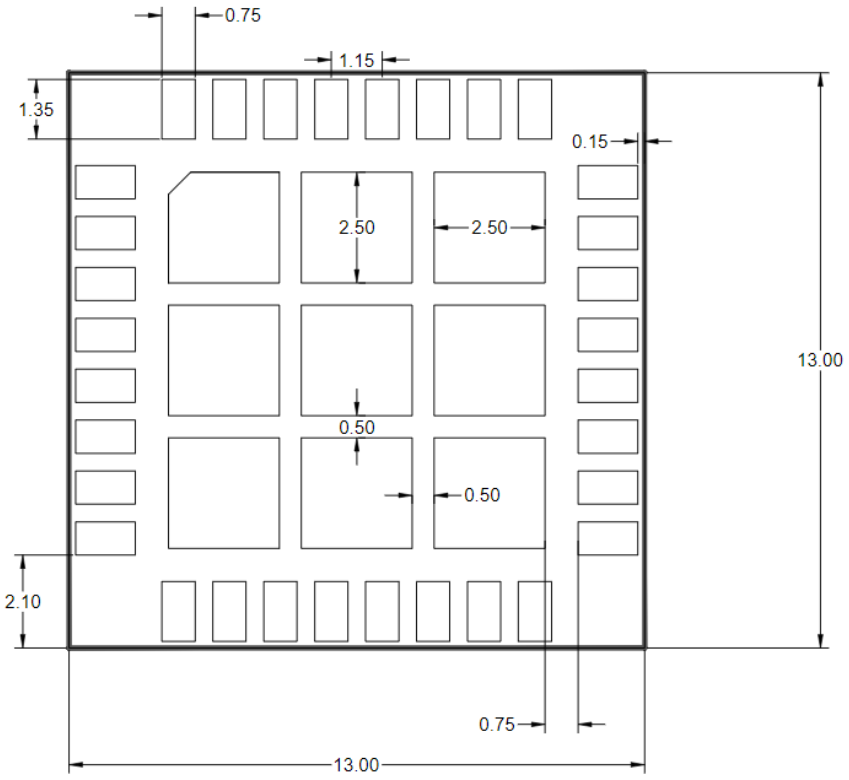


Figure 7: Recommended PCB footprint for shielded SiP



8 PART NUMBER

Figure 8: Part Number Description

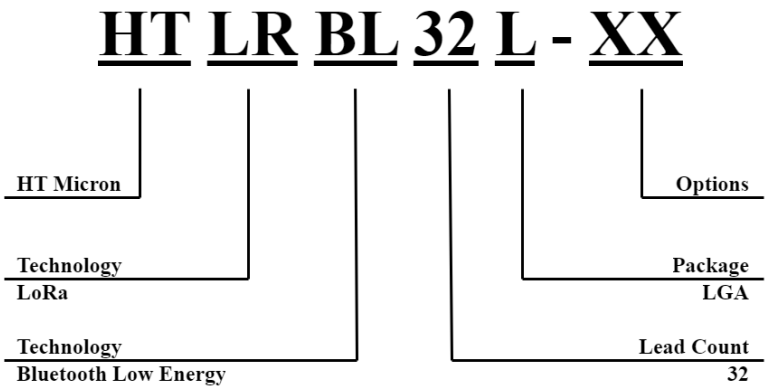


Table 15: Options Table

Option Number	HSE	Shielding
00	No	No
01	No	Yes
10	Yes	No
11	Yes	Yes

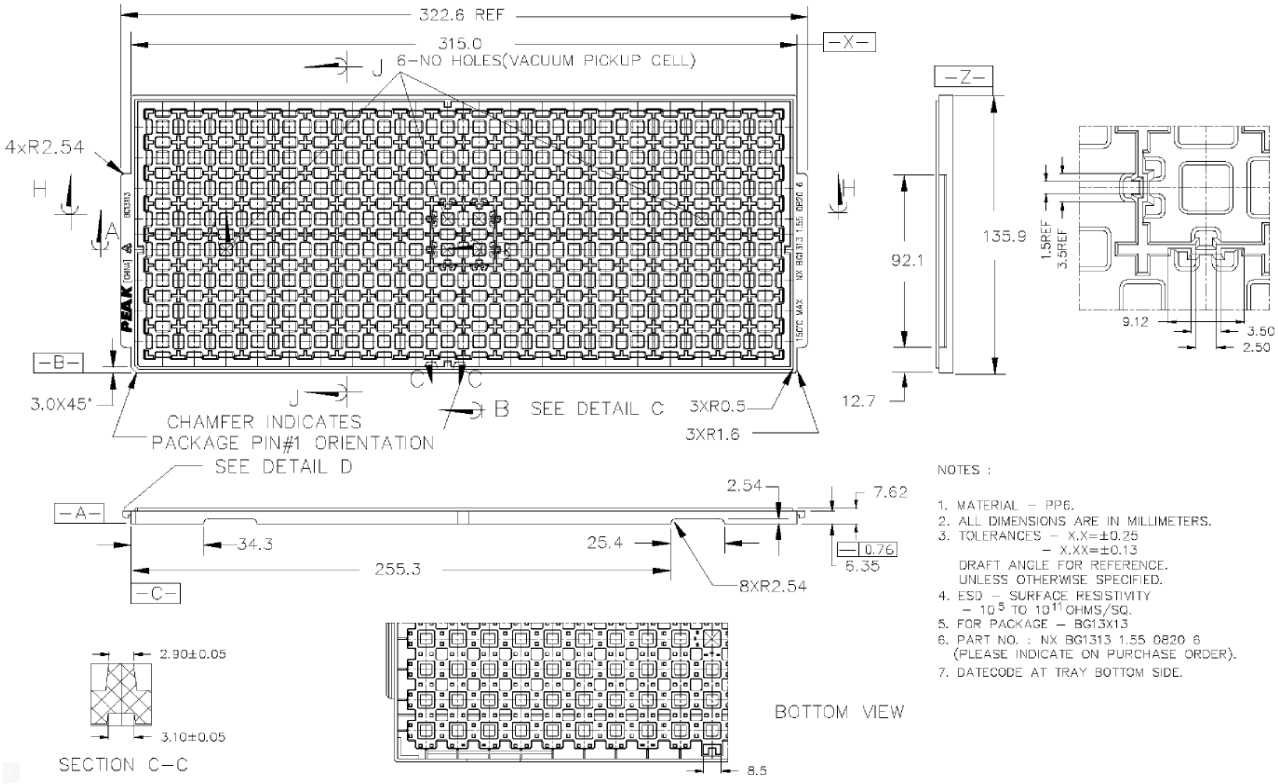
9 PACKAGING AND ORDERING INFORMATION

Table 16: Ordering Information

Part number	Package	
	Name	Description
HTLRBL32L-xx	iMCP HTLRBL	SiP module in LGA package; body 13mm x 13mm

Products sold directly by HT Micron will be delivered in bagged trays, sealed in moisture-resistant bags with a desiccant pack and humidity cards. Trays are suitable for baking temperatures. Samples provided by HT Micron may be delivered in other packing methods. Please, refer to section 10 for storage, handling and moisture sensitivity information.

Figure 9: Tray Sizes



10 STORAGE AND HANDLING

CAUTION

ELECTROSTATIC and MOISTURE
SENSITIVE DEVICE

LEVEL 3

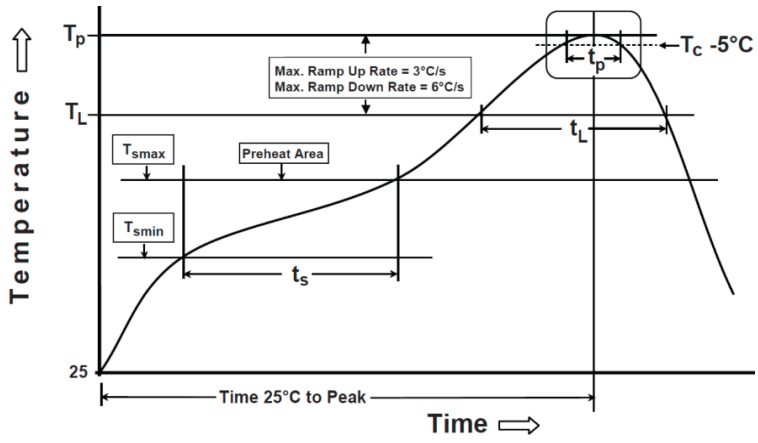
- Baking for 24 hours at 125 ±5°C is strongly recommended prior to mounting.
- Take proper precautions to avoid high-energy electrostatic discharge (ESD) as permanent damage may occur.
- For handling methods refer to the latest ESD Association standard ANSI/ESD S20.20.
- Do not expose the device to corrosive gasses, extreme humidity, extensive direct sunlight.
- The device is susceptible to delamination or crack damage induced by absorbed moisture and high temperature.
- Shelf life in sealed bagged tray: 12 months at ≤40°C and ≤90% relative humidity (RH).
- This device is rated MSL 3.
- For bagged tray lots: after the bag is opened, the humidity card must read ≤20% (at 23 ±5°C), and the devices must be mounted within 168 hours at environmental conditions of ≤30°C, ≤60% RH.
- If the above condition is not met, baking for 24 hours at 125 ±5°C is mandatory prior to mounting.
- For moisture sensitivity devices precaution methods refer to the latest standard IPC/JEDEC-J-STD-033.
- For any other packing method: baking is required for 192 hours at 40°C prior to mounting.

- This device is composed of all RoHS-compliant materials. Refer to Figure 10 for typical Pb-Free reflow conditions.
- Hand soldering is not recommended for this device.
- For moisture sensitivity classification and soldering methods, refer to the latest standard IPC/JEDEC-J-STD-020.
- Do not drop, shock or apply mechanical stress.

11 SOLDERING INFORMATION

Soldering conditions depend greatly on the solder paste that is used and as such are application specific. The picture below depicts typical Pb-free soldering conditions as seen in IPC/JEDEC-J-STD-020 standard, which are commonly used in the industry. However, ultimately, we recommend that the instructions of the solder supplier are followed.

Figure 10: Typical PB-Free Reflow Conditions (IPC/JEDEC-J-STD-020)



Min preheat temperature (T_{smin}): 150 °C
Max preheat temperature (T_{smax}): 200 °C
Preheat (soaking) time (T_s): 60 to 120 s
Liquidous temperature (T_L): 217 °C
Peak temperature (T_p): 260 °C
Max ramp-up rate (T_L to T_p): 3 °C/s
Time above T_L (t_L): 60 to 150 s
Classification temperature (T_c): 260 °C
Time above Tc -5 °C (t_p): 30 s
Max ramp-down rate (T_p to T_L): 6 °C/s
Max time 25°C to T_p: 8 minutes

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ABBREVIATIONS

Table 17: ABBREVIATIONS

Acronym	Description
ADC	Analog to Digital Converter
CLK	Clock
DMA	Direct Memory Access
FSK	Frequency Shift Keying
GFSK	Gaussian Frequency Shift Keying
GMSK	Gaussian Minimum Shift Keying
GPIO	General Purpose Input Output
HSE	Hardware Secure Element
I2C	Inter-Integrated Circuit
IO	Input Output
IrDA	Infrared Data Association
LGA	Land Grid Array
LPUART	Low Power Universal Asynchronous Receiver/Transmitter
MCU	Microcontroller Unit
MSK	Minimum Shift Keying
MSL	Moisture sensitivity level
PCB	Printed-Circuit Board
PDM	Pulse Density Modulation
PGA	Programmable Gain Amplifier
PWM	Pulse Width Modulation
RAM	Random Access Memory
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
ROM	Read-Only Memory
RTC	Real Time Clock
RX	Receiver
SCL	Serial Clock
SDA	Serial Data
SDK	Software Development Kit
SMPS	Switched Mode Power Supply
SPI	Serial Peripheral Interface
TX	Transmitter
USART	Universal Synchronous Asynchronous Receiver Transmitter
WDG	Watchdog

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