Computer Architecture and system programming

Kristoffer Klokker

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Contents

1 Exercises

1.1 Benchmark

For the 40MHz processor which performed the instructions

Instruciton type	Instruction count	Cycles per instruction
Integer artihemtic	41,000	1
Data transfer	28,000	2
Floating point	25,000	2
Control transfer	6,000	2

1.1.1 Find the average CPI

$$\frac{1 \cdot 41000 + 2 \cdot 28000 + 2 \cdot 25000 + 2 \cdot 6000}{100000} = 1.59$$

CPI is the average cycles pr instruction. Therefore 4.5

1.1.2 Execution time

$$\begin{aligned}
CPI &= 1.59 \\
I_c &= 100000 \\
\tau &= \frac{1}{f} = \frac{1}{40000000Hz} \\
T &= I_c \cdot CPI \cdot \tau \\
&= 1.59 \cdot 100000 \cdot \frac{1}{40000000Hz} \\
T &= 0.003975s
\end{aligned}$$

1.1.3 MIPS

$$\begin{aligned}
MIPS &= \frac{f}{CPI \cdot 10^6} \\
CPI &= 1.59 \\
f &= 40000000Hz \\
MIPS &= \frac{40000000Hz}{1.59 \cdot 10^6} \\
MIPS &= 25.16\frac{1}{s}
\end{aligned}$$

1.2 Explain how a negative number is represnted in the following representation

- Sign-magnitude - The left most bit must be 1 which result in the rest being interpretated as negative
- Twos compliment - The left most bit is 1 to subtract the maximum value from the rest
- Biased - Bias is most usually half the range therefore a negative value is simply less half the maximum value

1.3 Represent the following in 8 bit twos compliment and sing magnitude

- 64 - 00100000
- -28 - twos 11100100 - sign 10011100

1.4 Convert from twos compliment to decimal

- 1100110 : -26
- 1011101 : -35

1.5 Show the calculations in 8 bit twos compliment

1.5.1 6+12

$$
\begin{aligned}
6 &= 00000110 \\
12 &= 00001100 \\
00000110 + 00001100 &= 00010010
\end{aligned}
$$

1.5.2 -6+12

$$
\begin{aligned}
-6 &= 11111010 \\
12 &= 00001100 \\
11111010 + 00001100 &= 00000110
\end{aligned}
$$

Overflow is ignored

1.5.3 6-12

$$6 = 00000110$$
$$-12 = 11110100$$
$$00000110 + 11110100 = 11111010$$

1.5.4 -6-12

$$-6 = 11111010$$
$$-12 = 11110100$$
$$11111010 + 11110100 = 11101110$$

Overflow is ignored

1.6 Fill out the table for the most twos compliment addition

Input			Output		
x_{n-1}	y_{n-1}	c_{n-2}	z_{n-1}	c_{n-1}	v
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	1	0	0
0	1	1	0	1	0
1	0	0	1	0	0
1	0	1	0	1	0
1	1	0	1	1	0
1	1	1	1	1	1

Here x_{n-1} and y_{n-1} is the most signifact bits of the two addends.
c is the carry bit and z_{n-1} is the results most significatn bit.
v is a bit singnaling overflow.
If can be seen in row 2 and the last row that:
Overflow occurs if and only if the carry into the addition of the MSBs isdifferent from the carry out of that addition

1.7 Convert 23 and 29 to 6 bit twos compliment and multiply using Booths algorithm

$$23 = 010111$$
$$29 = 011101$$
$$A = 0$$
$$Q_{-1} = 0$$
$$M = 010111$$
$$Q = 011101$$
$$count = 6$$

$$Q_0, Q_{-1} = 10$$
$$A = A - M = 101001$$
$$shift\ A = 101001\ Q = 011101\ Q_{-1} = 0$$
$$A = 110100$$
$$Q = 101110$$
$$Q_{-1} = 1$$
$$count = 5$$

$$Q_0, Q_{-1} = 01$$
$$A = A + M = 110100 + 010111 = 001011$$
$$shift$$
$$A = 000101$$
$$Q = 110111$$
$$Q_{-1} = 0$$
$$count = 4$$

$$Q_0, Q_{-1} = 10$$
$$A = A - M = 000101 - 011001$$
$$A = 000101 + 101001 = 101110$$
$$shift\ A = 101110\ Q = 110111\ Q_{-1} = 0$$
$$A = 110111$$
$$Q = 011011$$
$$Q_{-1} = 1$$
$$count = 3$$

$$Q_0, Q_{-1} = 11$$
$$shift\ A = 110111\ Q = 011011\ Q_{-1} = 1$$
$$A = 111011$$
$$Q = 101101$$
$$Q_{-1} = 1$$
$$count = 2$$

$$Q_0, Q_{-1} = 11$$
$$shift\ A = 111011\ Q = 101101\ Q_{-1} = 1$$
$$A = 111101$$
$$Q = 110110$$
$$Q_{-1} = 1$$
$$count = 2$$

$$Q_0, Q_{-1} = 01$$
$$A = A + M = 111101 + 011001$$
$$A = 010100$$
$$shift\ A = 010100\ Q = 110110\ Q_{-1} = 1$$
$$A = 001010$$
$$Q = 011011$$
$$Q_{-1} = 0$$
$$count = 2$$

$$010111 \times 011101 = AQ = 001010011011$$