Started on Thursday, 1 August 2024, 9:23 AM

State Finished

Completed on Thursday, 1 August 2024, 9:24 AM

Time taken 44 secs

Question 1
Not answered
Marked out of
12,00

For each statement, indicate if it is True or False.

True	False	
0	0	The operating system maintains one page table per CPU core for virtual memory translation.
		A pointer is a variable that stores a memory address.
		For a single threaded program written in C, both the compiler and the CPU itself may re- order data-independent instructions in the program to optimize performance. However, both the compiler and the CPU apply re-ordering conservatively, such that the final outcome of the program is the same as the output of the original program written by the developer.
		Global variables are stored on the heap.
		When debugging your C program with the GDB debugger, the memory addresses you see for variables in your program are physical (as opposed to virtual) memory addresses.
		When the gcc compiler (with optimization level greater than the default -O0) analyzes a particular procedure foo, it treats each procedure that foo calls as a "white box". This means that while the compiler is applying optimizations, it appears to the compiler as if this all procedures in the code are inlined.
		The virtual memory address of an integer local variable in your C program may be different each time the program runs due to Address Space Layout Randomization (ASLR), which randomizes the start of the stack and shared library memory regions.
		Variables stored on the heap have higher memory addresses than variables stored on the stack.
		As a C programmer, you should use assert statements to notify users about any unexpected errors in the inputs they provide to your program.
		The gcc compiler ensures that procedure arguments and local variables are always stored in the procedure's stack frame.
		If the value of a int pointer $\bf p$ on the heap is 0x1000, then ( $\bf p$ +1) is 0x1004. Assume size of (int)=4.
		Compared to single-level page tables, multi-level page tables optimize address translation latency.

Not answered Marked out of 2,00 Consider the C declaration:

```
int arr[10] = {9, 8, 7, 6, 5, 4, 3, 2, 1, 0};
```

Suppose that the compiler has placed the variable arr in the %ecx register.

How do you move the value at arr[2] into the %eax register? Assume that %ebx is 2 and sizeof(int) = 4.

You can view the x86-64 reference sheet by clicking here.

omovl (%ecx,%ebx,4),%eax	8
○ movl 4(%ecx,%ebx,1),%eax	8
○ leal 8(%ecx),%eax	<u>\$</u>
○ leal (%ecx,%ebx,4),%eax	8
○ leal 4(%ecx,%ebx,2),%eax	8

Scoring method: SC1/0 ?

## Question $\bf 3$

Not answered Marked out of 6,00 Consider the executable a.out, compiled and linked as follows:

> gcc -fno-common -o a.out main.c init.c

main.c contains:

```
#include <stdio.h>
int a = 1;
static int b = 2;
int c = 3;
int main() {
   int c = 4;
   init();
   printf("a=%d, b=%d, c=%d\n", a, b, c);
   return 0;
}
```

init.c contains:

```
extern int a, c;
int b;

void init() {
    a = 5;
    b = 6;
    c = 7;
}
```

What values of a, b, an c does a.out print?



# Question 4 Not answered Marked out of

20,00

In this question you will analyze the cache miss rate for a function written in C.

Consider the following function that transposes a matrix src and writes the result in dst.

```
void transpose(int src[4][4], int dest[4][4]){
   int i,j;
   for (i=0; i<4; i++) {
      for (j=0; j<4; j++) {
         dst[j][i] = src[i][j];
      }
   }
}</pre>
```

Consider a **direct-mapped**, **write-allocate**, **write-back** L1 data cache with **16 byte blocks** (i.e., cache line size = 16 bytes) and **128 bytes total data capacity**.

Assume the src array starts at address  $\underline{0xff00}$  and the dst array starts at address  $\underline{0xff40}$ . Assume size of (int) = 4.

#### Part 1:

For each read to *src* and write to *dst* while the function is executing, select whether the read or write access is a **miss** or a **hit** in the L1 data cache. Assume the cache is empty at the beginning.

Assume row-major order, i.e., src[0][1] is row 0, col 1.

#### src

	Col 0	Col 1	Col 2	Col 3
Row 0				
Row 1				
Row 2				
Row 3				

#### dst

(	Col 0	Col 1	Col 2	Col 3
Row 0				
Row 1				
Row 2				
Row 3				

What is the L1 cache **miss rate** in %? Enter a number from 0 to 100:

#### Part 2:

Repeat part 1, now assuming the L1 cache's total data capacity is 64 bytes instead of 128 bytes. For each read to *src* and write to *dst* while the function is executing, select whether the read or write access is a **miss** or a **hit** in the L1 data cache. Assume the cache is empty at the beginning.

Assume row-major order, i.e., src[0][1] is row 0, col 1.

#### src

	Col 0	Col 1	Col 2	Col 3
Row 0				
Row 1				
Row 2				
Row 3				

## dst

(	Col 0	Col 1	Col 2	Col 3
Row 0				
Row 1				
Row 2				
Row 3				

What is the L1 cache <b>miss rate</b> in %? Enter a number from 0 to 100:	

## Question 5

Not answered

Marked out of 6,00

Consider a virtual memory system that has the following characteristics:

- Physical addresses are 32 bits wide
- Virtual addresses are 48 bits wide
- The page size is 4K bytes
- The TLB contains 32 entries of the page table
- The TLB is 4-way associative
- For simplicity, assume the metadata per entry consists of 1 valid bit and 1 dirty bit

How many bits are used to represent the Virtual Page Number?	
How many bits are used for each TLB tag?	
How many bits per TLB entry?	

Not answered Marked out of 16,00 Consider the following code:

```
int product(int* a, int n){
   int i, x, y, z;
   int p = 1;
   for (i = 0; i < n-2; i+=3) {
        x = a[i];
        y = a[i+1];
        z = a[i+2];
        p = p * x * y * z; // PRODUCT CALCULATION
   }
   for (; i < n; i++) {
        p = p * a[i];
   }
   return p;
}</pre>
```

For the line marked "PRODUCT COMPUTATION" consider 4 different re-association options:

```
Version a: p = ((p * x) * y) * z

Version b: p = (p * (x * y)) * z

Version c: p = p * ((x * y) * z)

Version d: p = (p * x) * (y * z)
```

This code executes on an Intel processor. Assume the processor has a **single integer multiplication unit** which is pipelined to support issuing **up to 1 integer multiplication per cycle** (i.e., after issuing an integer multiplication, the next integer multiplication can be issued in the next cycle). Assume the **latency of an integer multiplication is 3 cycles** for this processor.

Calculate the **theoretical cycles per element** for each PRODUCT COMPUTATION option. Recall that the cycles per element (CPE) is a measure of performance where the cycles for a computation on an array of size n is expressed as Cn + K, where C is the cycles per element. The theoretical CPE is the value of C assuming the only factors are the cycles per issue and the latency of the integer multiplication unit in the processor.

Hint: focus on the first for loop, you do not need to take into account the second for loop for the theoretical CPE calculation.

Fill in the blanks by specifying values with up to 2 decimal places.

```
a) With p = ((p * x) * y) * z, the theoretical CPE is:
b) With p = (p * (x * y)) * z, the theoretical CPE is:
c) With p = p * ((x * y) * z), the theoretical CPE is:
d) With p = (p * x) * (y * z), the theoretical CPE:
```

Which of the above versions has the lowest cycles per element?

- ab
- ) c
- O d

Which of the above versions has the highest cycles per element?

- o a
- b
- $\bigcirc$  c
- $\bigcirc$  d

Complete

Marked out of 12.00



## lti.solvedSession.not.found

Error: Solved session not found [lti.solvedSession.not.found] at LtiWorkflowHandler.getSolvedSession (imports/utils/LtiWorkflowHandler.ts:394:13) at imports/utils/LtiWorkflowHandler.ts:168:32 at /var/expert/bundle/programs/server/npm/node\_modules/meteor/promise/node\_modules/meteor-promise/fiber\_pool.js:43:40 => awaited here: at Function.Promise.await (/var/expert/bundle/programs/server/npm/node\_modules/meteor/promise/node\_modules/meteor-promise/promise\_server.js:56:12) at imports/utils/LtiWorkflowHandler.ts:134:7 at /var/expert/bundle/programs/server/npm/node\_modules/meteor/promise/node\_modules/meteor-promise/fiber\_pool.js:43:40 => awaited here: at Function.Promise.await (/var/expert/bundle/programs/server/npm/node\_modules/meteor/promise/node\_modules/meteor-promise/promise\_server.js:56:12) at imports/utils/LtiWorkflowHandler.ts:108:5 at /var/expert/bundle/programs/server/npm/node\_modules/meteor/promise/node\_modules/meteor-

#### Question 8

Complete

Marked out of 24,00



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Complete

Marked out of 12.00



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#### Question 10

Complete

Marked out of 12,00



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Information

This question is about x86 Assembly.

To help you with this question, you can view the x86-64 reference sheet by clicking here.

#### Question 11

Complete

Marked out of 20,00



## lti.solvedSession.not.found

Error: Solved session not found [lti.solvedSession.not.found] at LtiWorkflowHandler.getSolvedSession (imports/utils/LtiWorkflowHandler.ts:394:13) at imports/utils/LtiWorkflowHandler.ts:168:32 at /var/expert/bundle/programs/server/npm/node\_modules/meteor/promise/node\_modules/meteor-promise/fiber\_pool.js:43:40 => awaited here: at Function.Promise.await (/var/expert/bundle/programs/server/npm/node\_modules/meteor/promise/node\_modules/meteor-promise/promise\_server.js:56:12) at imports/utils/LtiWorkflowHandler.ts:134:7 at /var/expert/bundle/programs/server/npm/node\_modules/meteor/promise/node\_modules/meteor-promise/fiber\_pool.js:43:40 => awaited here: at Function.Promise.await (/var/expert/bundle/programs/server/npm/node\_modules/meteor/promise/node\_modules/meteor-promise/promise\_server.js:56:12) at imports/utils/LtiWorkflowHandler.ts:108:5 at /var/expert/bundle/programs/server/npm/node\_modules/meteor/promise/node\_modules/meteor-

Complete

Marked out of 12,00



## lti.solvedSession.not.found

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#### Question 13

Complete

Marked out of 25,00