1. Description

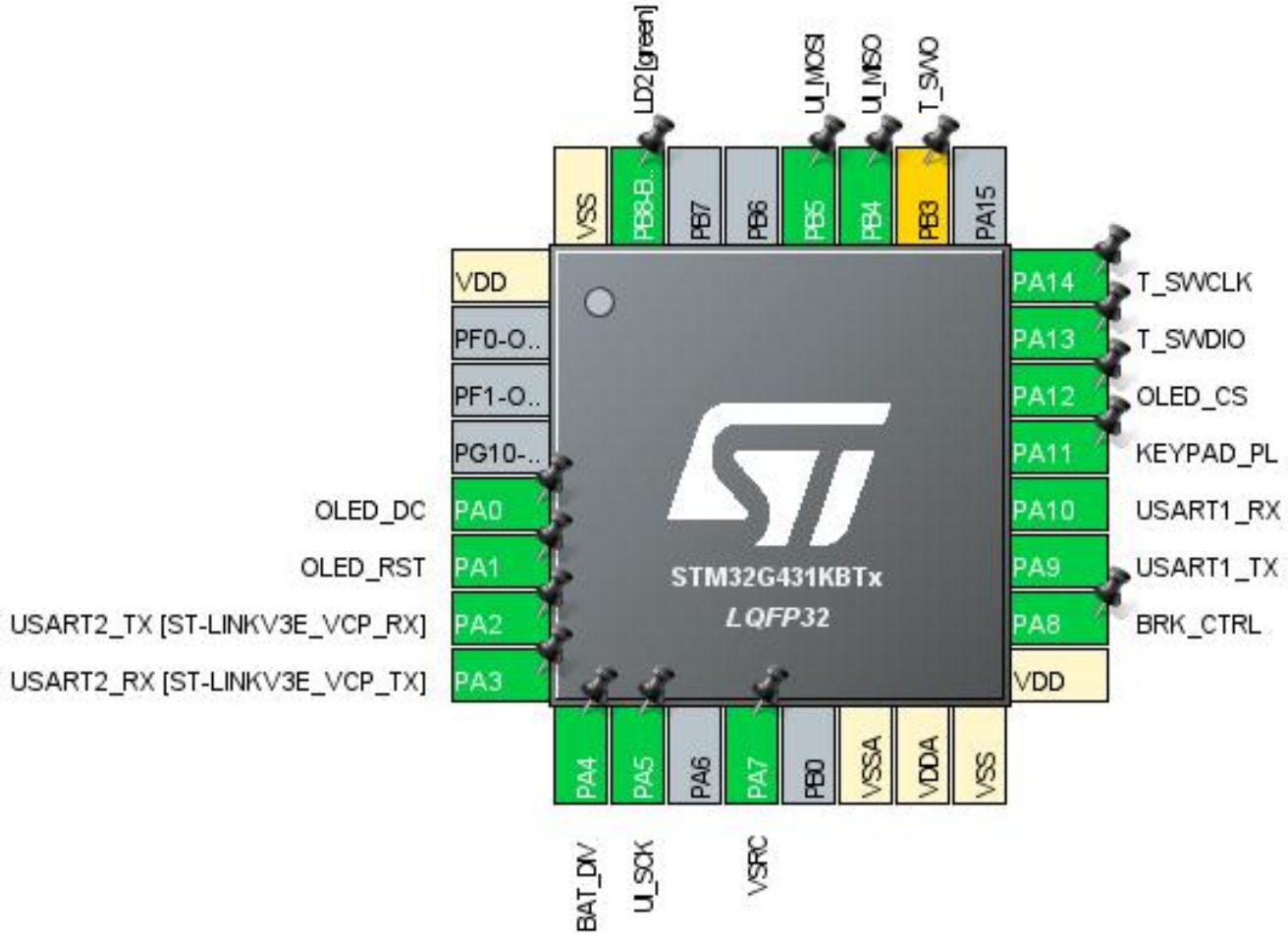
1.1. Project

Project Name	Blinky
Board Name	NUCLEO-G431KB
Generated with:	STM32CubeMX 5.6.0
Date	05/16/2020

1.2. MCU

MCU Series	STM32G4
MCU Line	STM32G4x1
MCU name	STM32G431KBTx
MCU Package	LQFP32
MCU Pin number	32

2. Pinout Configuration



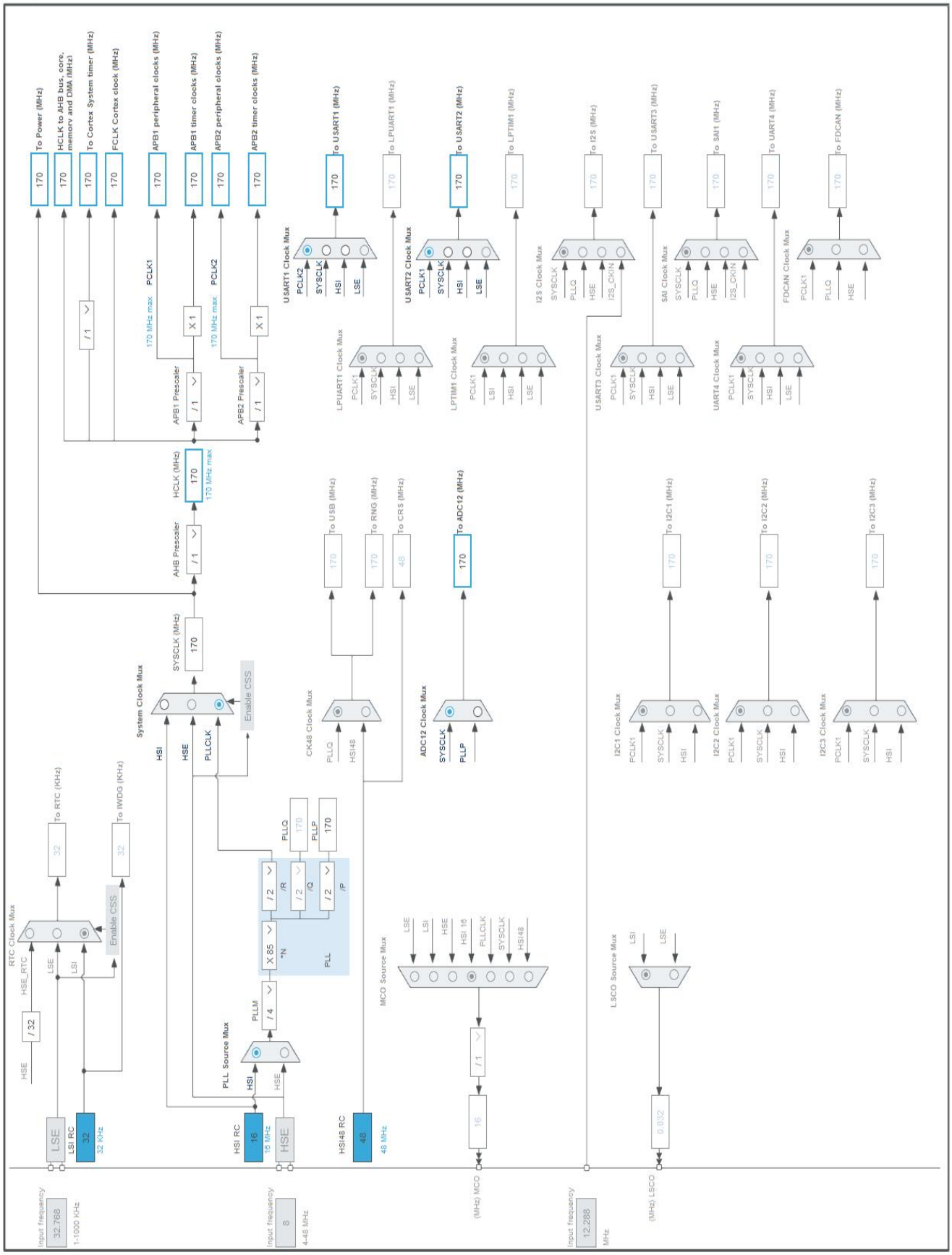
3. Pins Configuration

Pin Number LQFP32	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VDD	Power		
5	PA0 *	I/O	GPIO_Output	OLED_DC
6	PA1 *	I/O	GPIO_Output	OLED_RST
7	PA2	I/O	USART2_TX	USART2_TX [ST-LINKV3E_VCP_RX]
8	PA3	I/O	USART2_RX	USART2_RX [ST-LINKV3E_VCP_TX]
9	PA4	I/O	ADC2_IN17	BAT_DIV
10	PA5	I/O	SPI1_SCK	UI_SCK
12	PA7 *	I/O	GPIO_Input	VSRC
14	VSSA	Power		
15	VDDA	Power		
16	VSS	Power		
17	VDD	Power		
18	PA8 *	I/O	GPIO_Output	BRK_CTRL
19	PA9	I/O	USART1_TX	
20	PA10	I/O	USART1_RX	
21	PA11 *	I/O	GPIO_Output	KEYPAD_PL
22	PA12 *	I/O	GPIO_Output	OLED_CS
23	PA13	I/O	SYS_JTMS-SWDIO	T_SWDIO
24	PA14	I/O	SYS_JTCK-SWCLK	T_SWCLK
26	PB3 **	I/O	SYS_JTDO-SWO	T_SWO
27	PB4	I/O	SPI1_MISO	UI_MISO
28	PB5	I/O	SPI1_MOSI	UI_MOSI
31	PB8-BOOT0 *	I/O	GPIO_Output	LD2 [green]
32	VSS	Power		

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	Blinky
Project Folder	C:\Users\Kyle\STM32CubeIDE\workspace_1.3.0\Blinky
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_G4 V1.2.0

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	Yes

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32G4
Line	STM32G4x1
MCU	STM32G431KBTx
Datasheet	DS12589_Rev0

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

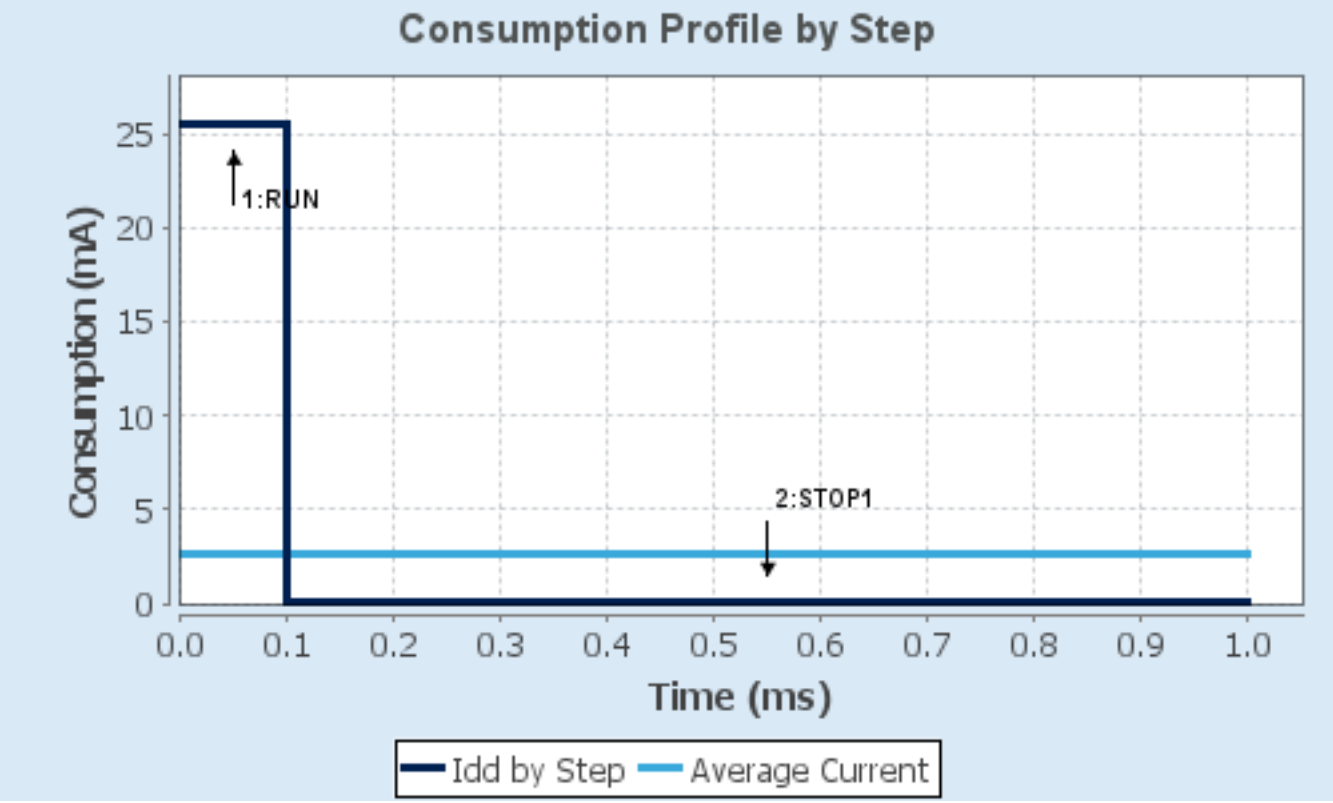
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP1
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-Boost	NoRange
Fetch Type	FLASH/ART	NA
CPU Frequency	170 MHz	0 Hz
Clock Configuration	HSE BYP PLL	ALL CLOCKS OFF
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	25.5 mA	59 µA
Duration	0.1 ms	0.9 ms
DMIPS	213.0	0.0
Ta Max	124.19	129.99
Category	In DS Table	In DS Table

6.5. RESULTS

Sequence Time	1 ms	Average Current	2.6 mA
Battery Life	1 month, 23 days, 22 hours	Average DMIPS	212.5 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
25
20
15
10
5
0
1:RUN
2:STOP1
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. IPs and Middleware Configuration

7.1. ADC2

mode: IN17 Single-ended

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**Asynchronous clock mode divided by 256 ***
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Gain Compensation	0
Scan Conversion Mode	Disabled
End Of Conversion Selection	End of single conversion
Low Power Auto Wait	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
Overrun behaviour	Overrun data preserved

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 17
Sampling Time	2.5 Cycles
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.2. GPIO

7.3. RCC

7.3.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Disabled
Data Cache	Enabled
Flash Latency(WS)	8WS (7 CPU cycle)

RCC Parameters:

HSI Calibration Value	64
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1 boost

Peripherals Clock Configuration:

Generate the peripherals clock configuration	TRUE

7.4. SPI1

Mode: Full-Duplex Master

7.4.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**256 ***
Baud Rate	**664.062 KBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled

NSS Signal Type	Software

7.5. SYS

Debug: Serial Wire

Timebase Source: SysTick

mode: save power of non-active UCPD - deactive Dead Battery pull-up

7.6. TIM6

mode: Activated

7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**340 ***
Counter Mode	Up
Dithering	Disable
Counter Period (AutoReload Register - 16 bits value)	**46 ***
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.7. TIM7

mode: Activated

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**340 ***
Counter Mode	Up
Dithering	Disable
Counter Period (AutoReload Register - 16 bits value)	**6 ***
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.8. TIM15

mode: Clock Source

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**1000 ***
Counter Mode	Up
Dithering	Disable
Counter Period (AutoReload Register - 16 bits value)	**850 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.9. TIM16

mode: Activated

7.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**1000 ***
Counter Mode	Up
Dithering	Disable
Counter Period (AutoReload Register - 16 bits value)	**850 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	**Enable ***

7.10. TIM17

mode: Activated

7.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**2125 ***
Counter Mode	Up
Dithering	Disable
Counter Period (AutoReload Register - 16 bits value)	**625 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	**Enable ***

7.11. USART1

Mode: Asynchronous

7.11.1. Parameter Settings:

Basic Parameters:

Baud Rate	**250000 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	**2 ***

Advanced Parameters:

Data Direction	**Transmit Only ***
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	clock /1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.12. USART2

Mode: Asynchronous

7.12.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	clock /1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC2	PA4	ADC2_IN17	Analog mode	No pull-up and no pull-down	n/a	BAT_DIV
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	UI_SCK
	PB4	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	UI_MISO
	PB5	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	UI_MOSI
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	T_SWDIO
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	T_SWCLK
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	USART2_TX [ST-LINKV3E_VCP_RX]
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	USART2_RX [ST-LINKV3E_VCP_TX]
Single Mapped Signals	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	T_SWO
GPIO	PA0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OLED_DC
	PA1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OLED_RST
	PA7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	VSRC
	PA8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	BRK_CTRL
	PA11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	KEYPAD_PL
	PA12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OLED_CS
	PB8-BOOT0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [green]

8.2. DMA configuration

DMA request	Stream	Direction	Priority
USART1_TX	DMA1_Channel1	Memory To Peripheral	Low
SPI1_TX	DMA1_Channel2	Memory To Peripheral	Low

USART1_TX: DMA1_Channel1 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

SPI1_TX: DMA1_Channel2 DMA request Settings:

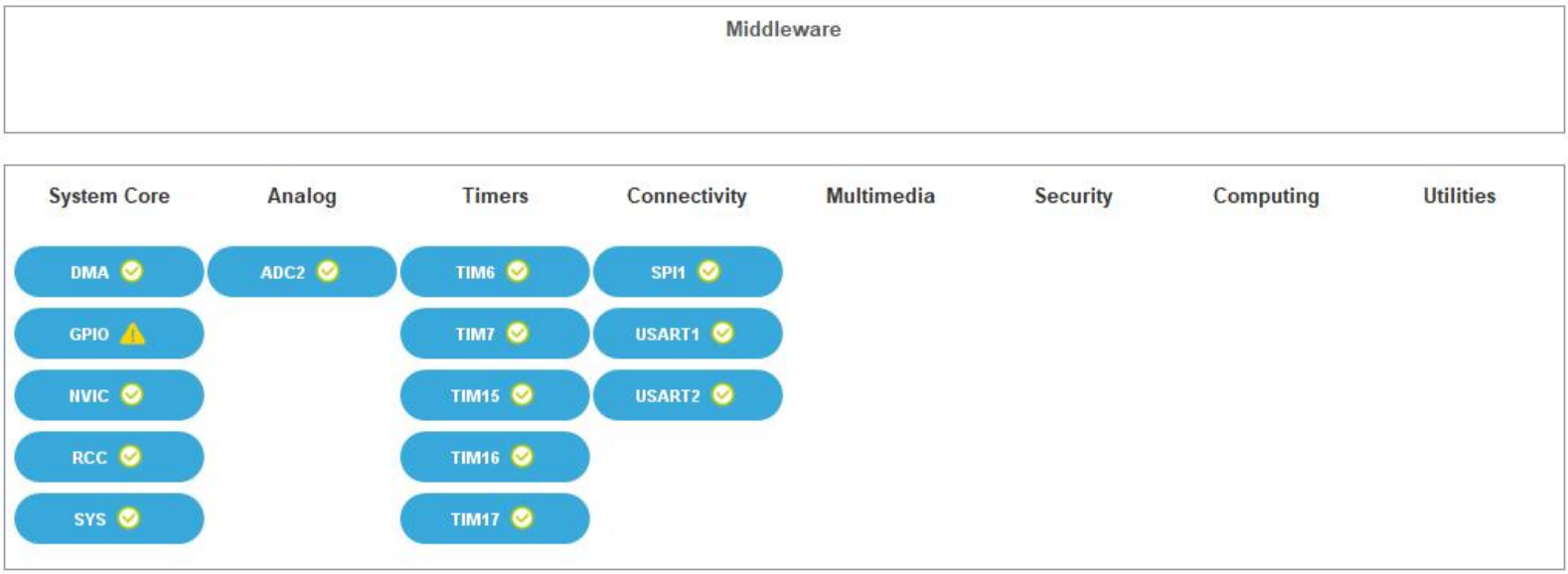
Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel1 global interrupt	true	0	0
DMA1 channel2 global interrupt	true	0	0
ADC1 and ADC2 global interrupt	true	0	0
TIM1 break interrupt and TIM15 global interrupt	true	0	0
TIM1 update interrupt and TIM16 global interrupt	true	0	0
TIM1 trigger and commutation interrupts and TIM17 global interrupt	true	0	0
SPI1 global interrupt	true	0	0
USART1 global interrupt / USART1 wake-up interrupt through EXTI line 25	true	0	0
TIM6 global interrupt, DAC1 and DAC3 channel underrun error interrupts	true	0	0
TIM7 global interrupt	true	0	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/38/39/40/41	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
USART2 global interrupt / USART2 wake-up interrupt through EXTI line 26	unused		
FPU global interrupt	unused		

*** User modified value**

9. Predefined Views - Category view : Current



10. Software Pack Report