# 8-Bit CPU Manual

Breadboard Computing

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## 1 Overview

### 2 Processor Architecture

#### 2.1 Registers:

- $\diamond$  A Register: REG\_A\_0, REG\_A\_1, ..., REG\_A\_7
- $\diamond$  B Register: REG\_B\_0, REG\_B\_1, ..., REG\_B\_7
- $\diamond \ \, \text{Temporary Register: REG\_TMP\_00, REG\_TMP\_01, } \ldots, \, \text{REG\_TMP\_15}$
- $\diamond$  Memory Address Register: REG\_MAR\_00, REG\_MAR\_01, ..., REG\_MAR\_15
- ♦ Memory Buffer Register: REG\_MBR\_0, REG\_MBR\_1, ..., REG\_MBR\_7
- $\diamond$  Flag Register: REG\_F\_0, REG\_F\_1, ..., REG\_F\_7
- $\diamond \ \, \text{Instruction Register: REG\_IR\_0, REG\_IR\_1, } \ldots, \, \text{REG\_IR\_7}$

#### 2.2 Buses

- $\diamond$  Data Bus: BUS\_0, BUS\_1, ..., BUS\_7
- ♦ Address Bus: ADDRESS\_00, ADDRESS\_01, ..., ADDRESS\_15

#### 2.3 Flags

- $\diamond$  REG\_F\_0: sign flag(1  $\rightarrow$  result is negative; 0  $\rightarrow$  result is non-negative)
- $\diamond$  REG\_F\_1: parity flag(1  $\rightarrow$  result is odd; 0  $\rightarrow$  result is even)
- $\diamond$  REG\_F\_2: zero flag(1  $\rightarrow$  result is not equal to zero; 0  $\rightarrow$  result is equal to zero)
- $\diamond$  REG\_F\_3: carry flag(for unsigned number operations: 1  $\rightarrow$  result is out of range; 0  $\rightarrow$  result is correct)
- $\diamond$  REG\_F\_4: overflow flag(for signed number operations: 1  $\rightarrow$  result is out of range; 0  $\rightarrow$  result is correct)

#### 2.4 Signals

Clock			
CLK	signal generated by clock with specified frequency		
CLK	inverted signal generated by clock with specified frequency		

Table 1: Clock Signals Description

Arithmetic Logic Unit			
REG_A_LOAD	A0	load data from data bus to register A	combined with CLK
REG_B_LOAD	A1	load data from data bus to register B	combined with CLK
ALU_OPC_O	A2	bit 0 of operation code to perform	
ALU_OPC_1	A3	bit 1 of operation code to perform	
ALU_OPC_2	A4	bit 2 of operation code to perform	
ALU_OPC_3	A5	bit 3 of operation code to perform	
ALU_OPC_4	A6	bit 4 of operation code to perform	
REG_F_LOAD	A7	load flags of current operation to flag register	combined with CLK
REG_F_OUT	В0	pass data from flag register to data bus	
ALU_OUT	B1	pass current operation result to data bus	

Table 2: Arithmetic Logic Unit Signals Description

Data Bus - Address Bus Connector			
REG_TMPH_LOAD	B2	load data from data/address bus to higher bits of temporary register	combined with CLK
REG_TMPL_LOAD	В3	load data from data/address bus to lower bits of temporary register	combined with CLK
REG_TMPH_OUT	В4	pass data from higher bits of temporary register to data/address bus	
REG_TMPL_OUT	В5	pass data from lower bits of temporary register to data/address bus	
REG_TMP_PASS_ADDRESS	В6	enable passing address from address bus/temporary register to temporary register/address bus	
REG_TMPH_PASS_DATA	В7	enable passing data from data bus/msb of temporary register to msb of temporary register/data bus	
REG_TMPL_PASS_DATA	C0	enable passing data from data bus/lsb of temporary register to lsb of temporary register/data bus	
REG_TMP_ADDRESS_DIR	C1	address direction selector: from address bus/temporary register to temporary register/address bus	
REG_TMPH_DATA_DIR	C2	data flow direction selector: from data bus/msb of temporary register to msb of temporary register/data bus	
REG_TMPL_DATA_DIR	С3	data flow direction selector: from data bus/lsb of temporary register to lsb temporary register/data bus	

Table 3: Data Bus - Address Bus Connector Signals Description

Program Counter			
PC_LOAD	C4	load address from address bus to program counter	
PC_RST	C5	set program counter to 0x0000	
PC_TICK	C6	increment program counter	$\begin{array}{c} \text{combined with} \\ \hline \hline \textbf{CLK} \end{array}$
PC_OUT	C7	pass data from program counter to address bus	

Table 4: Program Counter Signals Description

#### 2.5 Instructions

### 2.6 Instruction Cycle

- $\diamond$  Fetch(fixed number of cycles)
- ♦ Decode(variable number of cycles)
- $\diamond$  Execute(variable number of cycles)

Stack Counter			
STC_LOAD	D0	load address from address bus to stack counter	
STC_RST	D1	set stack counter to 0x0000	
STC_TICK	D2	increment/decrement stack counter; increment/decrement depends on mode	combined with CLK
STC_MODE	D3	stack counter operation selector: increment or decrement	
STC_OUT	D4	pass data from stack counter to address bus	

Table 5: Stack Counter Signals Description

Memory Unit			
REG_MAR_LOAD	D5	load data from address bus to memory address register	combined with CLK
REG_MBR_LOAD	D6	load data from data bus to memory buffer register	combined with CLK
MEM_OUT	D7	read data to memory buffer register from memory at address from memory address register	
MEM_IN	E0	write data from memory buffer register to memory at address from memory address register	
MEM_PART	E1	additional bit of memory address; it is used to easy memory division	
ZERO_PAGE	E2	clear higher bits of memory address; it is used to faster access to memory at low addresses	
REG_MBR_WORD_DIR	E3	data flow direction selector: pass data from data bus/memory buffer register to memory buffer register/data bus	
REG_MAR_USE_BTTNS	E4	use buttons to enter value to set to memory address register	
REG_MBR_USE_BTTNS	E5	use buttons to enter value to set to memory buffer register	
REG_MBR_USE_BUS	E6	use bus to pass value to set to memory buffer register or get value from memory buffer register	

Table 6: Memory Unit Signals Description

#### 2.7 Decoder

Input:  $MI_7I_6I_5I_4I_3I_2I_1I_0C_3C_2C_1C_0$ :

- $\diamond~M$  operating mode,
- $\diamond\ I_7I_6I_5I_4I_3I_2I_1I_0$  instruction,
- $\diamond~C_3C_2C_1C_0$  microcode counter

Control Unit			
REG_IR_LOAD	F0	load instruction from data bus	$\begin{array}{c} \text{combined with} \\ \hline \hline \text{CLK} \end{array}$
MCC_TICK	F1	increment microcode counter	$\begin{array}{c} \text{combined with} \\ \hline \hline \textbf{CLK} \end{array}$
MCC_RST	F2	set microcode counter to 0x0000	

Table 7: Control Unit Signals Description