California Polytechnic State University Pomona
DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING

Circuit Analysis 2 Laboratory

ECE 2101L-03
Report #12

LAB 12 – Four-pole Low-Pass Filter

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Presented to
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Introduction:

In this lab experiment, we will be analyzing a butter worth low-pass active filter. More specifically, we will analyze this filter's flat passband. This filter will consist of resistors, capacitors, and two operational amplifiers. The filter produces a high output voltage and drops quickly to near zero voltage as the frequency is increased. The advantage of using two op-amps is due to how quickly the roll-off happens compared to circuits without op-amps. In the second half of our lab, we will simulate a state-variable filter. These types of filters are designed for high Q band-pass filters but have separate low-pass and high-pass outputs. These filters come in IC packages and allow the user to control gain, bandwidth, and Q using external resistors.

Component List:

Resistors: one 1.5 kΩ, four 8.2 kΩ, two 10 kΩ, one 22 kΩ, one 27 kΩ
Capacitors: four 0.01 µF, four 1.0 µF
Two LM741C op-amps

Part 1: Butter worth low-pass active filter

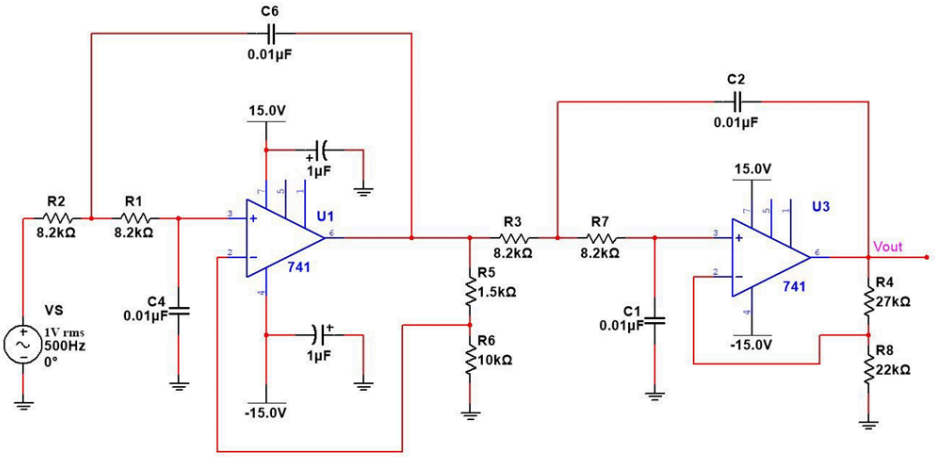


Figure 1: Circuit Schematic of Butter Worth Low-Pass Active Filter

PCB Design:

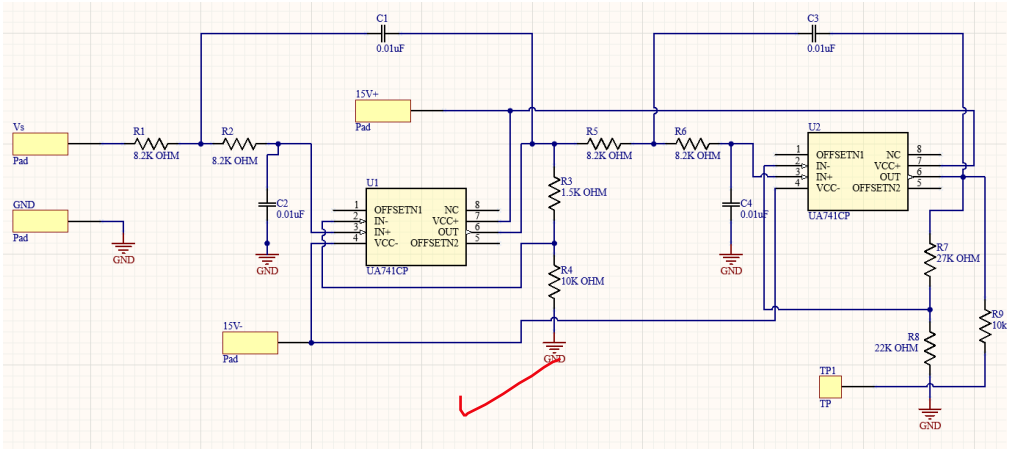


Figure 2: PCB Schematic of Butter Worth Low-Pass Active Filter

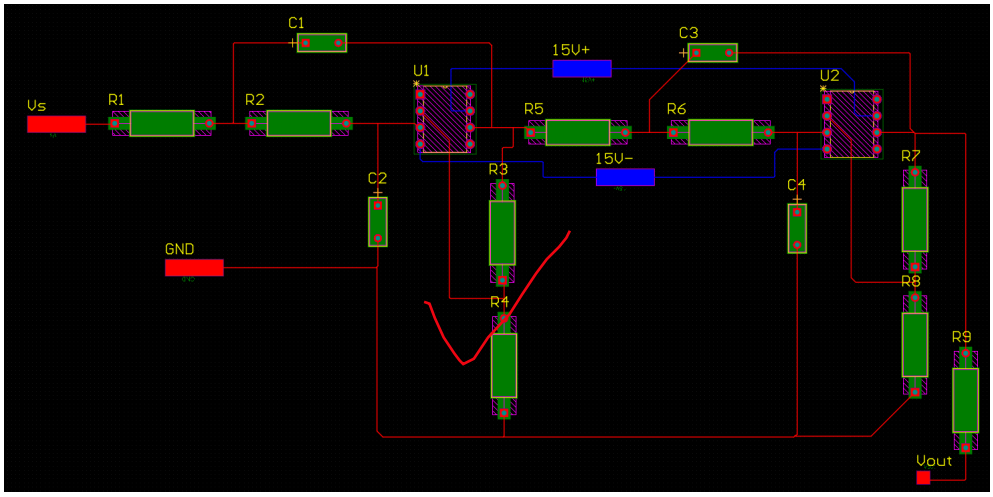


Figure 3: PCB Design of Butter Worth Low-Pass Active Filter

Simulation:

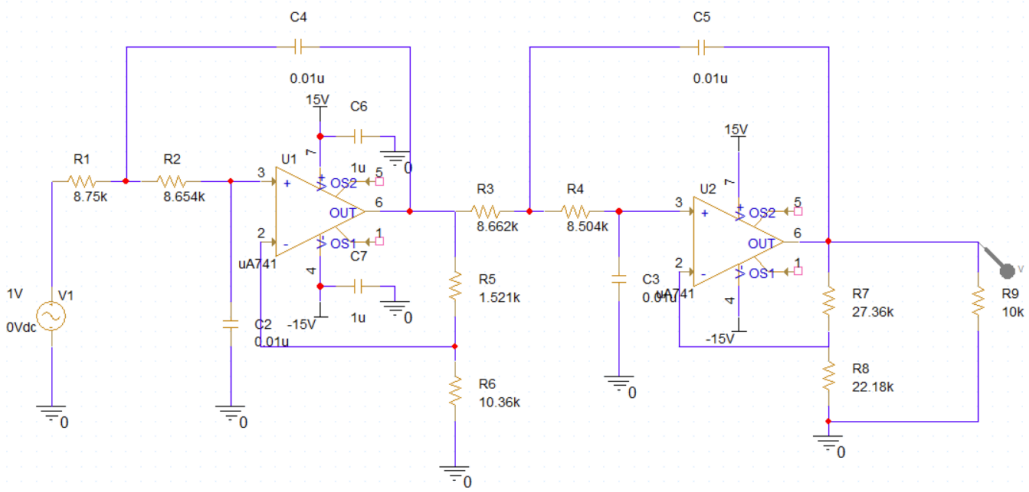


Figure 4: Simulation Schematic of Butter Worth Low-Pass Active Filter

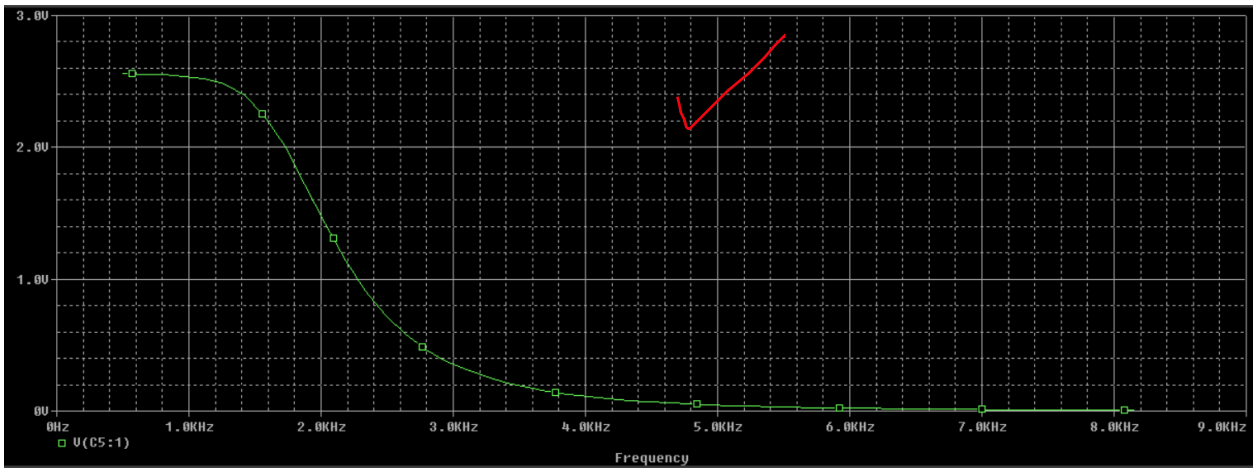


Figure 5: Simulation Results In Linear RMS Voltage

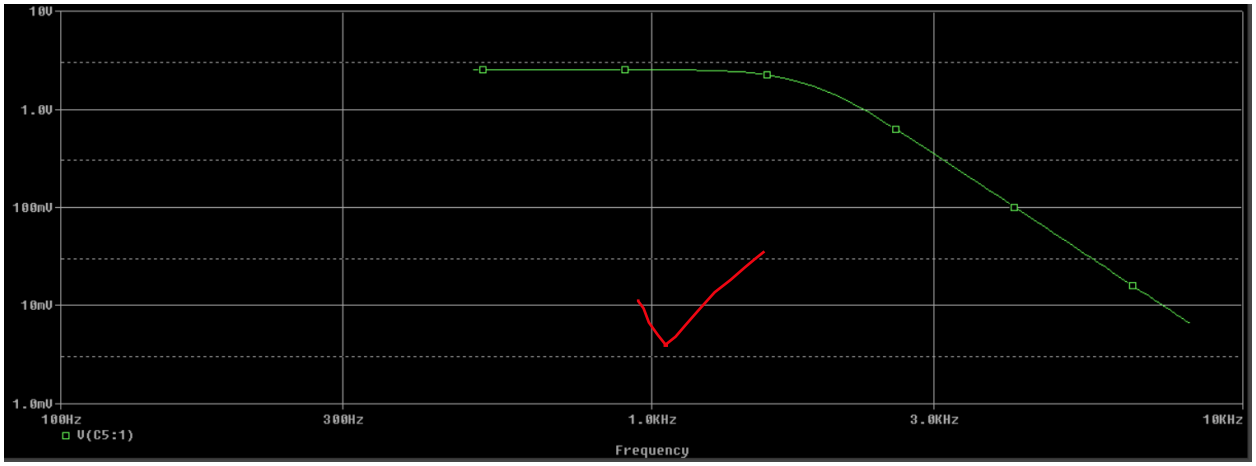


Figure 6: Simulation Results in Log RMS Voltage

Measurements:

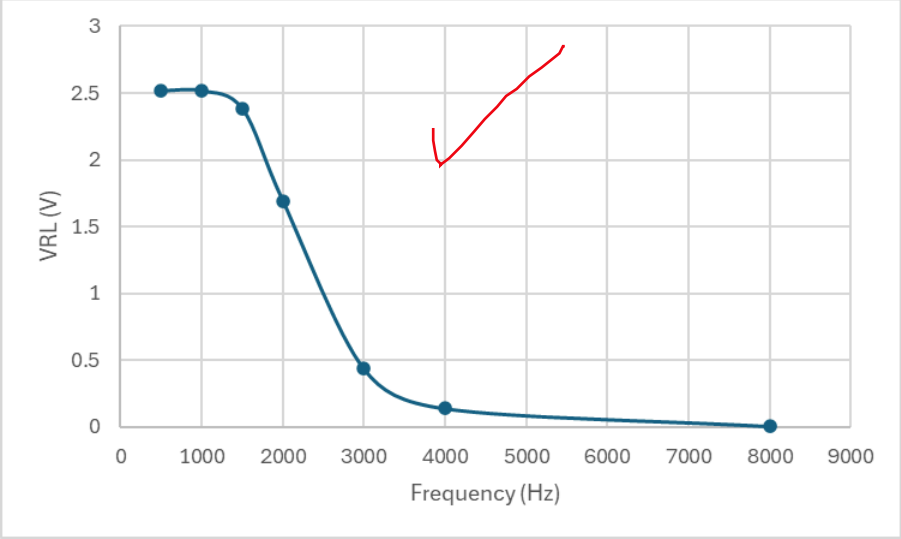
Component	Listed Value	Measured values			
		A1	B1	A2	B2
R_{A1},R_{B1},R_{A2},R_{B2}	8.2 kΩ	8.750 k	8.654 k	8.662 k	8.504 k
C_{A1},C_{A2},C_{B1},C_{B2}	0.01 µF	0.01µ	0.01µ	0.01µ	0.01µ
R_{i1}	10 kΩ	10.36k			
R_{f1}	1.5 kΩ	1.521k			
R_{i2}	22 kΩ	22.18k			
R_{f2}	27 kΩ	27.36k			

Table 1: Resistors and Capacitors Measurements

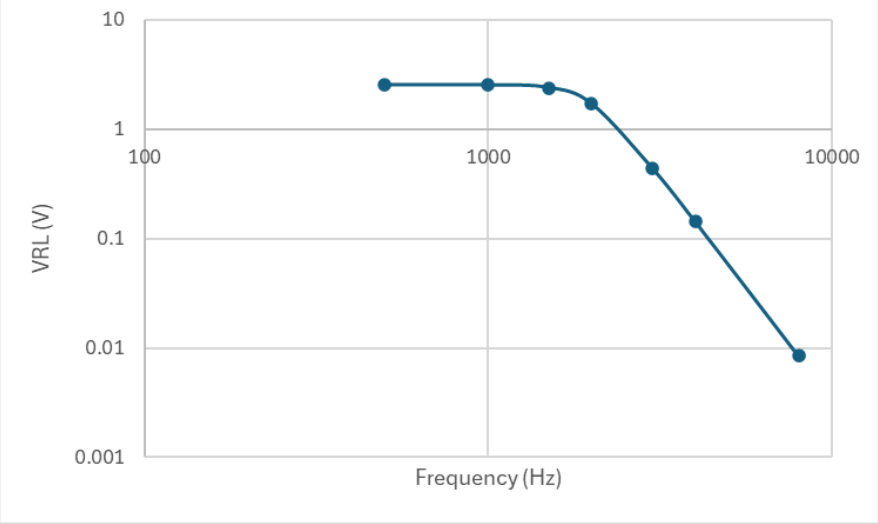
Frequency	V_{RL} (V) (peak to peak)	V_{RL} (V rms)	V_{RL} (V rms) (Simulation)
500 Hz	7.11	2.514	2.56

1000 Hz	7.11	2.514	2.55
1500 Hz	6.73	2.379	2.40
2000 Hz	4.78	1.690	1.67
3000 Hz	1.235	0.4366	0.430
4000 Hz	0.401	0.1418	0.138
8000 Hz	0.0238	0.008414	0.00909

Table 2: Voltages Over Load Resistance Across Frequencies



Plot 1: Frequency vs Vout with linear axes

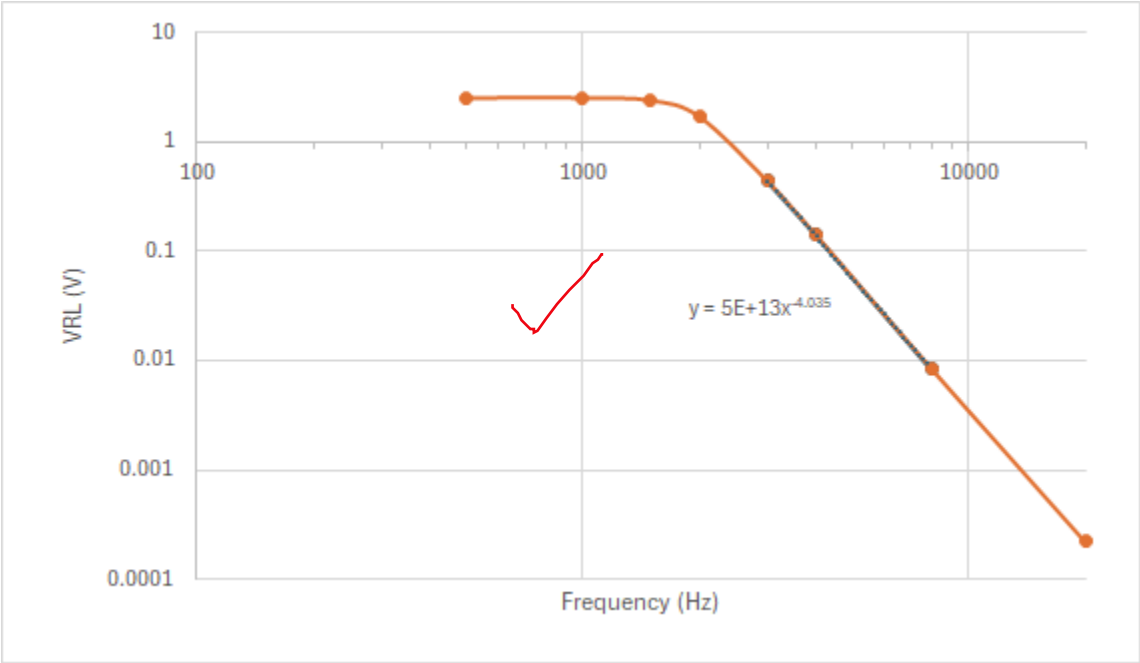


Plot 2: Frequency vs Vout with logarithm axes

Cutoff frequency = 1831.5 Hz

The measured voltage gain in the passband is $\frac{Vout}{Vin} = \frac{2.514V}{1V} = 2.514$

It should be 2.5613 = $(1 + \frac{1.5k}{10k})(1 + \frac{27k}{22k})$



Plot 3: 20kHz Prediction Using Trendline Across 3kHz and 8kHz

Vout at frequency of 20kHz is 0.000221V (rms)

The predicted value for VRL (dB) at 22kHz is -73.454.
The known value for VRL (dB) at 2kHz is 4.55.
So the roll of for my filter across 10kHz(22k-2k) is -78.004 (-73.454-4.55).
The percent difference between the theoretical -80dB/decade is 2.495%.

Part 2- State Variable Filter

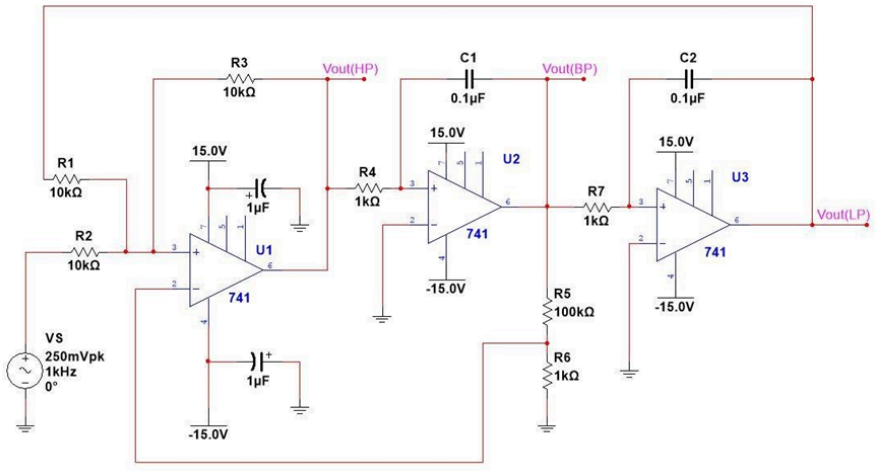


Figure 7: State Variable Filter Circuit Diagram

PCB Design:

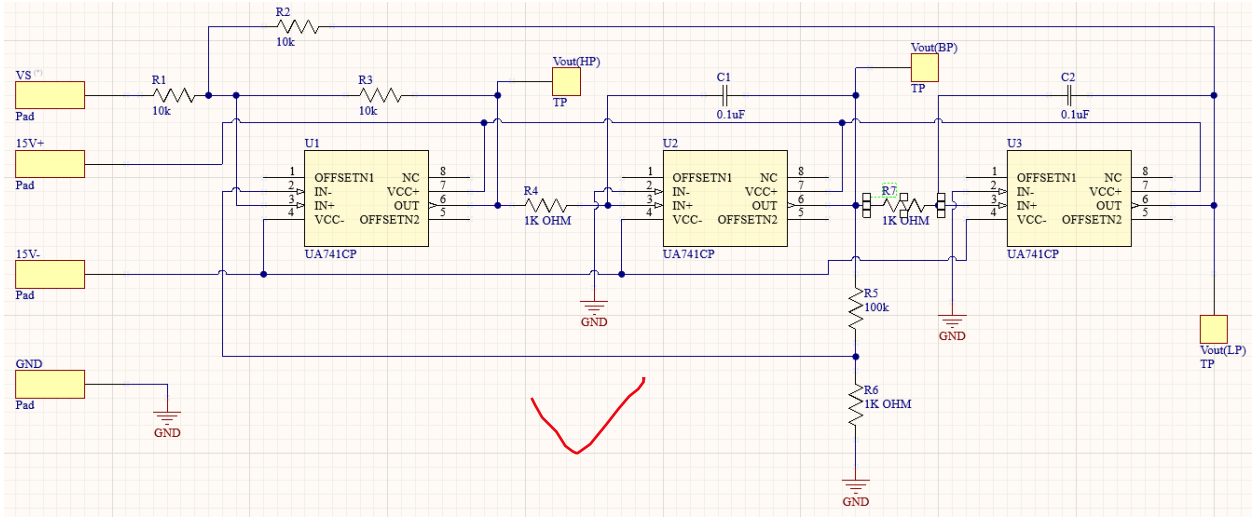


Figure 8: PCB Schematic of State Variable Filter

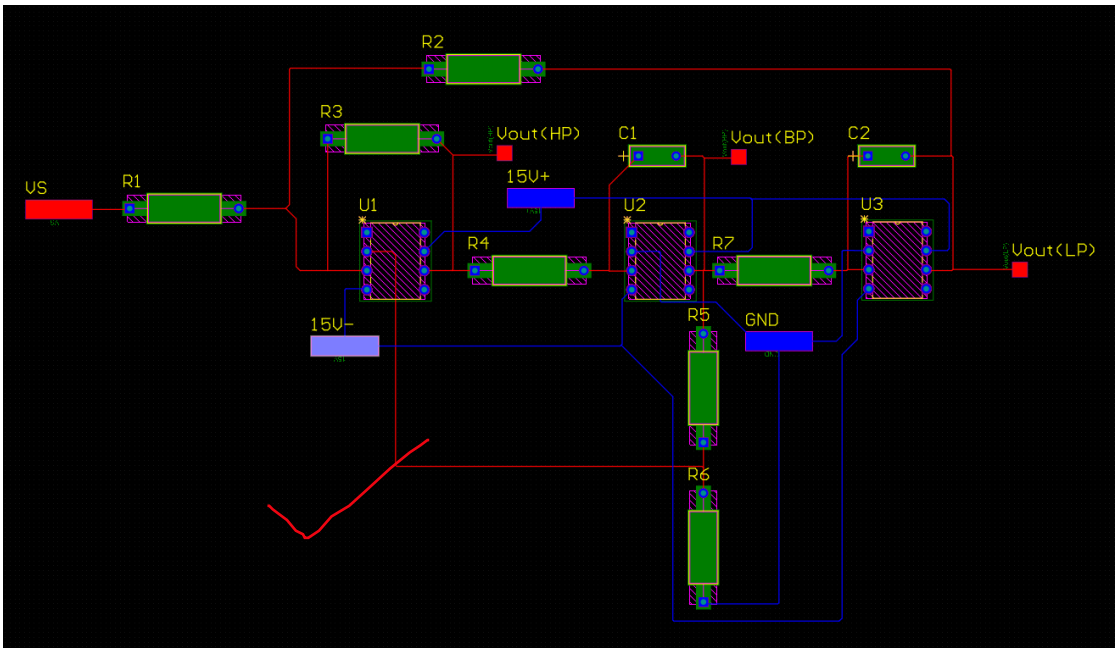


Figure 9: PCB Design of State Variable Filter

Simulation:

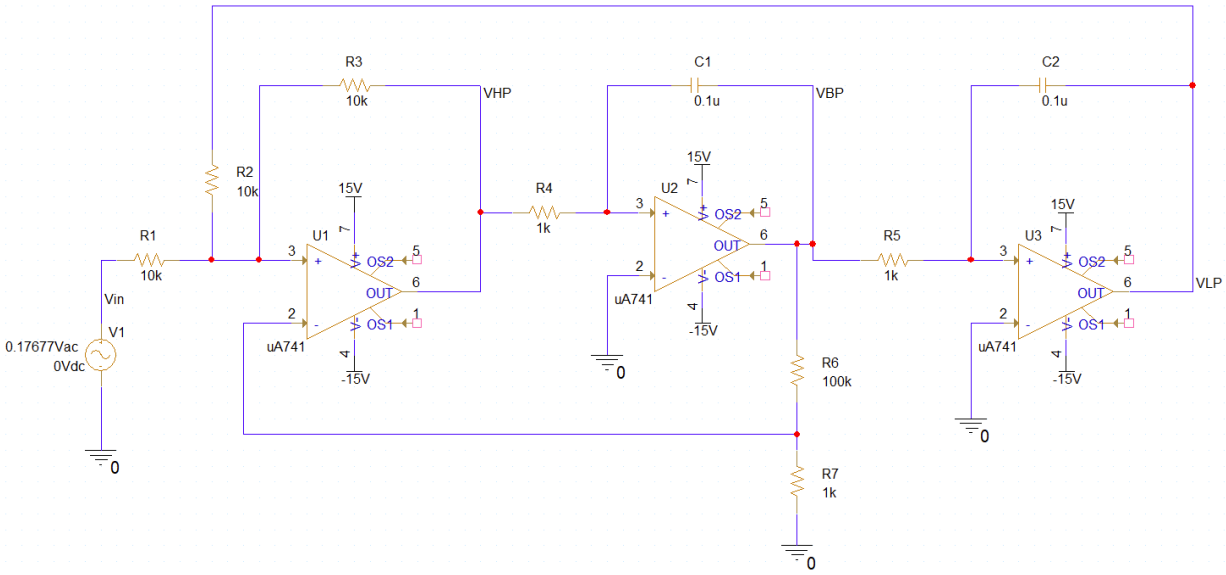
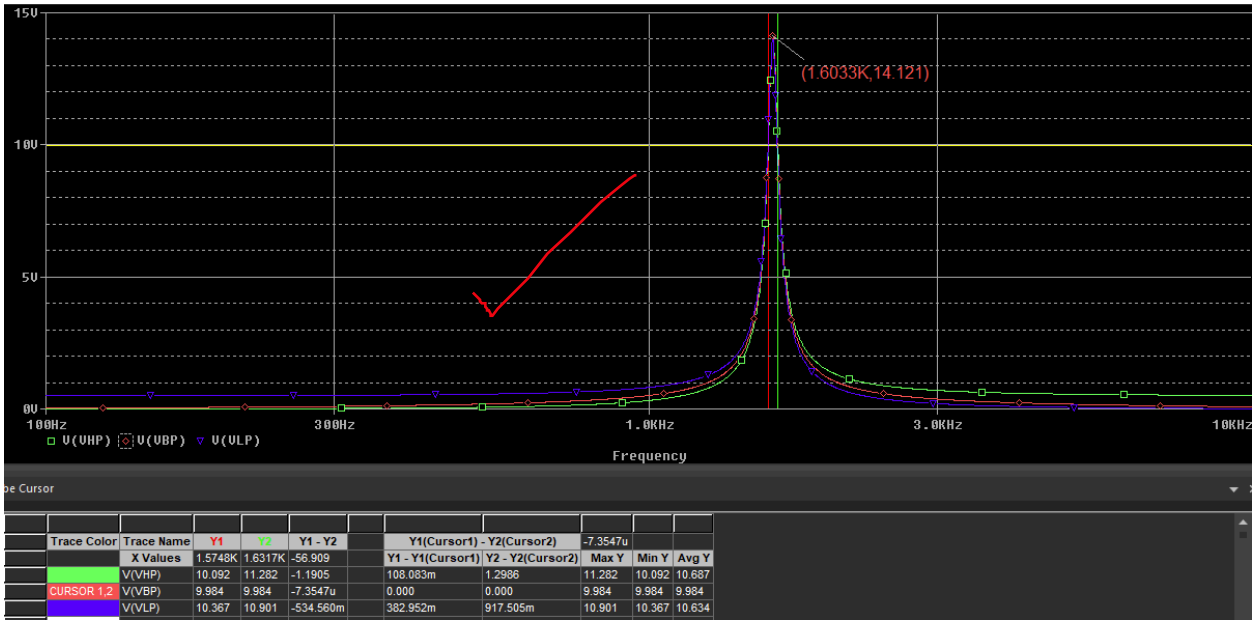


Figure 10: Simulation Schematic of State Variable Filter



	Trace Color	Trace Name	Y1	Y2	Y1 - Y2	Y1(Cursor1) - Y2(Cursor2)		-7.3547u		
		X Values	1.5748K	1.6317K	-56.909	Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
		V(VHP)	10.092	11.282	-1.1905	108.083m	1.2986	11.282	10.092	10.687
	CURSOR 1,2	V(VBP)	9.984	9.984	-7.3547u	0.000	0.000	9.984	9.984	9.984
		V(VLP)	10.367	10.901	-534.560m	382.952m	917.505m	10.901	10.367	10.634

Figure 11: Simulation Results Showing Upper Bound, Lower Bound, and Center Frequencies
Note: The y-axis shows peak-to-peak voltage on a linear scale.

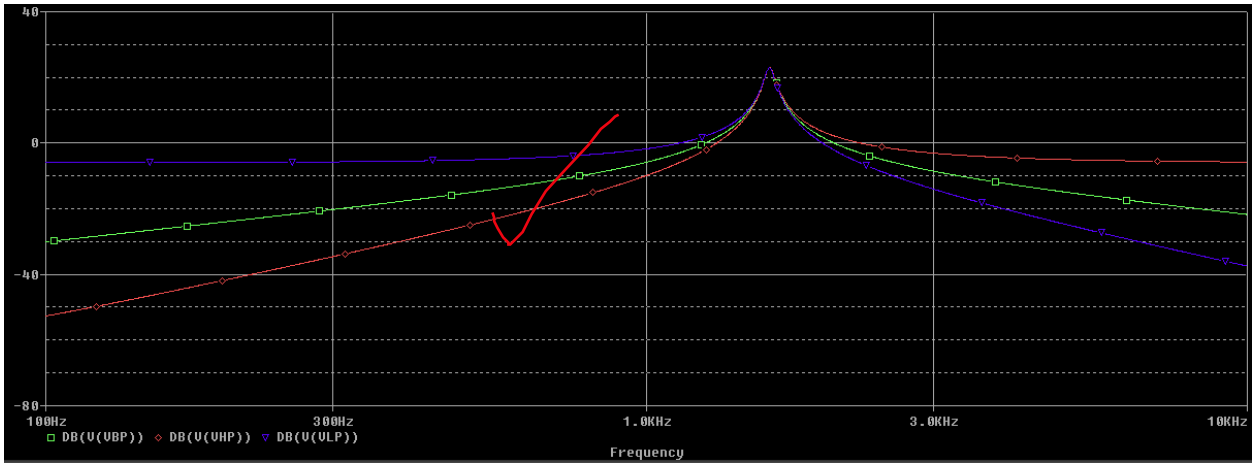
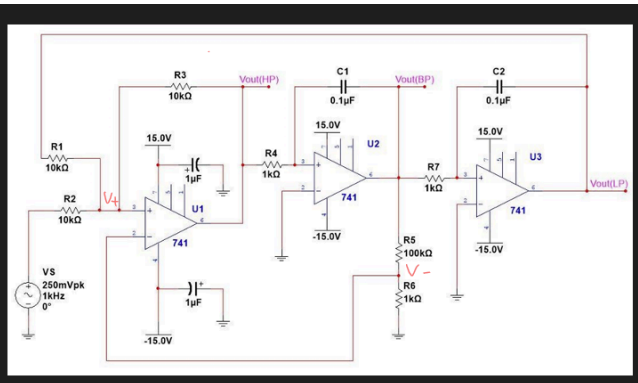


Figure 12: Y-axis In DB Scale Showing The Three Variable States

Calculations:



At node V+ for U1

$$\frac{V_S - V_+}{R_2} - \frac{(V_+ - V_{LP})}{R_1} - \frac{(V_+ - V_{HP})}{R_3} = 0$$

$$\frac{V_S}{R_2} - \frac{V_+}{R_2} - \frac{V_+}{R_1} + \frac{V_{LP}}{R_1} - \frac{V_+}{R_3} + \frac{V_{HP}}{R_3} = 0$$

$$-V_+\left(\frac{1}{R_2} + \frac{1}{R_1} + \frac{1}{R_3}\right) + \frac{V_S}{R_2} + \frac{V_{LP}}{R_1} + \frac{V_{HP}}{R_3} = 0$$

$$\frac{V_S}{R_2} + \frac{V_{LP}}{R_1} + \frac{V_{HP}}{R_3} = V_+\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right)$$

$$V_+ = \frac{\frac{V_S}{R_2} + \frac{V_{LP}}{R_1} + \frac{V_{HP}}{R_3}}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}}$$

At node V- for U1

$$\frac{V_- - V_{BP}}{R_5} - \frac{V_-}{R_6} = 0$$

$$\frac{V_-}{R_5} - \frac{V_{BP}}{R_5} - \frac{V_-}{R_6} = 0$$

$$V_-\left(\frac{1}{R_5} - \frac{1}{R_6}\right) = \frac{V_{BP}}{R_5}$$

$$V_- = \frac{\frac{V_{BP}}{R_5}}{\frac{1}{R_5} - \frac{1}{R_6}}$$

For U_1

$V_+ = V_-$

$$\frac{\frac{V_S}{R_2} + \frac{V_{LP}}{R_1} + \frac{V_{HP}}{R_3}}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}} = \frac{\frac{V_{BP}}{R_5}}{\frac{1}{R_5} - \frac{1}{R_6}}$$

$R_1 = R_2 = R_3 = R_{10k}$

$$\frac{\frac{V_S + V_{LP} + V_{HP}}{R_{10k}}}{\frac{3}{R_{10k}}} = \frac{\frac{V_{BP}}{R_5}}{\frac{R_6 - R_5}{R_5 R_6}}$$

$$\frac{V_S + V_{LP} + V_{HP}}{3} = \frac{V_{BP} R_5 R_6}{R_5(R_6 - R_5)}$$

$$\frac{1}{3}V_S + \frac{1}{3}V_{LP} + \frac{1}{3}V_{HP} = V_{BP}\frac{R_6}{R_6 - R_5}$$

$$\frac{1}{3}V_{HP} = -\frac{1}{3}V_S + V_{BP}\frac{R_6}{R_6 - R_5} - \frac{1}{3}V_{LP}$$

$$V_{HP} = -V_S + V_{BP}\frac{3R_6}{R_6 - R_5} - V_{LP}$$

$$\frac{V_{out}}{V_{in}} = \frac{V_{LP}}{V_S} = \frac{-\frac{1}{RC}}{\frac{1}{RC} + \left(\frac{3R_6}{R_6 - R_5} \times \frac{1}{2\pi f_c RC}\right) + \frac{1}{(2\pi f_c RC)^2}}$$

$$= \frac{\frac{1}{RC}}{-\frac{1}{RC} - \left(\frac{3R_6}{R_6 - R_5} \times \frac{1}{2\pi f_c RC}\right) + \frac{1}{(2\pi f_c RC)^2}}$$

$$2\xi = \frac{-3R_6}{R_6 - R_5}, \quad Q = \frac{1}{2\xi} = \frac{R_6 - R_5}{-3R_6} = 33$$

Quantity	Computed	Simulated
Center Frequency, f_0	$= \frac{1}{2\pi RC} = \frac{1}{2\pi * 1k * 0.1u} =$ 1591.549 Hz	1621.8 Hz
V_{pp} (Center)		14.1193
Upper cutoff, f_{cu}		1.6317 kHz
Lower cutoff, f_{c1}		1.5748 kHz
Bandwidth, BW	$= \frac{f0}{Q} =$ 48.229Hz	56.9
Q	=33	28.502

Conclusion:

We began this experiment by measuring all of our components to make sure they were the correct values. After confirming our component values, we built our Butterworth low-pass active filter with a 10k load resistor. Once the circuit is built, we will set the voltage to 1.0 Vrms, and the frequency to 500 Hz, and then measure our load voltage (VRL). We will continue this process at the following frequencies: 1000 Hz, 1500 Hz, 2000 Hz, 3000 Hz, 4000 Hz, and 8000 Hz. Then we graphed our measured load voltage values as a function of frequency. We also graphed the Bode plot of Voltage vs Frequency. In the second half of this lab experiment, we simulated a State Variable Filter. With this simulation, we got our simulated: center frequency, Vpp, upper cutoff, lower cutoff, bandwidth, and quality factor. Lastly, we compared these to our computed center frequency, bandwidth, and quality factor. Overall, this lab was extremely insightful and allowed us to work with physical filters and analyze them in the real world.

Post Lab:

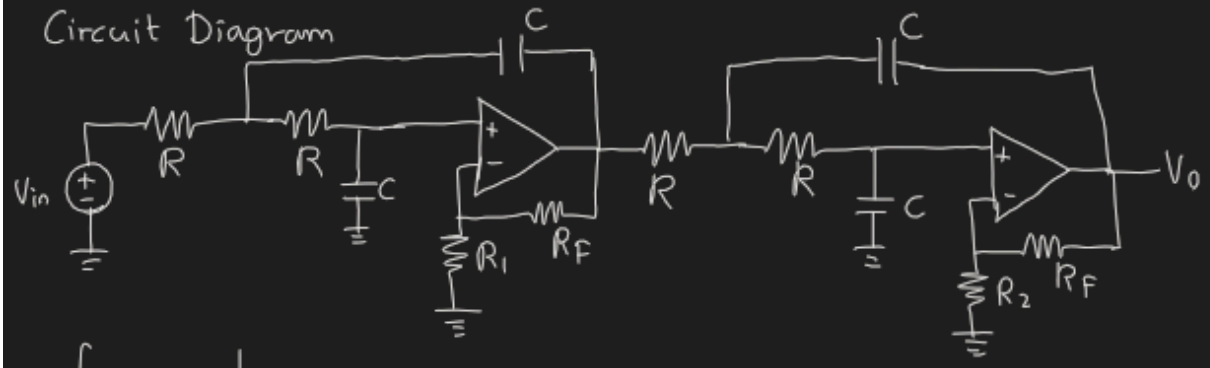
1. Design a fourth-order low-pass filter with a cutoff frequency of 500 Hz and a passband gain of 10. Use 1 mF capacitors. Sketch the Bode magnitude plot for this filter. Verify your design by simulation. Build a PCB for your design. Show both the schematic and layout and 3d model of your PCB. (5 points)

Calculation:

Post Lab 1:

Given: $f_c = 500Hz$, Passband gain = 10, $C = 1mF$

Circuit Diagram



$$f_c = \frac{1}{2\pi RC}$$

$$R = \frac{1}{2\pi C f_c} = \frac{1}{2\pi \times 1m \times 500} = 0.3183\Omega$$

No

$A_F = 10 = A_1 \times A_2$

Wrong

Let $A_1 = 5$, then $A_2 = 2$

-2

$A_1 = 1 + \frac{R_F}{R_1}$, Let $R_F = 4k\Omega$, $5 = 1 + \frac{4k}{R_1}$

$4 = \frac{4k}{R_1} \Rightarrow R_1 = \frac{4k}{4} = 1k\Omega$

$A_2 = 1 + \frac{R_F}{R_2}$, $R_F = 4k\Omega$, $2 = 1 + \frac{4k}{R_2}$

$1 = \frac{4k}{R_2} \Rightarrow R_2 = 4k\Omega$

PCB Design:

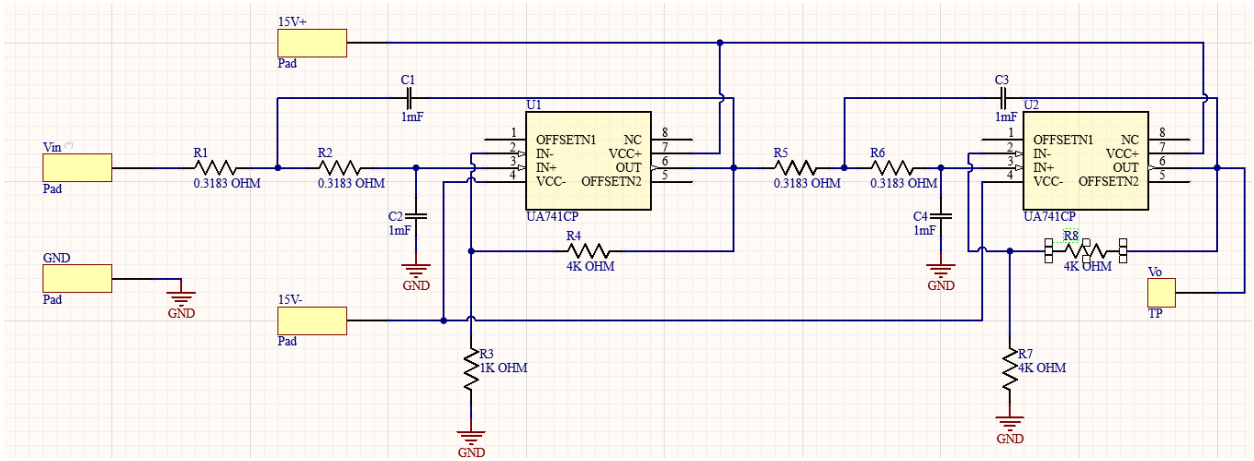


Figure 13: PCB Schematic of Post Lab 1

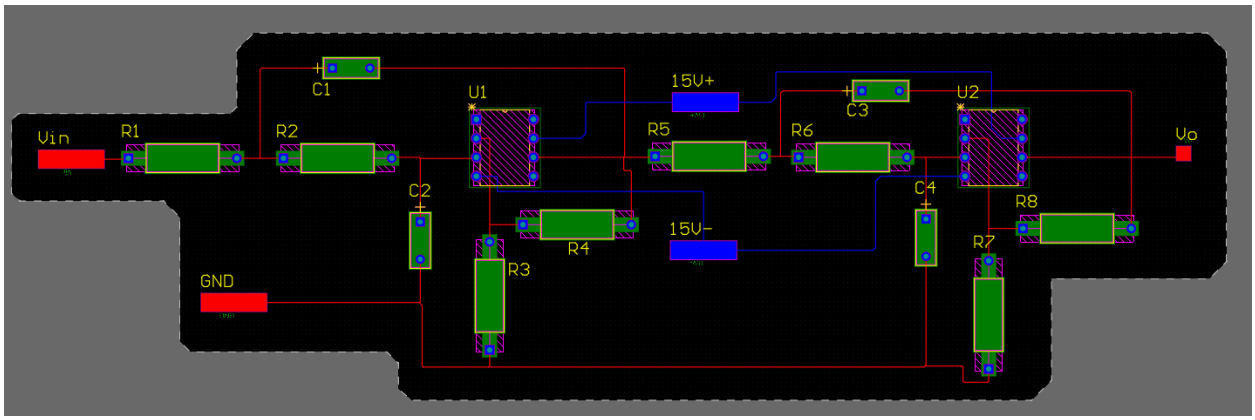


Figure 14: PCB Design for Post Lab 1

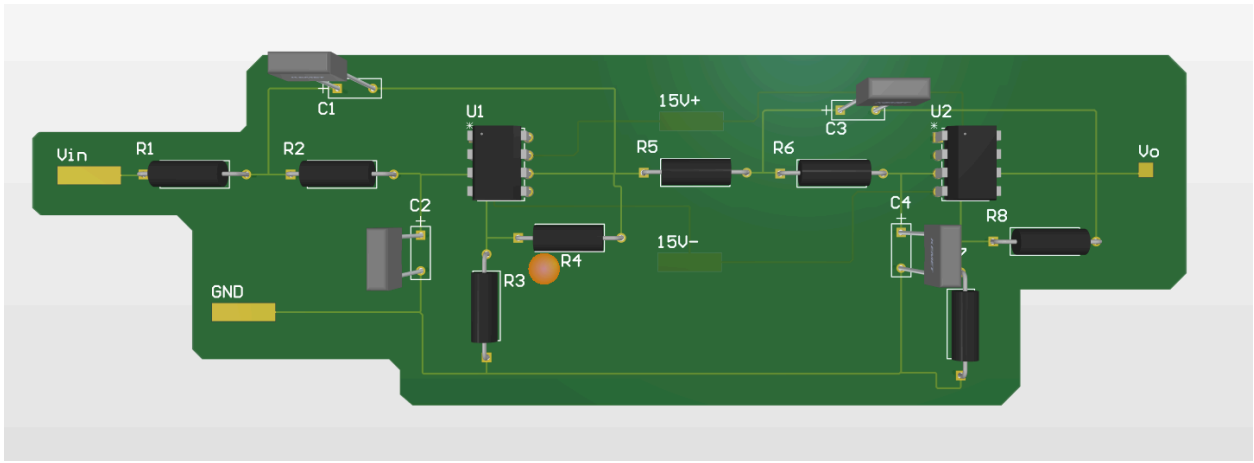


Figure 15: PCB Design in 3D for Post Lab 1

Simulation:

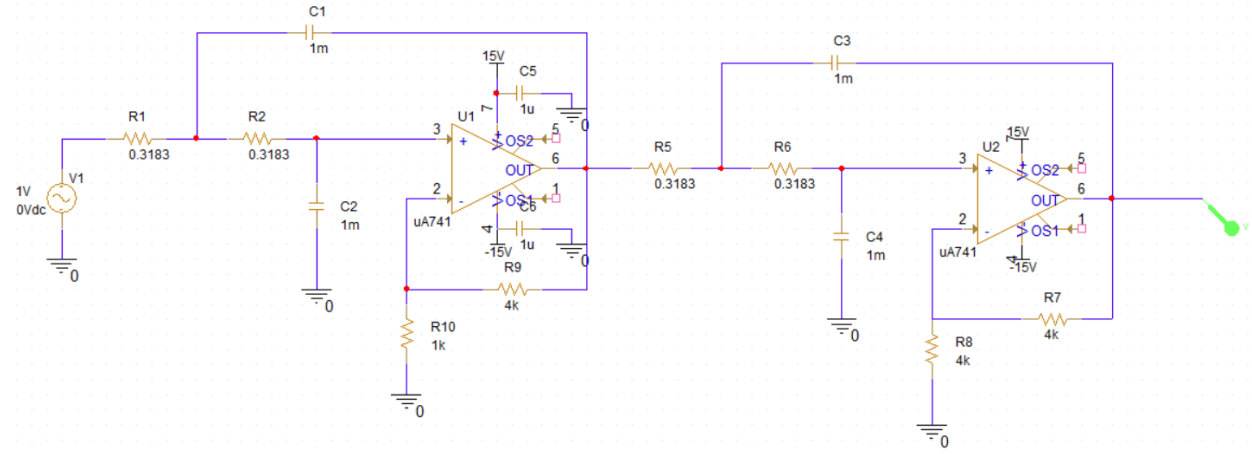


Figure 16: Simulation Schematic of Post Lab 1

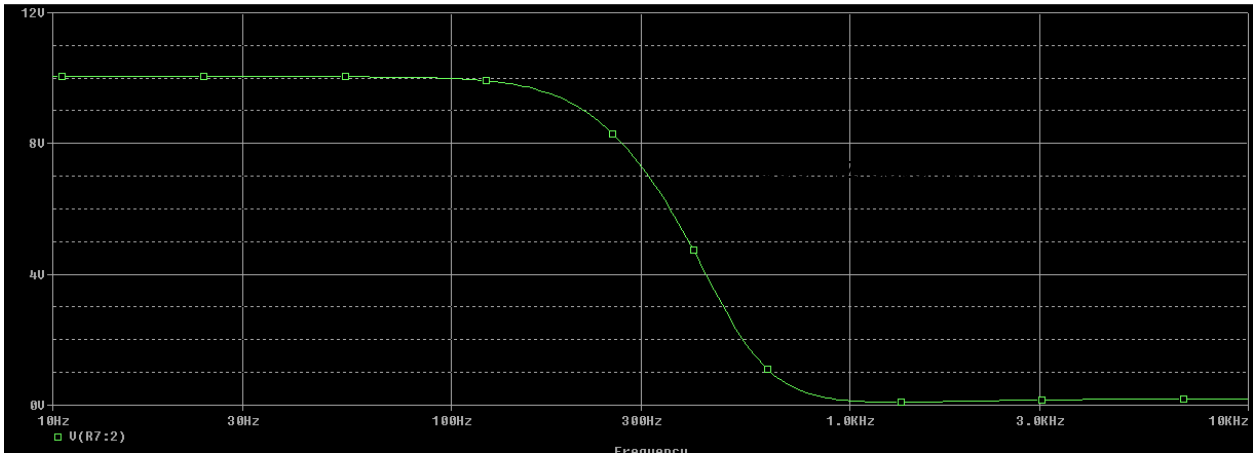


Figure 17: Simulation Results Showing Linear Performance of the Filter

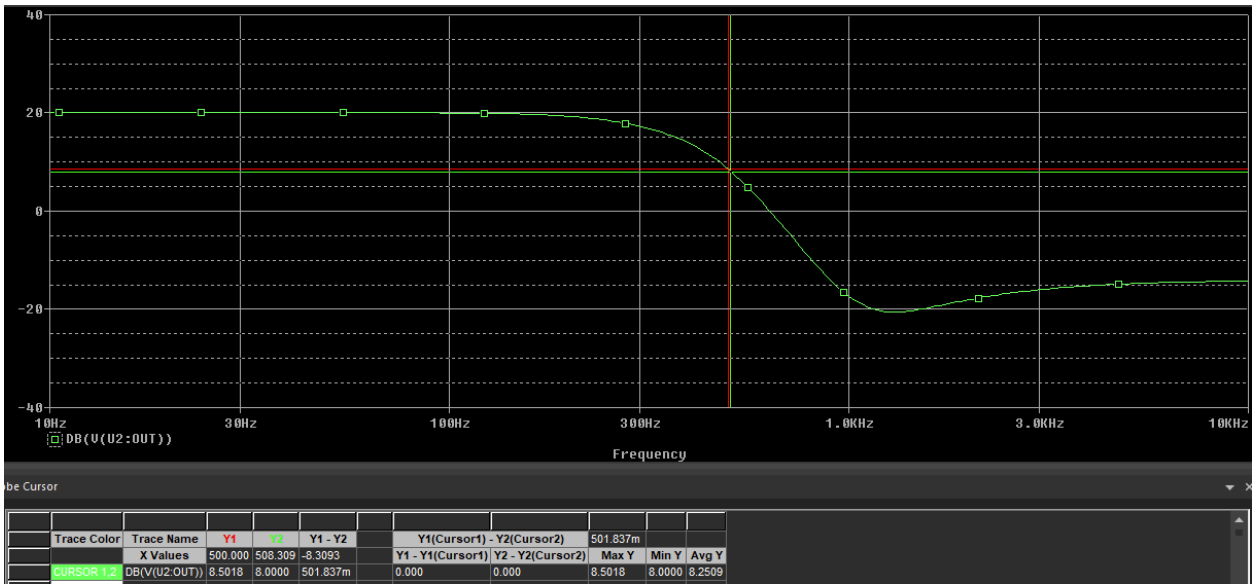


Figure 18: Simulation Results Showing dB Scale Performance & 8dB Cut-Off Frequency

Note: Since the filter is fourth order and has a gain of 20dB, fc can be found at 20dB - (3dB*n) where n is the order of the filter. Thus, the cut-off frequency is close to 8dB.

2. Design a fourth-order Butterworth low-pass filter with a cutoff frequency of 500 Hz and a passband gain of 10. Use as many 1 kÆ resistors as possible. Compare the Bode magnitude plot for this Butterworth filter. verify your design by simulation. Build a PCB for your design. Show both the schematic and layout and the 3d model of your PCB. (5 points)

Calculations:

Post Lab 2:

Butterworth denominator 4th: $(1+0.765s+s^2)(1+1.848s+s^2)$

A_{max} (pass band gain) = 10

$H(s)$ (unity gain) $= \dfrac{\frac{1}{C_1C_2}}{s^2+\frac{2}{C_1}s+\frac{1}{C_1C_2}}$ at $\omega_o = \dfrac{1}{R\sqrt{C_1C_2}} = 1$ and $R = 1\,\Omega$

if $s^2+\frac{2}{C_1}s+\frac{1}{C_1C_2} = 1+0.765s+s^2$

then $\frac{2}{C_1} = 0.765$ and $\frac{1}{C_1C_2} = 1$ } first stage

$C_1 = 2.6144\,F$ $C_2 = \frac{1}{C_1} = 0.3825$

$\frac{2}{C_3} = 1.848$ and $\frac{1}{C_3C_4} = 1$ } second stage

$C_3 = 1.0822\,F$ $C_4 = \frac{1}{C_1} = 0.924\,F$

$\omega_o = 2\pi f_c = 3141.5926$ Hz and $R = 1k$

Thus $K_m = 1000$ and $K_f = 3141.5926$

$C = \frac{C_{old}}{K_m K_f} \Rightarrow C_1 = 832nF,\ C_2 = 122nF,\ C_3 = 344nF,\ C_4 = 294nF$

$A_{max} = 10 = 1+\frac{R_F}{R_1}$ Let $R_1 = 500\Omega \Rightarrow 9\times500 = R_F = 4500\Omega$

PCB Design:

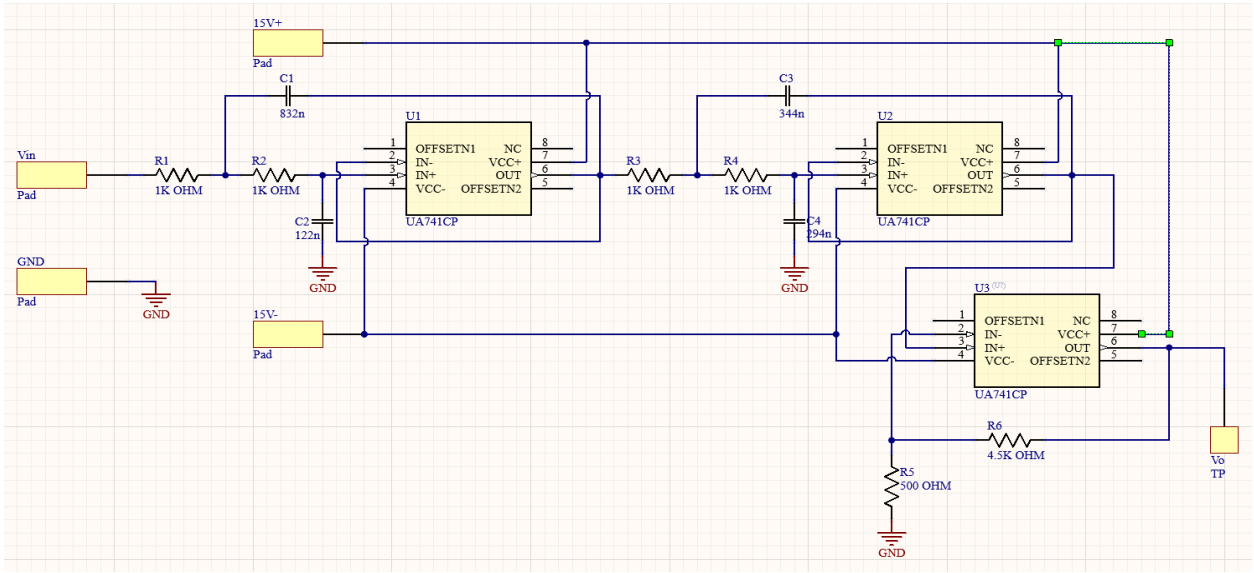


Figure 19: PCB Schematic of Post-Lab 2

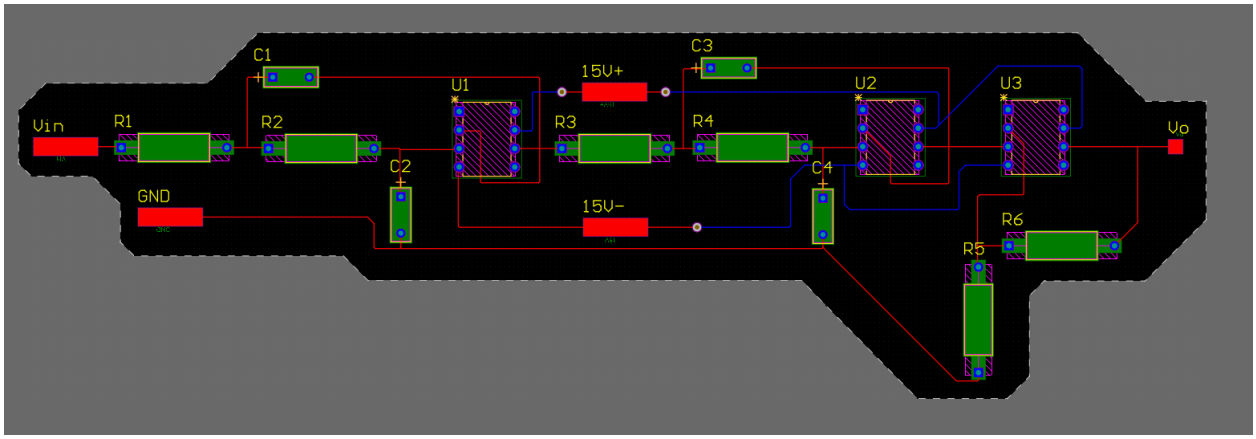


Figure 20: PCB Design of Post-Lab 2

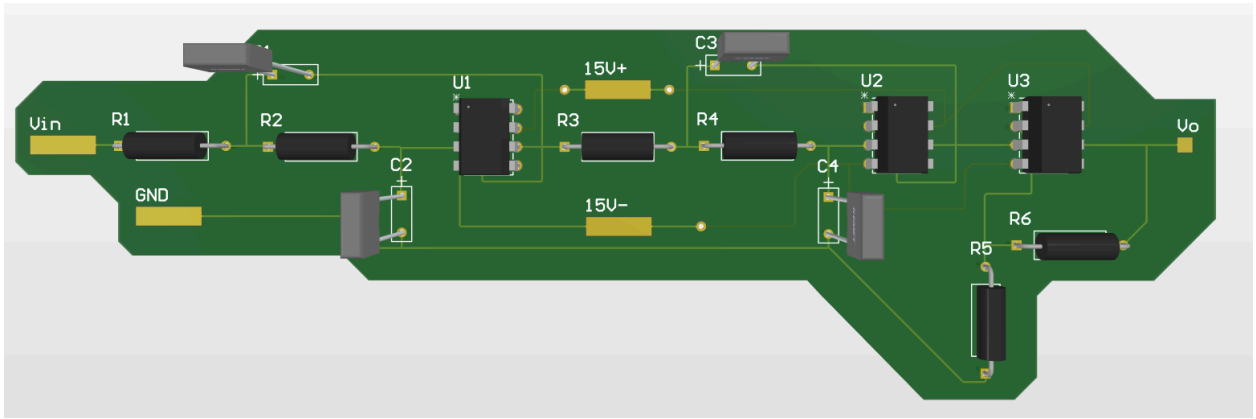


Figure 21: PCB Design in 3D for Post-Lab 2

Simulation:

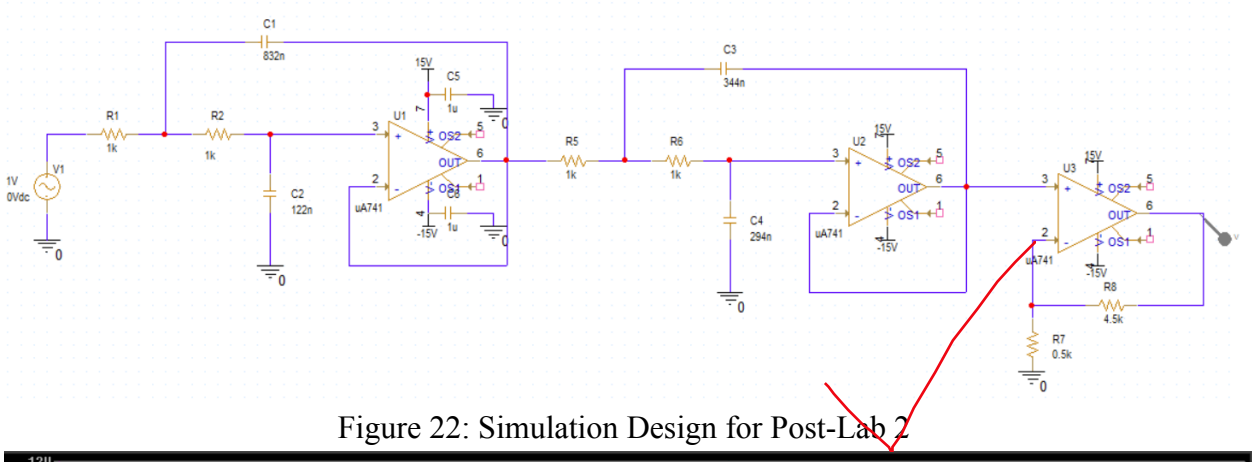


Figure 22: Simulation Design for Post-Lab 2

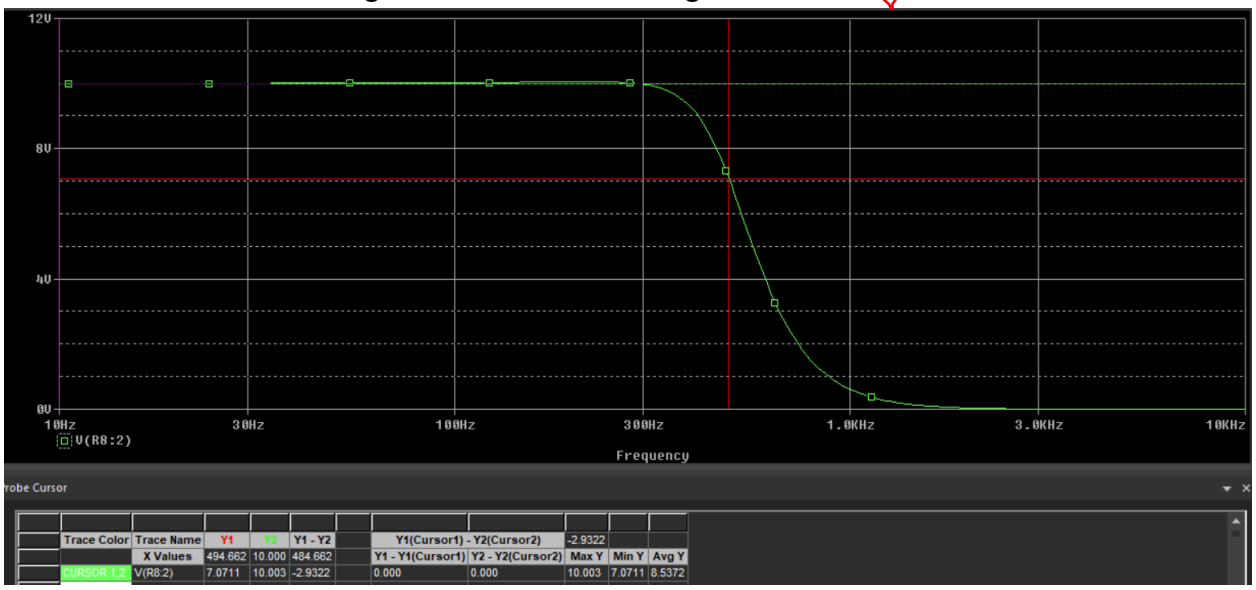


Figure 23: Simulation Results Showing Cut Off Frequency in Linear Scale

Comparison: The Butterworth design produces a voltage that is 0.707 times the maximum voltage at the cut-off frequency. In the non-Butterworth design, the cut-off frequency is placed at half the max voltage in linear scale thus hard to find.

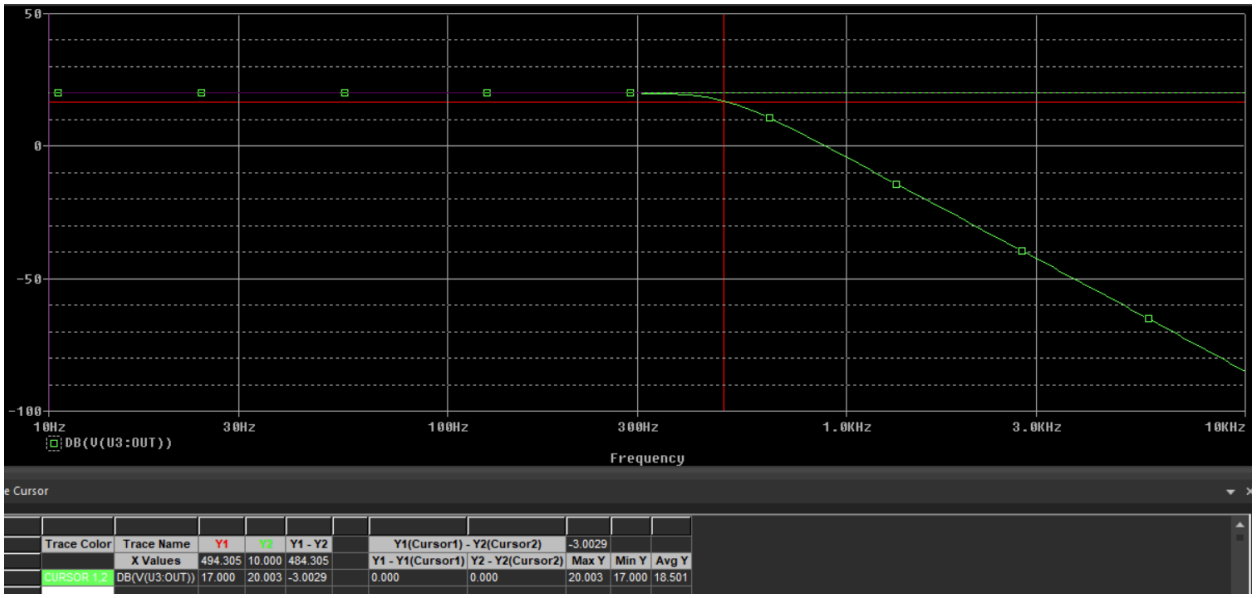


Figure 24: Simulation Results showing -3dB cut-off frequency

Comparison: The Butterworth design produces the cut-off frequency at the 17dB point (20dB-3dB). In the non-Butterworth design, the cut-off frequency is at 8dB point (20dB-(3dB*4)) due to the gain and quality factor affecting the cut-off frequency voltage.

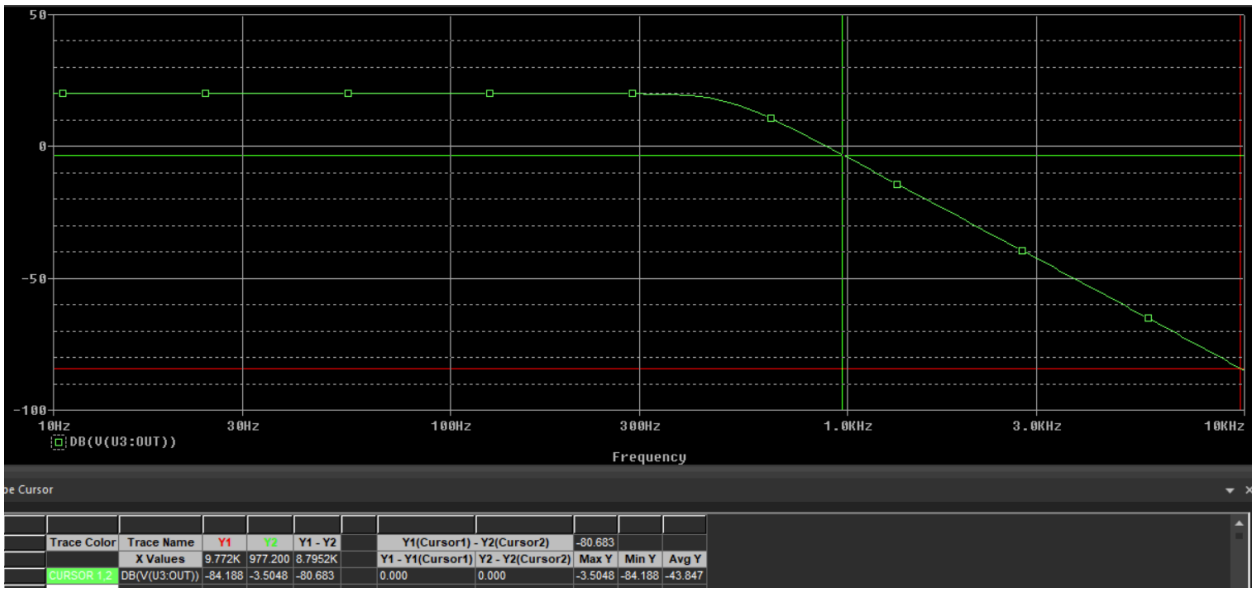


Figure 25: Simulation Results Showing -80dB/decade Roll Off in dB scale