Kaushik Nikhil Shroff

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EDUCATION:

University of Wisconsin-Madison, Madison, Wisconsin **Sep 2024 – Dec 2025**
Master of Science, Electrical and Computer Engineering GPA: 3.2/4.0
Coursework: Advanced Computer Architecture, VLSI Systems Design, Testing and Testable Design of Digital Systems

Savitribai Phule Pune University, Pune, India **Jul 2020 – Jun 2024**
Bachelor of Engineering, Electronics and Telecommunication GPA: 3.8/4.0
Courses: Digital Circuits, Microcontrollers, VLSI

SKILLS:

Languages:	Verilog, VHDL, C++, Embedded C, C
Tools:	Xilinx Vivado, gem5, Ki CAD, Multisim, Proteus
Hardware:	FPGA Programming, PCB Design & Fabrication, Microcontroller Interfacing,Computer Assembling
Soft Skills:	Research, Manuscript writing, Leadership, Event Management, Content Writing, Oration

WORK EXPERIENCE:

Embedded Intern, *JyoSH AI Solutions* **Dec 2022 – May 2023**
Tools: Raspberry Pi, Python, C++

- **Designed** and **developed** an automated door-locking system with face recognition on Raspberry Pi, which improved security and **reduced** access time by **30%**.
- **Integrated** facial recognition algorithms using OpenCV, achieving **80%** accuracy in identifying authorized individuals and preventing unauthorized access.
- Facilitated **integration** with other security systems, including **uninterruptible power supplies** and **alarm systems**, for comprehensive security solutions.
- Conducted **installation** and **testing** in designated areas, achieving a system **reliability rate** of **98%** after extensive verification.

ACADEMIC PROJECTS:

Out Of Order CPU Power Modelling in gem5, *University of Wisconsin-Madison*
Tools: gem5, McPAT, Python, C++

- Developed a power model for the **Out Of Order processor** in gem5.
- Identified components like reorder buffers and branch predictors to measure **dynamic power.**
- Used **McPA**T to estimate energy consumption for critical CPU components.
- **Added** stat reporting and integrated **power metrics** through gem5's Python front end.
- **Benchmarked** CPU operations by running C++ workloads to **evaluate efficiency**.
- **Contributed** to gem5 by adding **new stats** used in the project.

5-Level Cascaded H-Bridge Multilevel Inverter, *Savitribai Phule Pune University*
Tools: Ki Cad, Microcontroller Interfacing, PCB Design and Fabrication, Embedded C

- **Designed** and **implemented** a 5-level CHB multilevel inverter as an educational test kit.
- Enabled students to **visualize waveform variations** and understand **inverter performance** under different load conditions.
- Achieved a **THD** ranging from **22.813% to 26.372%** while performing **harmonic analysis**.
- Facilitated **collaboration** between industry and academia, for **2-layer PCB** printing methods.
- **2nd Runner Up** in Open Hardware category at Impetus and Concepts 2024 competition.

PUBLICATIONS:

- **Shroff, Kaushik**. (2023). Affordable Vehicle Tracking System. PICT's International Journal of Engineering and Technology (PIJET), 1(1).
- Nagar, R., **Shroff, K.**, Jagtap, A., Patil, N.B., Patil, L.P. (2024). A Survey on Conventional Multilevel Inverter Topologies. In: Senjyu, T., So–In, C., Joshi, A. (eds) Smart Trends in Computing and Communications. SmartCom 2024 2024. Lecture Notes in Networks and Systems, vol 947. Springer, Singapore.
- **K. Shroff**, R. Nagar, A. Jagtap, N. B. Patil and L. P. Patil, "Implementation Of 5-Level Cascaded H-Bridge Multilevel Inverter," 2024 4th Asian Conference on Innovation in Technology (ASIANCON), Pimpri Chinchwad, India, 2024, pp. 1-7, doi: 10.1109/ASIANCON62057.2024.10837940.