

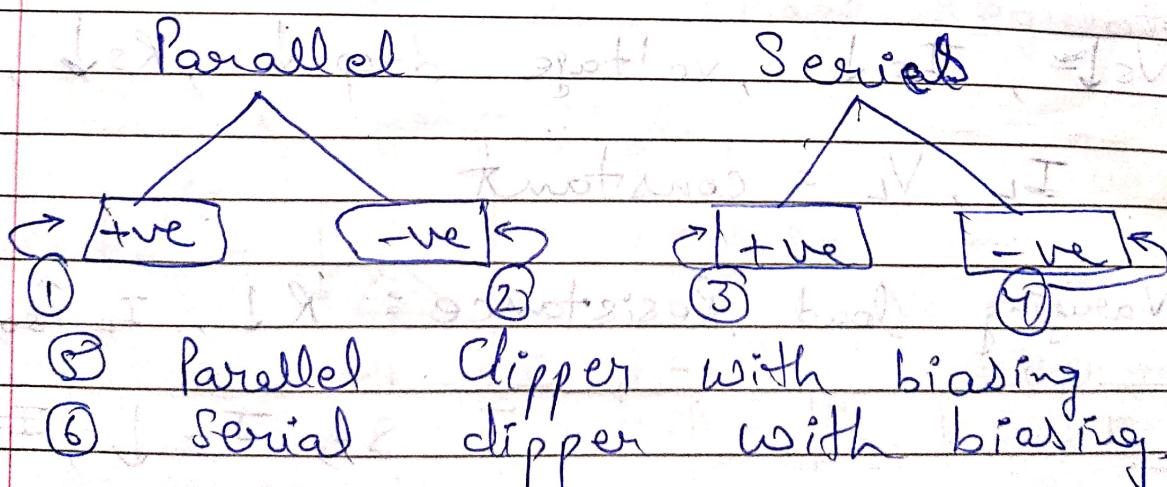
$I_L \uparrow, I_L \downarrow, I_2 \uparrow$

$I_S R_S = \text{constant}, V_i = \text{constant}$

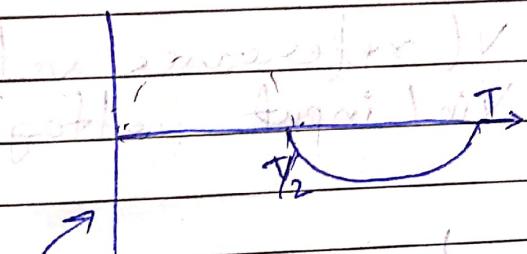
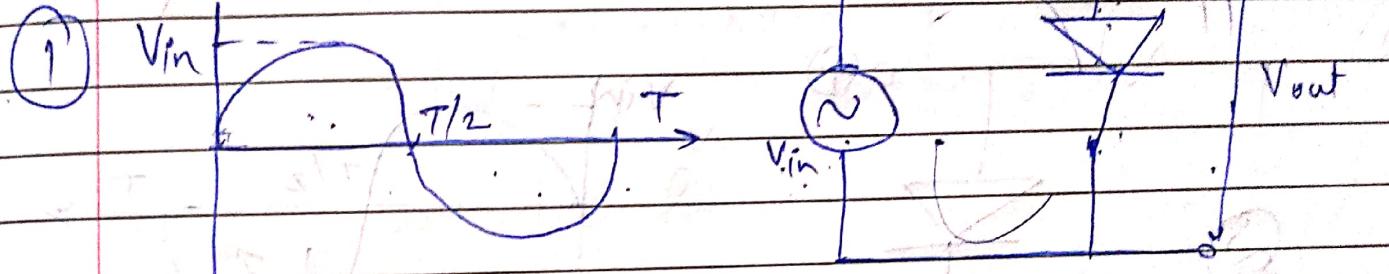
18 August, 2025

Clipper : Clipper circuit prevents output wave form from exceeding certain limit, at the same time, does not disturb the remaining wave form. It is used in over voltage protection circuit to prevent from high voltage spikes.

Two types :-

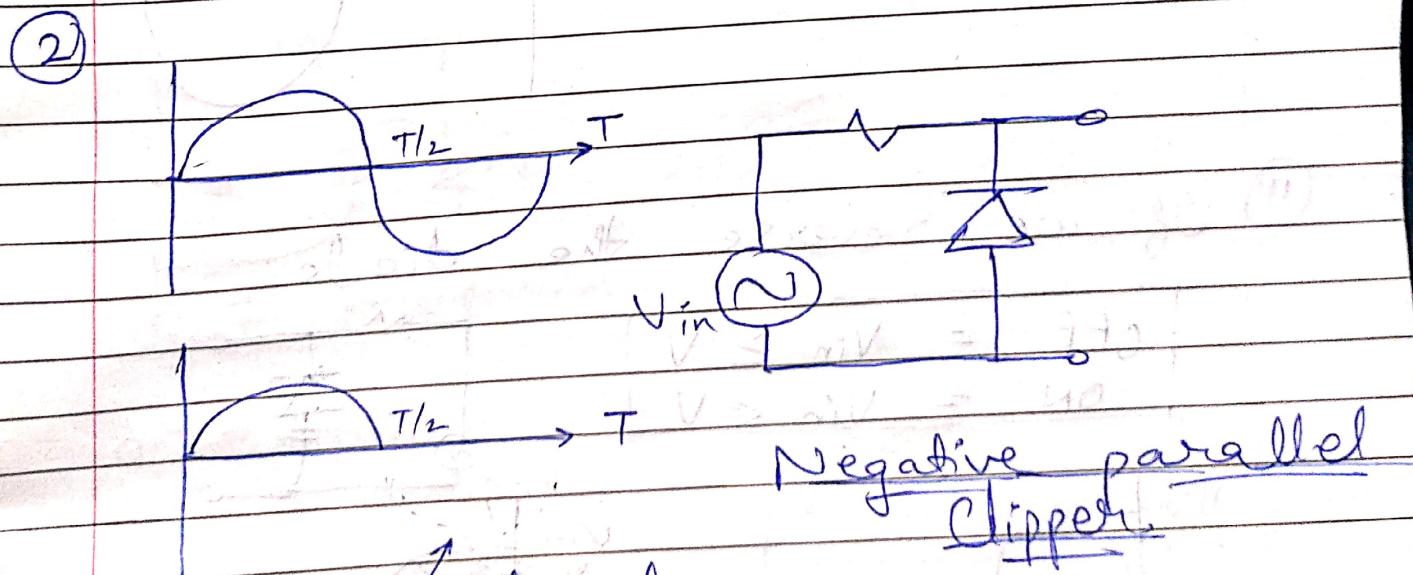


Date: 1/1

Parallel

Positive parallel  
clipped

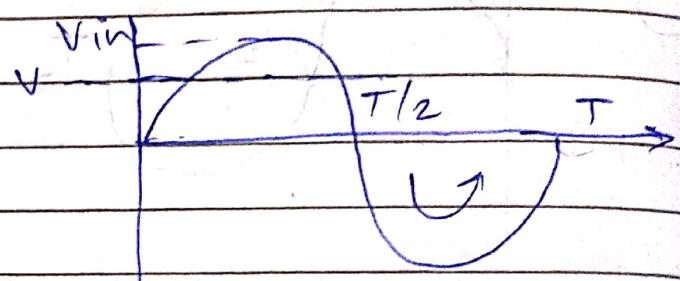
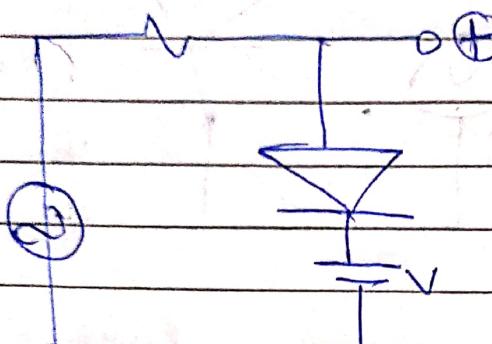
positive part gets clipped



negative part gets  
clipped

Negative parallel  
clipped

Date : 1/1/1

Parallel Clipper with Biasing

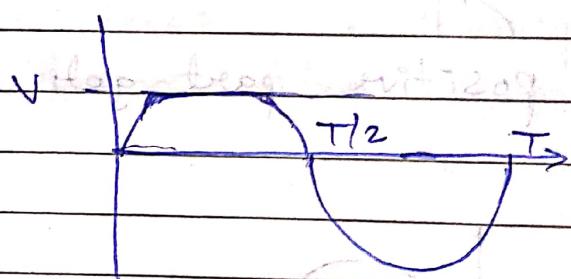
fwd Bias

$$\text{(closed)} \quad \text{ON} = V_{in} \geq V$$

fwd Bias

$$\text{(open circuit)} \quad \text{OFF} = V_{in} < V$$

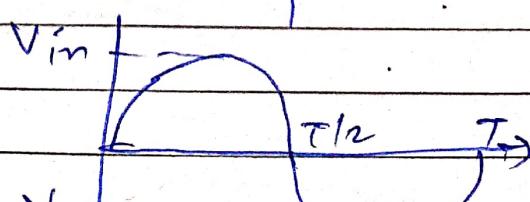
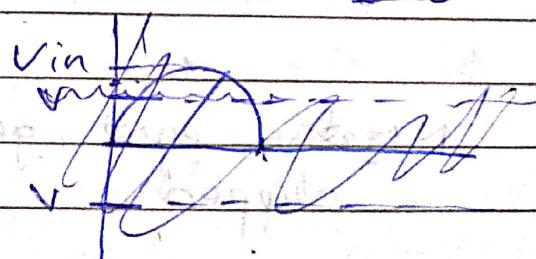
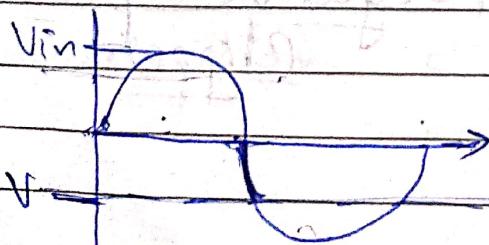
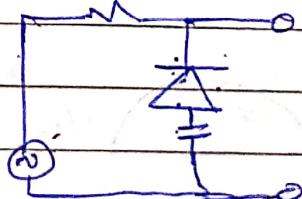
$V$  (reference voltage)  
 $V_{in}$  (input voltage)



⑪ If we reverse the diode

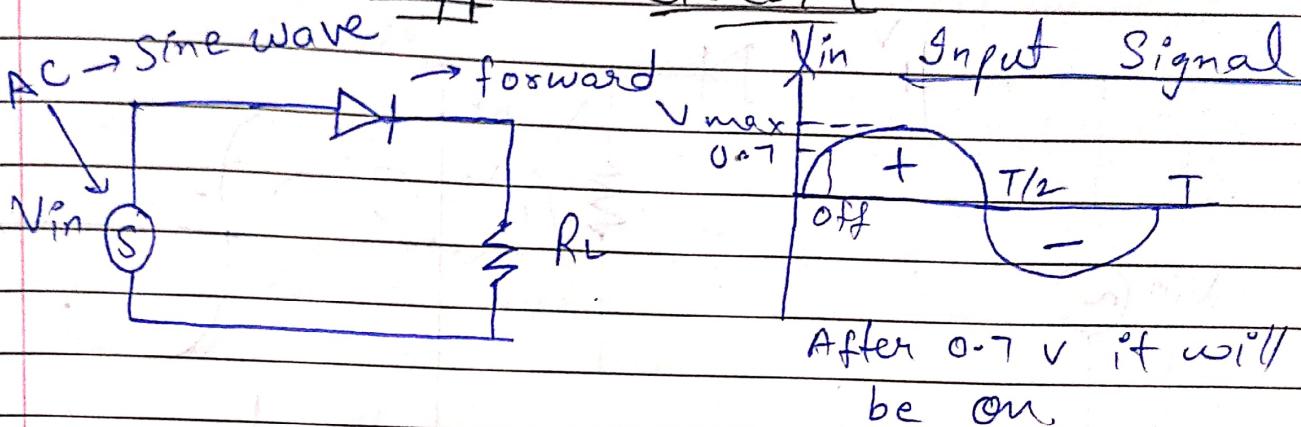
$$\text{OFF} = V_{in} \geq V$$

$$\text{ON} = V_{in} < V$$



Date: 21/8/25

## Series Clipper Circuit



series +ve clipper



Input signal

$0.7 \Rightarrow$  threshold

voltage

$V_{max}$

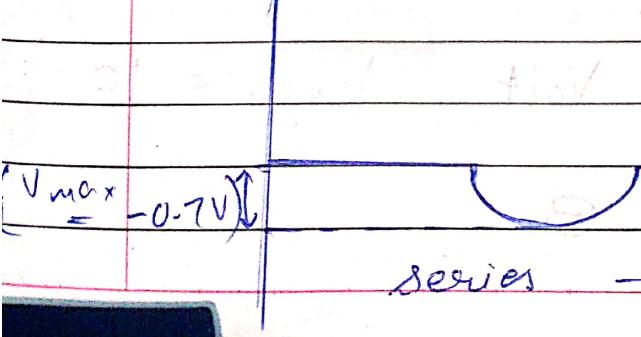
$0.7\text{V}$

+

$T/2$

$T$

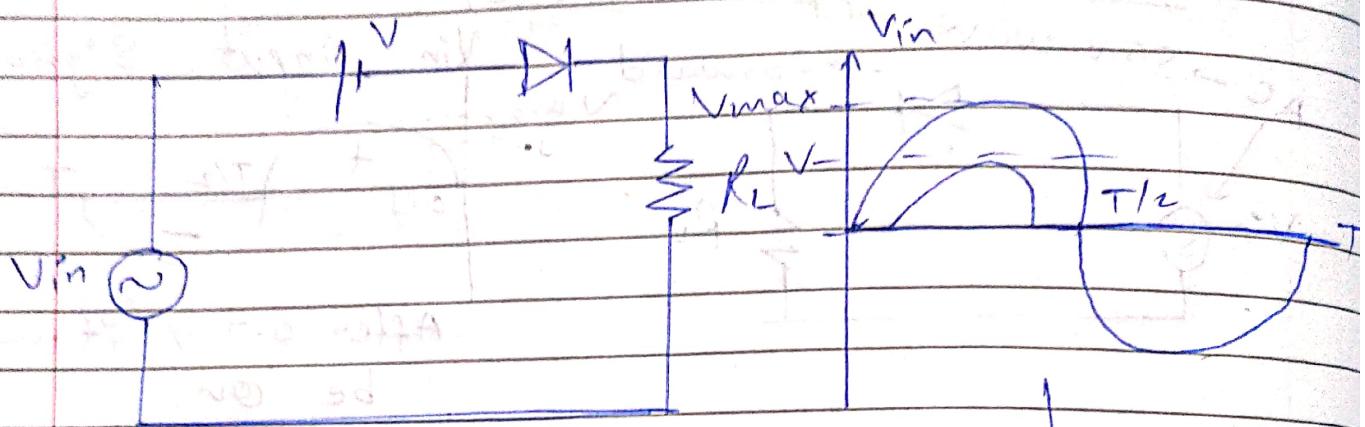
series -ve clipper



series -ve clipper

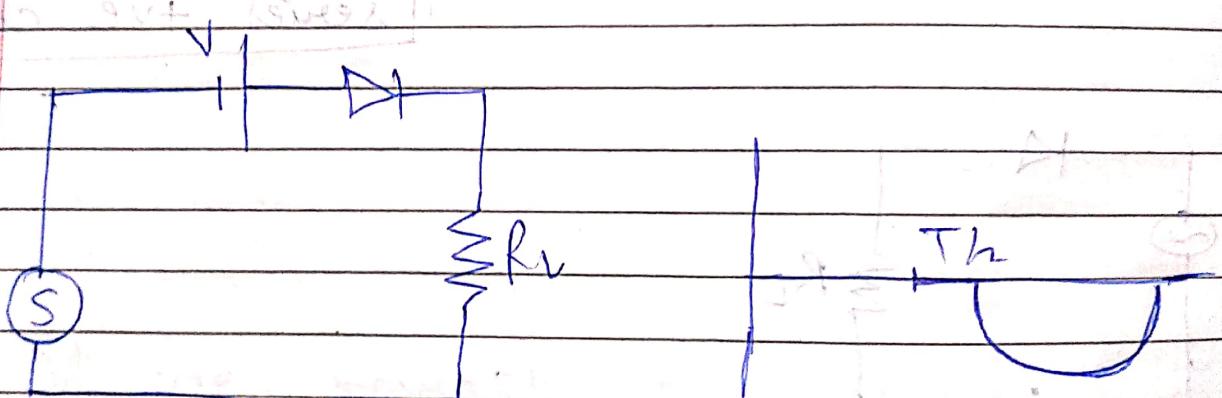
Date : 1/1/2023

# Series Clipper Circuit With Biasing :-

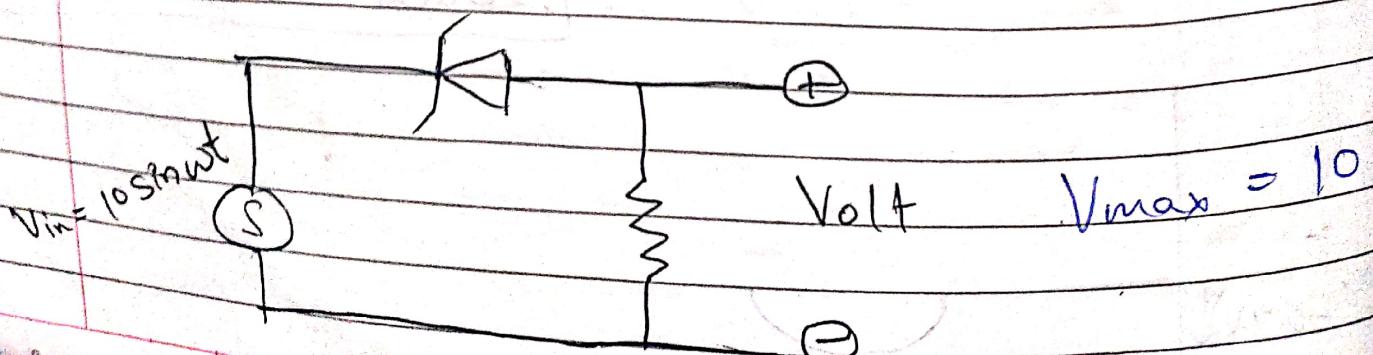


$$V_{in} - V > 0$$

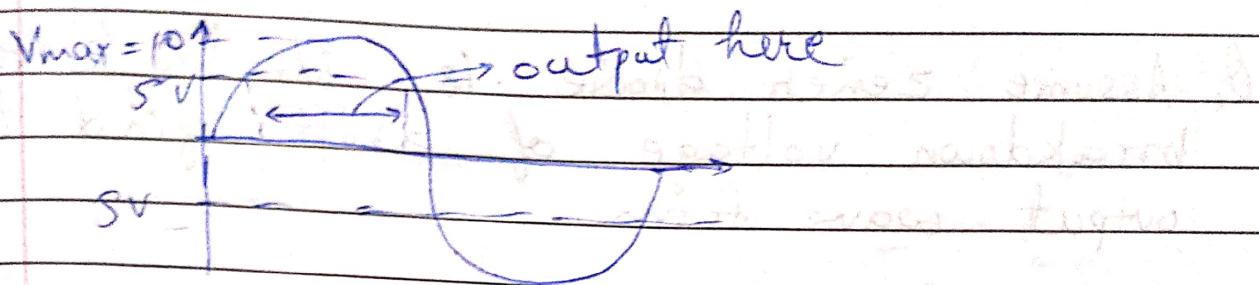
$$V_{in} > V$$



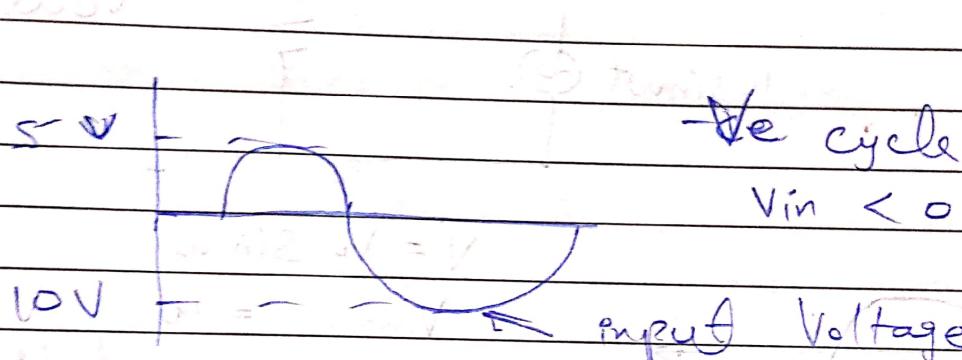
- Q1 Assume Zener diode is ideal breakdown voltage of 5v . find the output wave form.



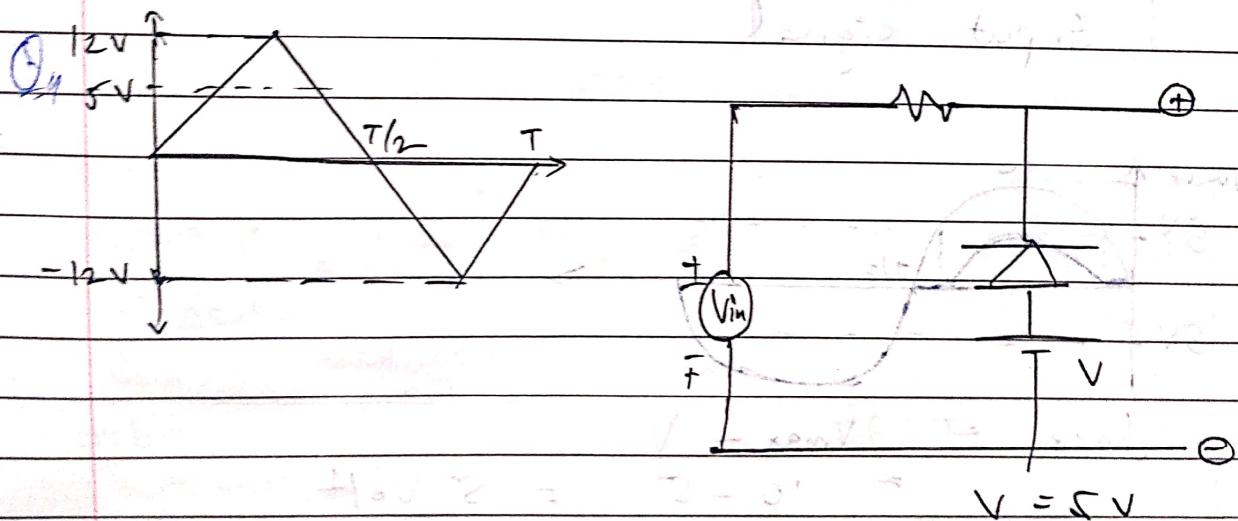
Date: 1/1



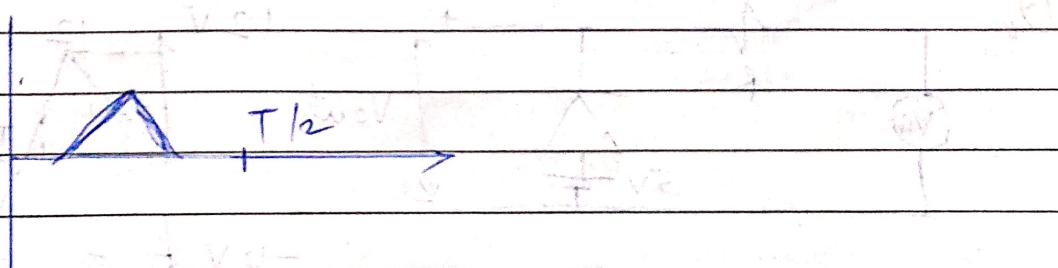
Output wave form:-



input Voltage = output V



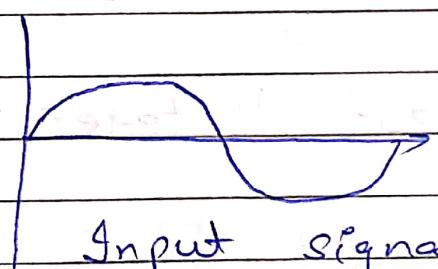
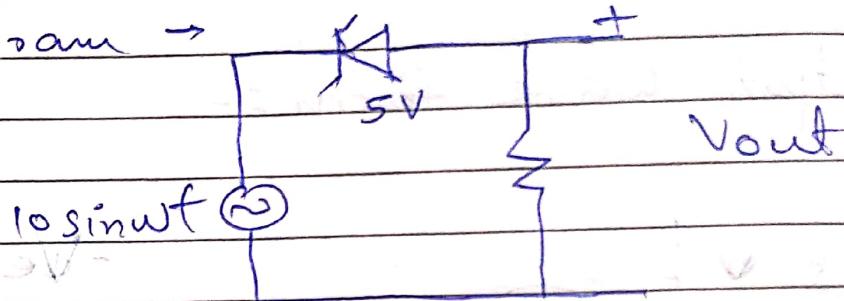
$$V = 5V$$



Date : / /

Q. Assume zener diode is ideal with breakdown voltage of 5 Volt, find the output wave form

given diagram →

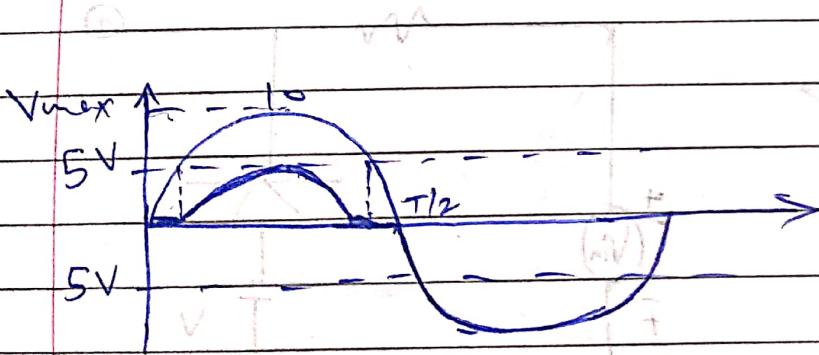


$$V = V_0 \sin \omega t$$

$$V_{max} = 10$$

5 volt = half

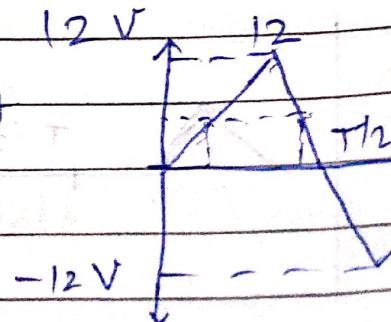
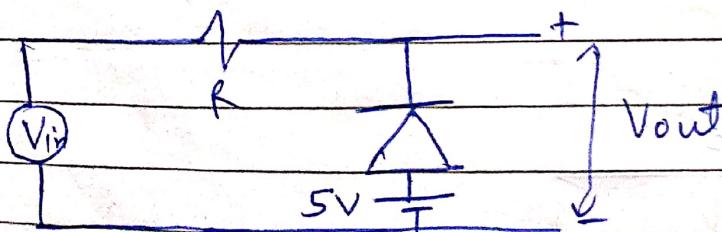
Input signal

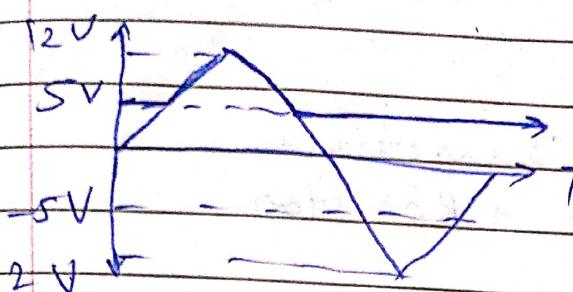


$$\text{loss} = V_{max} - V$$

$$= 10 - 5 = 5 \text{ volt}$$

Q.



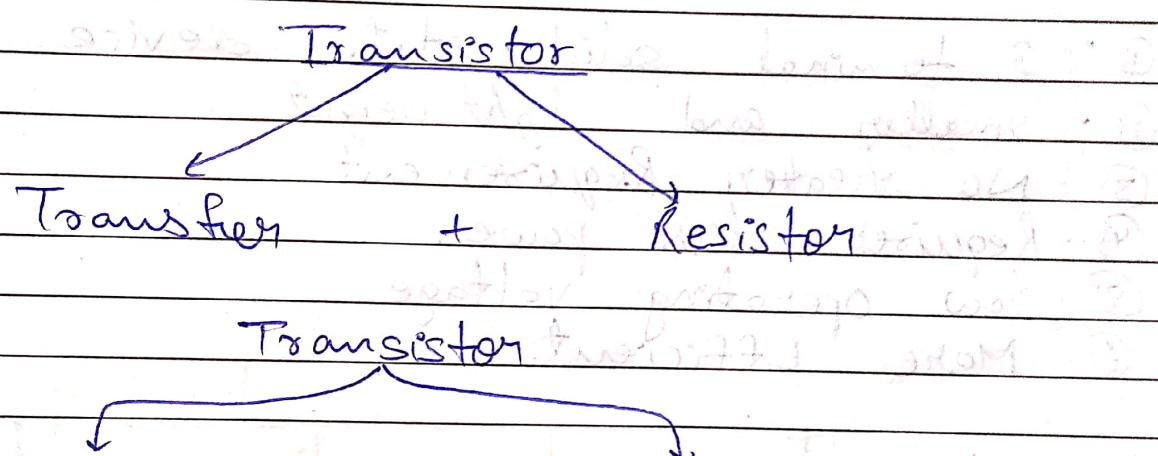


$V_{in} < 5V$ , forward bias

$V_{in} > 5V$ , reverse bias

### Module - 3

#### Bipolar Junction Transistor



BJT (Bipolar Junction)      FET (Field Effect)

n-p-n

p-n-p

JFET

MOSFET

n-channel  
p-channel

I  
n-channel      p-channel

enhancement mode

depletion mode

n-channel      p-channel

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Bipolar:  $e^-$  &  $h^+$ 

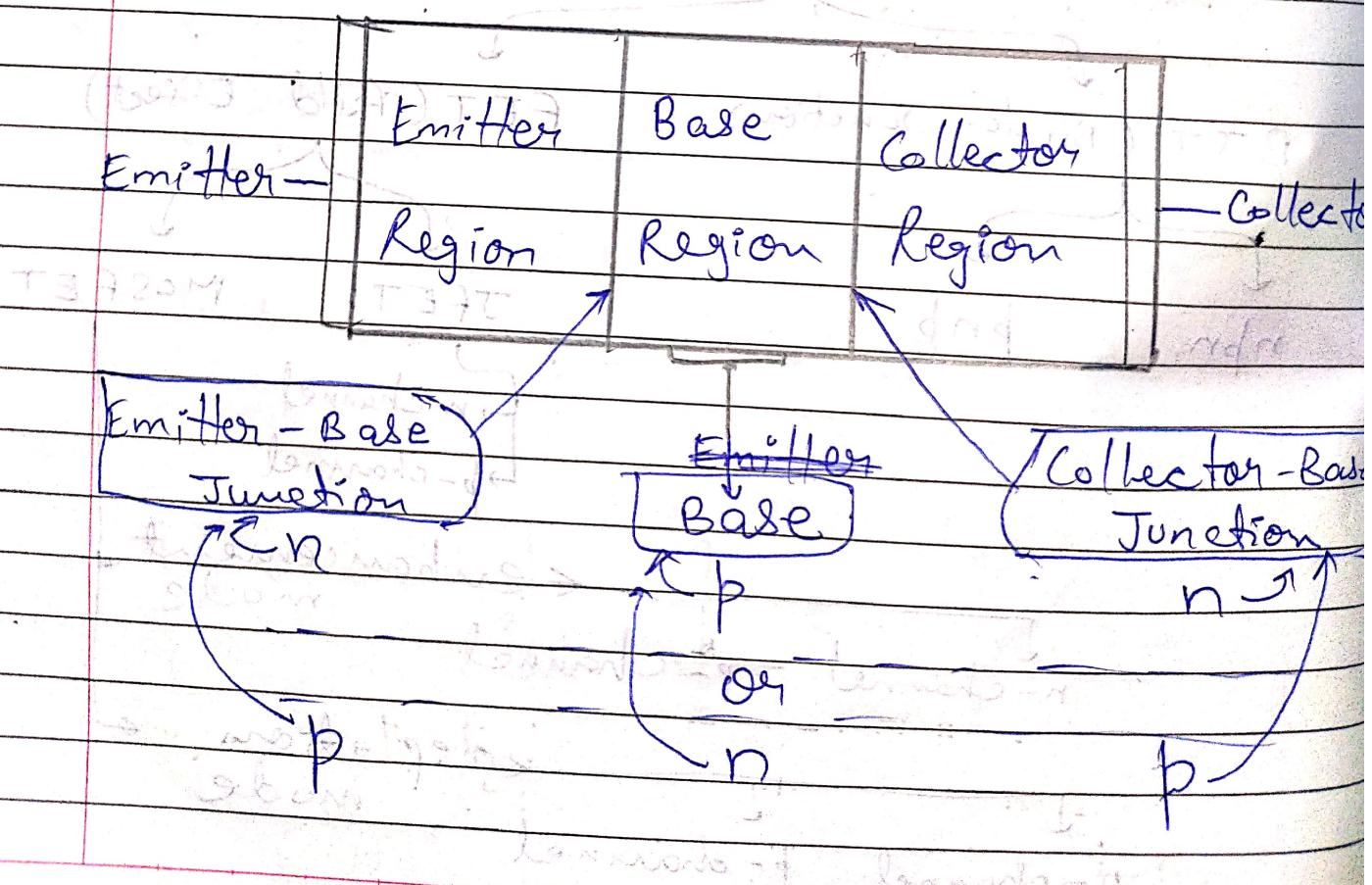
Junction: 2 p &amp; n Junction

Transistor: Transfer + Resistor

- It is a 3 terminal device
- Amplify and magnify signal

### Important features of BJT →

- ① 3 terminal solid state device
- ② smaller and light weight
- ③ No heater requirement
- ④ Requires less power.
- ⑤ low operating voltage
- ⑥ More Efficient.



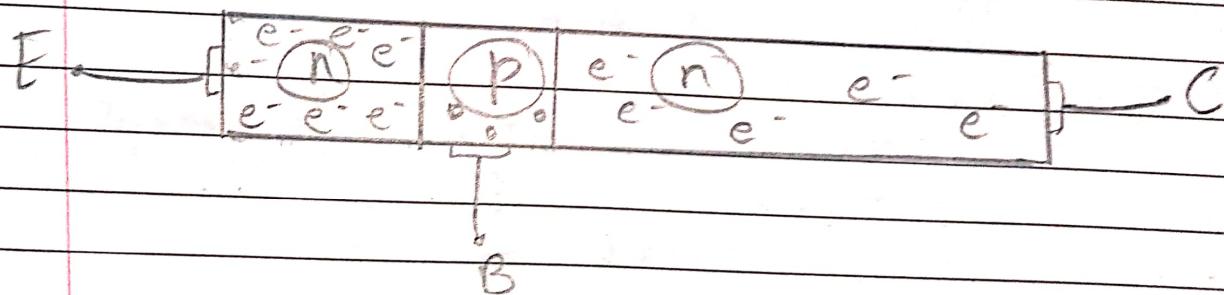
Symbols :-

$npn \rightarrow B - \begin{cases} C \\ E \end{cases}$  (arrow Emitter k-  
taraf)

$pnp \rightarrow B - \begin{cases} E \\ C \end{cases}$  (arrow base k-  
taraf)

Construction :-

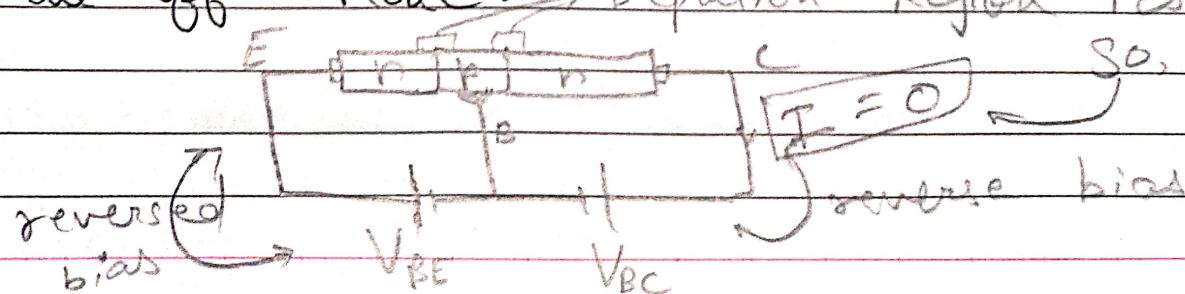
	F	B	C
<u>width</u>	Med.	Thin	High
Doping lvl	High	Low	Moderate



\* Working principle :-

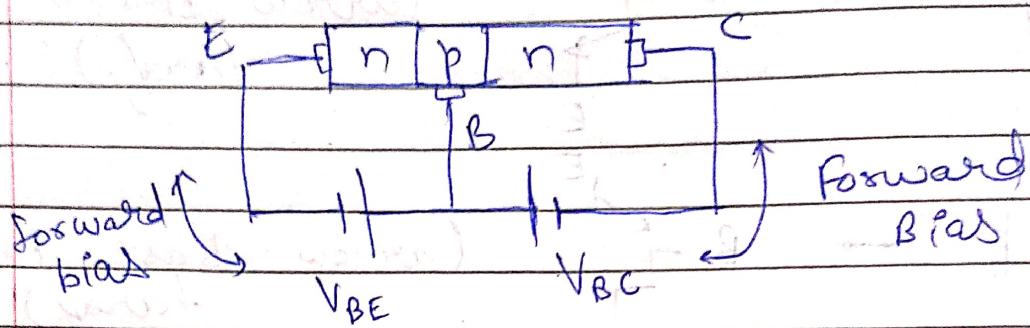
- 1> Cut off mode
- 2> Saturation mode
- 3> Active mode

① Cut off Mode :- Depletion Region Yes.



Date : / /

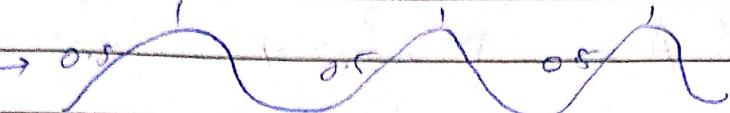
## (2) Saturation :-

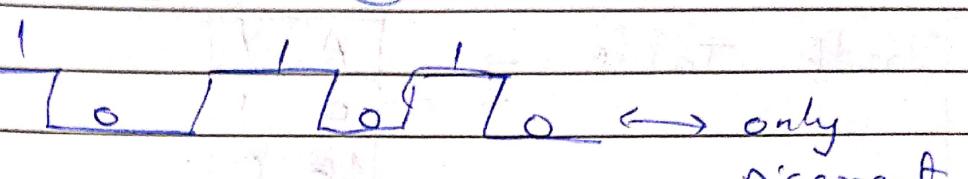


∴ Depletion region = smallest  
So,  $I = I_{max}$

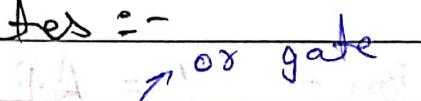
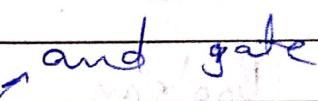
## (3) Active :-

# Digital Electronics :-

Analog  $\rightarrow$  

Digital  $\rightarrow$  

Boolean algebra and logic gates :-

 OR gate       AND gate

Identity :  $A + 0 = A$ ,  $A \cdot 1 = A$

Null :  $A + 1 = 1$ ,  $A \cdot 0 = 0$

Inverse :  $A + \bar{A} = 1$ ,  $A \cdot \bar{A} = 0$   $\rightarrow$  not gate

Idempotent :  $A + A = A$ ,  $A \cdot A = A$

Types of laws :-

- (i) Associative
- (ii) Commutative
- (iii) Distributive

DeMorgan's theorem :-

$$\text{i)} A \cdot B = \bar{A} + \bar{B}$$

$$\text{ii)} \overline{A+B} = \bar{A} \cdot \bar{B}$$

Gates Categorised :-

1) Basic gate  $\rightarrow$  AND, OR, NOT

2) Universal gate  $\rightarrow$  NAND, NOR

3) Exclusive gate  $\rightarrow$  EX-OR, EX-NOR

**NOT GATE →**Boolean expression  $\rightarrow Y = \bar{A}$ Symbol  $\rightarrow A \rightarrow Y$ Truth Table  $\rightarrow$ 

A	Y
0	1
1	0

**(And) Gate →**Boolean expression  $\rightarrow Y = A \cdot B$ Symbol  $\rightarrow A \rightarrow B \rightarrow Y$ Truth Table  $\rightarrow$ 

A	B	Y
0	0	0
1	0	0
0	1	0
1	1	1

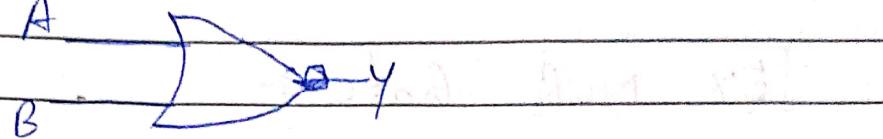
**OR Gate →**Boolean expression  $\rightarrow Y = A + B$ Symbol  $\rightarrow A \rightarrow B \rightarrow Y$ Truth Table  $\rightarrow$ 

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

R NOR gate :-

Boolean expression  $\Rightarrow Y = \overline{A+B}$

Symbol  $\rightarrow A$



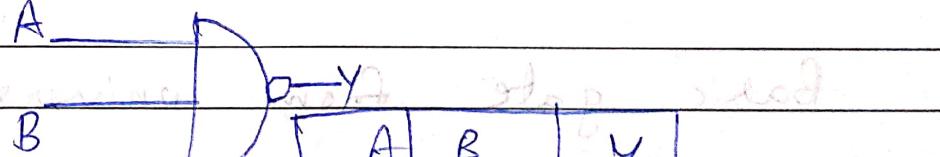
Truth Table  $\rightarrow$

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

NAND Gate  $\rightarrow$ 

Boolean expression  $\rightarrow Y = \overline{A \cdot B}$

Symbol  $\rightarrow A$



Truth Table  $\rightarrow$

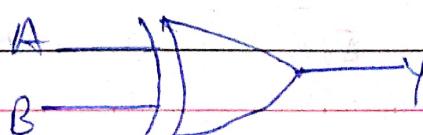
A	B	Y
0	0	1
1	0	1
0	1	1
1	1	0

EX-OR Gate :-

Boolean expression  $Y = (\overline{A \cdot B}) + (A \cdot \overline{B})$

$$Y = A \oplus B$$

Symbol  $\rightarrow A$



Date: 1/1/2023

Truth Table →

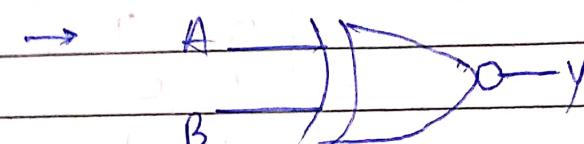
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

EX-NOR Gate :-

Boolean expression =  $Y = (\bar{A} \cdot \bar{B}) + (A \cdot B)$

$$Y = A \odot B = \overline{A \oplus B}$$

Symbol →



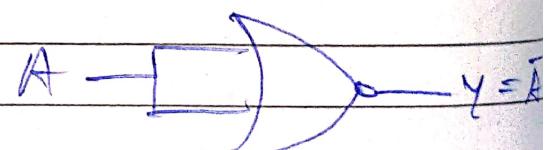
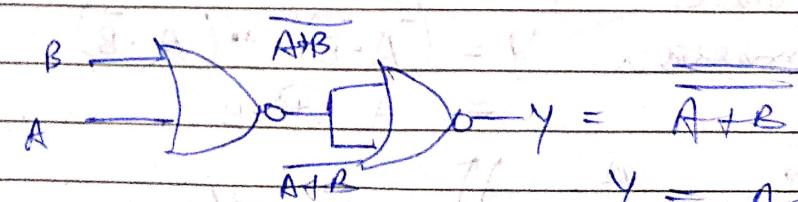
Truth Table →

A	B	Y
0	0	1
1	0	0
0	1	0
1	1	1

Basic gate from universal gate:-

NOR

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

OB

$$Y = A + B \text{ (OR gate)}$$

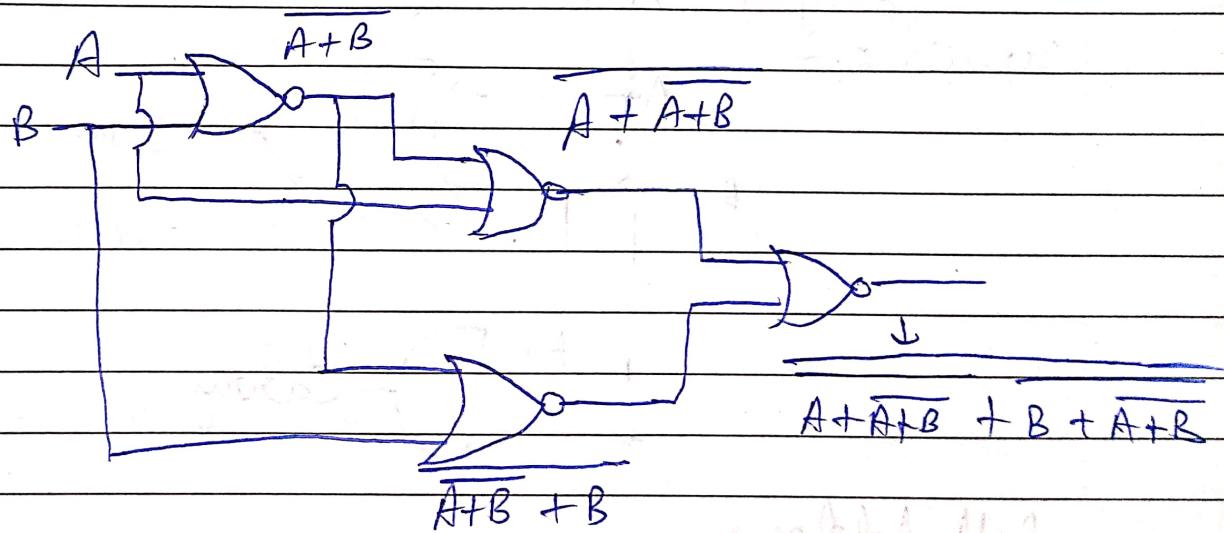
Date: 19/9/25

EX-NOR using NOR :-

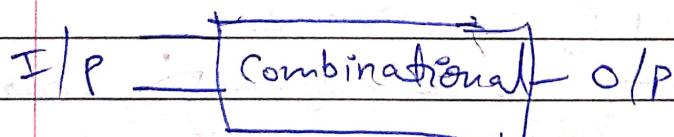
$$\begin{aligned}\text{EX-NOR} &\rightarrow \overline{\overline{AB}} + A\cdot B \\&= \overline{A \oplus B} \\&= \overline{AB} + A\overline{B} \\&= \overline{AB} + A\overline{A} + A\overline{B} + B\overline{B} \\&= \overline{A}(\overline{A+B}) + \overline{B}(\overline{A+B})\end{aligned}$$

Apply de morgan's law :-

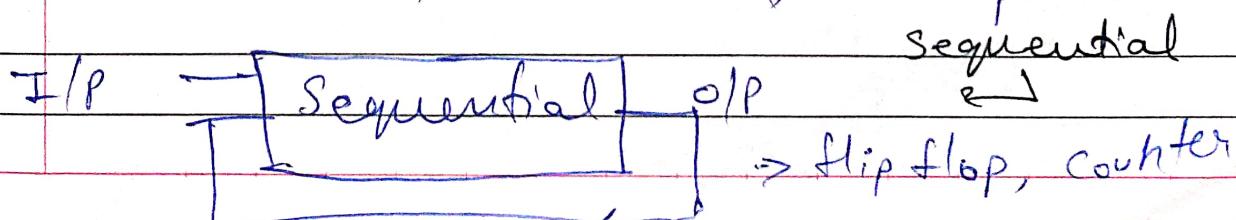
$$= A + \overline{A+B} + B + \overline{A+B}$$



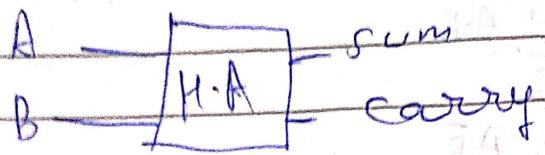
\* combinational :-



= adder, subtractor, multiplier



Date: / /

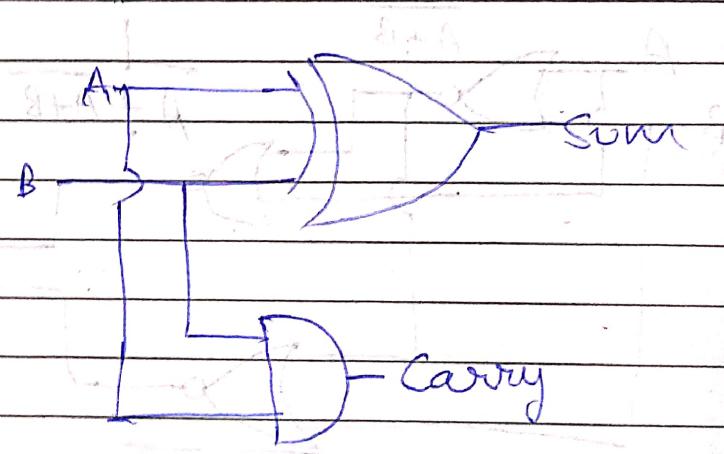
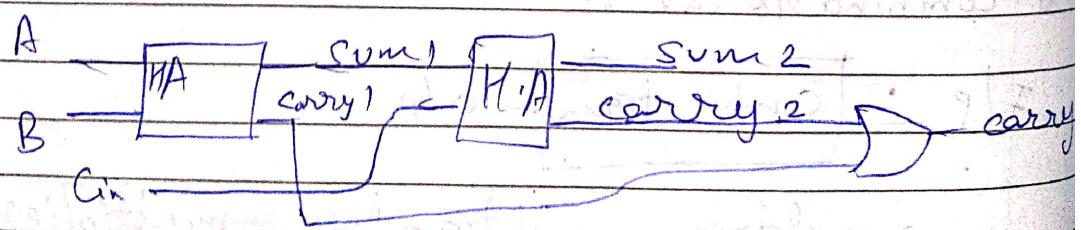
Half Adder :-

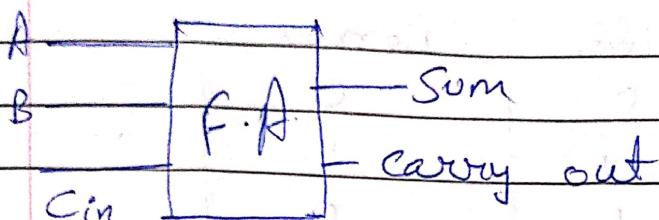
A	B	Sum	Carry
0	0	0	0
1	0	1	0
0	1	1	0
1	1	0	1

$$\text{Sum} = A \oplus B + C_1 \cdot B + C_1 \cdot A$$

$$\text{Carry} = A \cdot B$$

Circuit :-

full Adder:-

Full Adder :-

A	B	Cin	Sum	Carry out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	0	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Equation for Sum :-

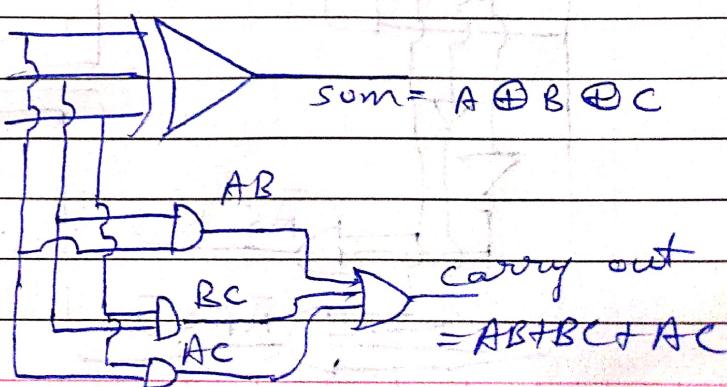
$$\text{Sum} = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$

$$= A \oplus B \oplus C$$

$$\text{carry out} = \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$$

$$= AB + BC + CA$$

Ckt Diagram  
from equations



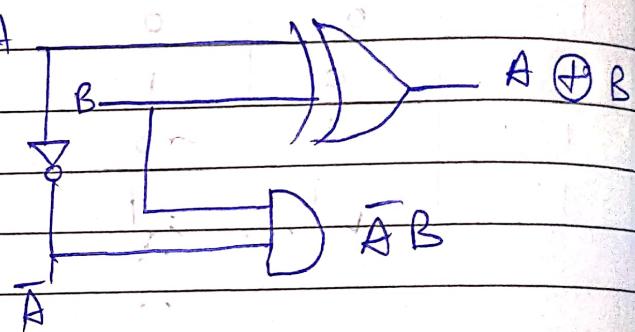
Date: \_\_\_\_\_ / \_\_\_\_\_ / \_\_\_\_\_

Half Subtractor :-

A	B	Diff.	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

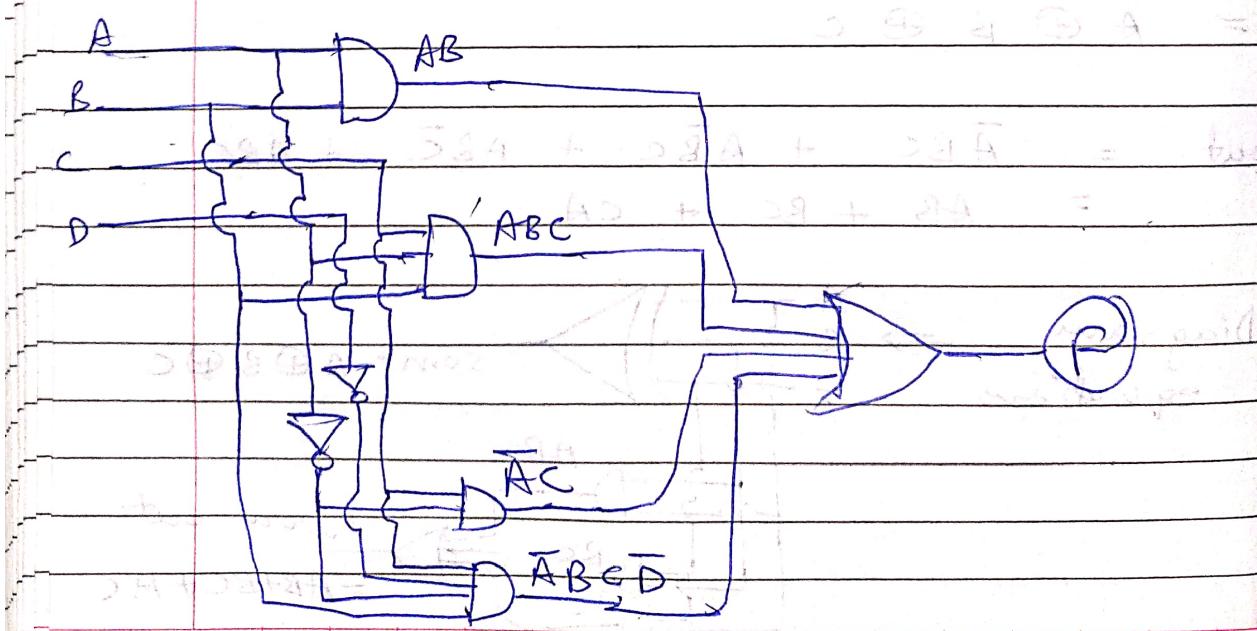
$$\text{Diff.} = \bar{A}\bar{B} + A\bar{B}$$

$$\text{Borrow} = \bar{A}B$$

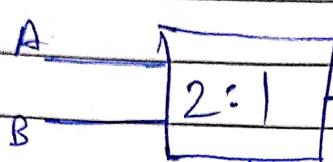
ckt diagram  $\rightarrow$ 

ckt making practice :-

$$F = AB + \bar{A}C + ABC + \bar{A}BCD + \bar{A}CD$$

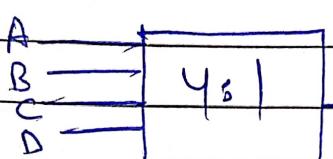


Multiplexer  $\rightarrow$  (MUX)



$S \leftarrow (\text{select})$

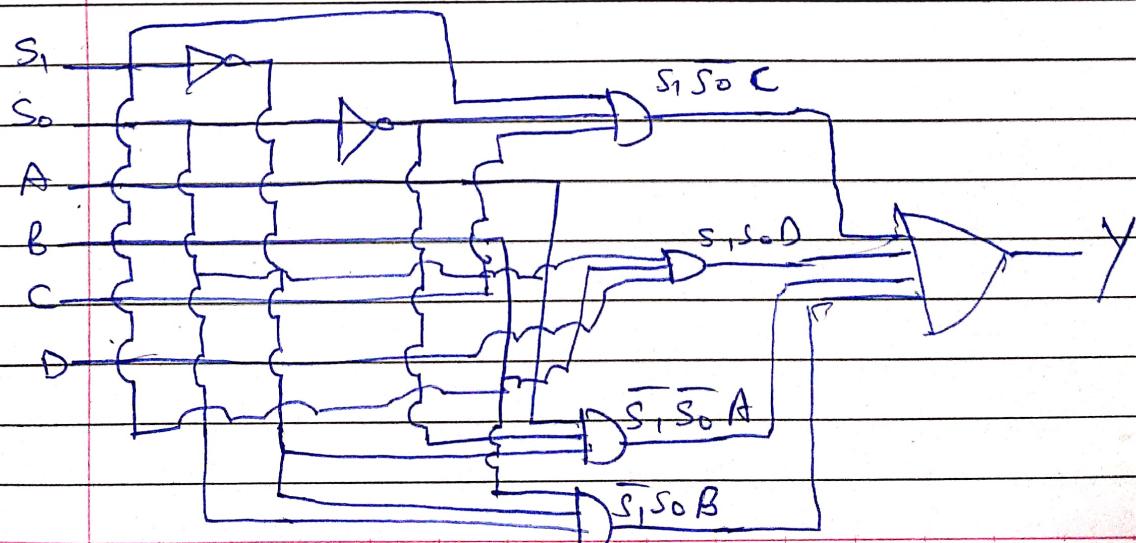
$$2:1 \Rightarrow 2^1$$



$$4:1 \Rightarrow 2^2$$

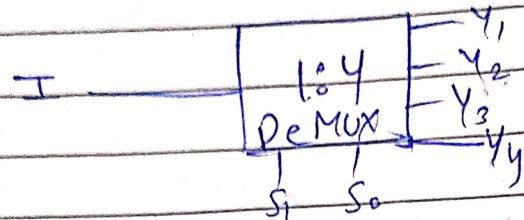
$S_1$	$S_0$	$Y$
0	0	A
0	1	B
1	0	C
1	1	D

$$Y = \bar{S}_1 \bar{S}_0 A + \bar{S}_1 S_0 B + S_1 \bar{S}_0 C + S_1 S_0 D$$



Date : 1/1

## De Multiplier (De MUX) :-



$$y_1 = \overline{s_0} s_1 I$$

$$y_2 = \overline{s_1} s_0 I$$

$$y_3 = s_1 \overline{s_0} I$$

$$y_4 = s_1 s_0 I$$

