Kaustubh Pandey

J +91-9636379818

kaustubhofficial.kp@gmail.com kaustubh-pandey

KPkaustubhKP

Education

Manipal Institute of Technology

Aug 2022 - Present

B. Tech in Electronics & Communication (VLSI)

- Current CGPA: 7.84 / 10 (as of 3rd Semester)

Manipal, Karnataka

Relevant Coursework

• Digital IC Design

- VLSI Design
- Analog Circuits
- FPGA System Design
- Semiconductor Physics
- Verilog HDL
- Signals & Systems
- Embedded Systems

Experience

VLSI System Design – PCB Design Intern

Feb 2025 - Mar 2025

PCB Designer

Manipal, India

- Designed and laid out the evaluation board for the Thejas32 (by Vega Processor & CDAC) using KiCad, including schematic capture and PCB layout.
- Applied high-speed routing and impedance control for Thejas32's.
- Generated manufacturing Gerber files .

Project MANAS – Hardware Subsystem, Autonomous UGV Team

June 2023 - Present

Hardware Engineer

Manipal, India

- Designed power distribution boards (PDB) for autonomous UGVs with robust thermal handling and high-current switching.
- Implemented precise current sensing using the INA226 current-sense IC to monitor load currents.
- Developed motor and microcontroller interface boards.
- Led PCB design using KiCad and coordinated manufacturing with Lion Circuits.
- Integrated CAN-bus communication using MCP2542FD transceivers for reliable subsystem messaging.

Projects

PID Motor Controller | Verilog, Vivado, Icarus Verilog, GTKWave

May 2025

- Designed and implemented a digital PID controller in Verilog to regulate DC motor speed via encoder feedback.
- Synthesized the design with Vivado for deployment FPGA development board.
- Simulated the controller using Icarus Verilog and analyzed waveforms with GTKWave to validate functionality.

Technical Skills

Languages: Verilog, C, Python, Bash, LATEX

Tools: KiCad, Vivado, Icarus Verilog, GTKWave, Cadence, LTSpice, Arduino IDE

Technologies: PCB Design, FPGA, Embedded Systems, Analog Design, Power Electronics

Leadership / Extracurricular

Project MANAS – Autonomous UGV Team

June 2023 - Present

Manipal Institute of Technology

Hardware Engineer & R&D Contributor

- Collaborated with AI and perception teams on sensor-fusion hardware design for real-time navigation.
- Mentored junior teammates on KiCad workflow, component selection, and design-for-manufacturability.
- Secured 3rd place in the AutoNav Challenge at IGVC 2025, representing MIT with a fully autonomous UGV platform.