Kaustubh Pandey

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Education

Manipal Institute of Technology **2023 – Present**
B.Tech in Electronics & Communication (VLSI) *Manipal, Karnataka*
– Current CGPA: 7.53 / 10 (as of 5th Semester)

Relevant Coursework

- VLSI Design
- Digital IC Design
- Analog IC Design
- Physical Design
- Analog Circuits
- FPGA System Design
- Semiconductor Physics
- Verilog HDL

Experience

VLSI System Design – PCB Design Intern **Feb 2025 – Oct 2025**
PCB Designer *Manipal, India*
– Designed and laid out the evaluation board for the Thejas32 (by Vega Processor & CDAC) using KiCad, including schematic capture and PCB layout.
– Collaborated on creating a shield for their FPGA board PCB design, integrating interface components and ensuring signal integrity.
– Applied high-speed routing and impedance control for Thejas32's critical signal paths.
– Generated manufacturing Gerber files and coordinated with fabrication partners for prototype development.

Project MANAS – Hardware Subsystem, Autonomous UGV Team **June 2023 – Present**
Hardware Engineer *Manipal, India*
– Designed power distribution boards (PDB) for autonomous UGVs with robust thermal handling and high-current switching.
– Implemented precise current sensing using current-sense IC to monitor load currents.
– Developed motor and microcontroller interface boards.
– Led PCB design using KiCad and coordinated manufacturing with Lion Circuits.
– Integrated CAN-bus communication using MCP2542FD transceivers for reliable subsystem messaging.

Projects

PID Motor Controller | *Verilog, Vivado, Icarus Verilog, GTKWave* **May 2025**
– **Published in IEEE:** DOI: 11232594 - Digital PID Controller Design for DC Motor Speed Regulation on FPGA.
– Designed a digital PID controller in Verilog HDL for DC motor speed regulation using encoder feedback signals.
– Synthesized and implemented the design on FPGA using Vivado with pipelined architecture for deterministic control loops.
– Performed comprehensive simulations using Icarus Verilog and validated timing behavior with GTKWave waveform analysis.
– Achieved closed-loop stability with tuned proportional, integral, and derivative gains; validated against real-world motor dynamics.

4H-SiC Trench U-MOSFET with BPT | *Synopsys Sentaurus TCAD, Device Physics* **Oct 2025**
– Co-authored research on 4H-SiC trench U-MOSFET achieving 556 V breakdown voltage using breakdown point transfer (BPT) technique.
– Performed 2D TCAD device simulations; optimized drift region and electric field profiles for high-voltage performance.

Technical Skills

Languages: SystemVerilog, Verilog, C, Python, Bash, Latex
Tools: KiCad, Vivado, Icarus Verilog, GTKWave, Cadence, Synopsys Sentaurus TCAD, LTSpice
Technologies: PCB Design, FPGA, Power Devices, Semiconductor Physics, Physical Design

Leadership / Extracurricular

Project MANAS – Autonomous UGV Team **June 2023 – Present**

Hardware Engineer & R&D Contributor *Manipal Institute of Technology*

- Collaborated with AI and perception teams on sensor-fusion hardware design for real-time navigation.
- Mentored junior teammates on KiCad workflow, component selection, and design-for-manufacturability.
- **Secured 3rd place in the AutoNav Challenge at IGVC 2025**, representing MIT with a fully autonomous UGV platform.
- **Won PIMA at ISDC 2025** held at BITS Goa, recognizing excellence in innovation and technical implementation.