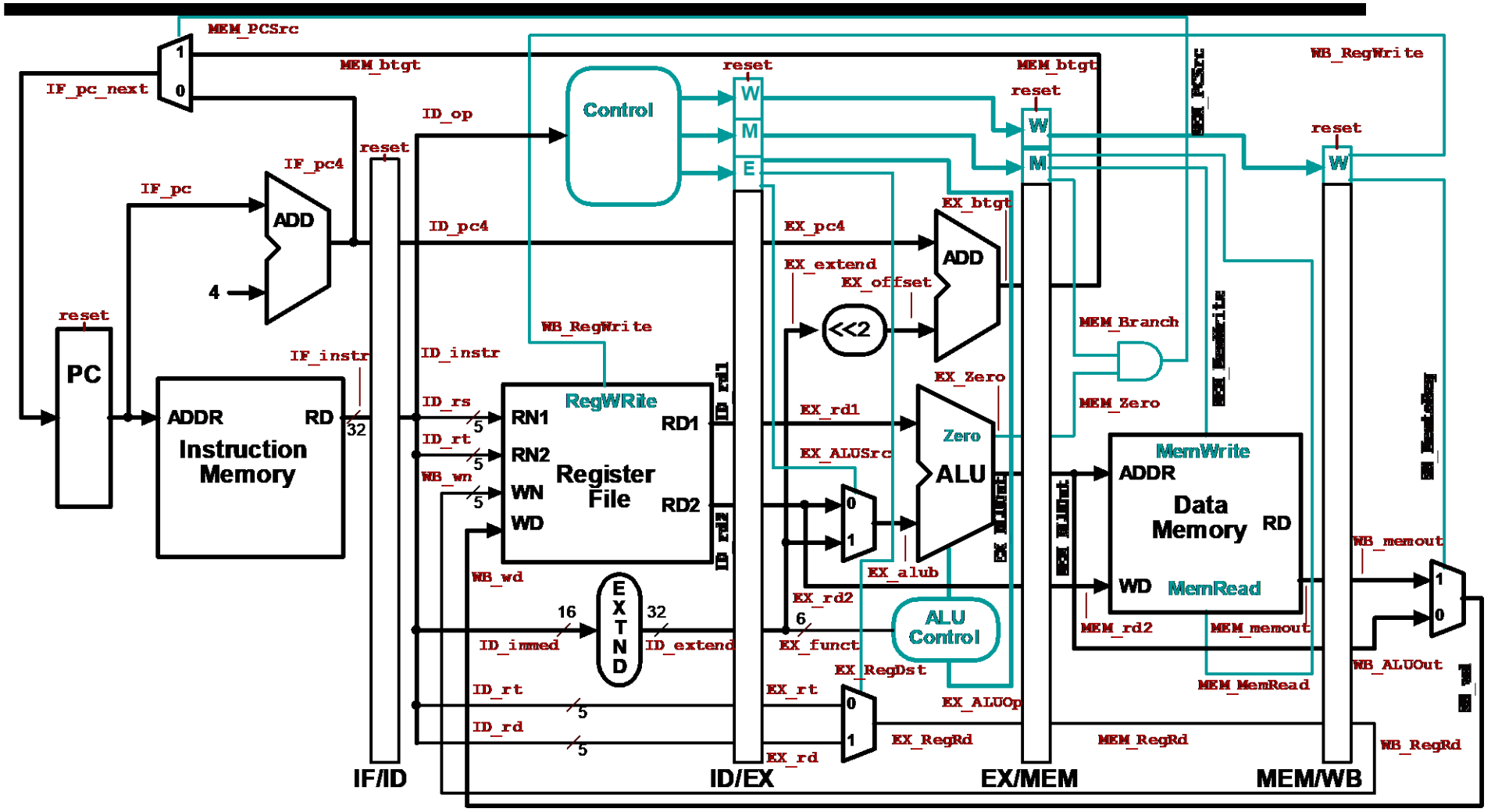
Computer Organization

Lecture 20 - Pipelined MIPS Verilog Project

Pipelining Outline

- Introduction
- Pipelined Processor Design
- Project 3: Verilog MIPS Pipeline Model

Demo - Pipelined MIPS Verilog Model

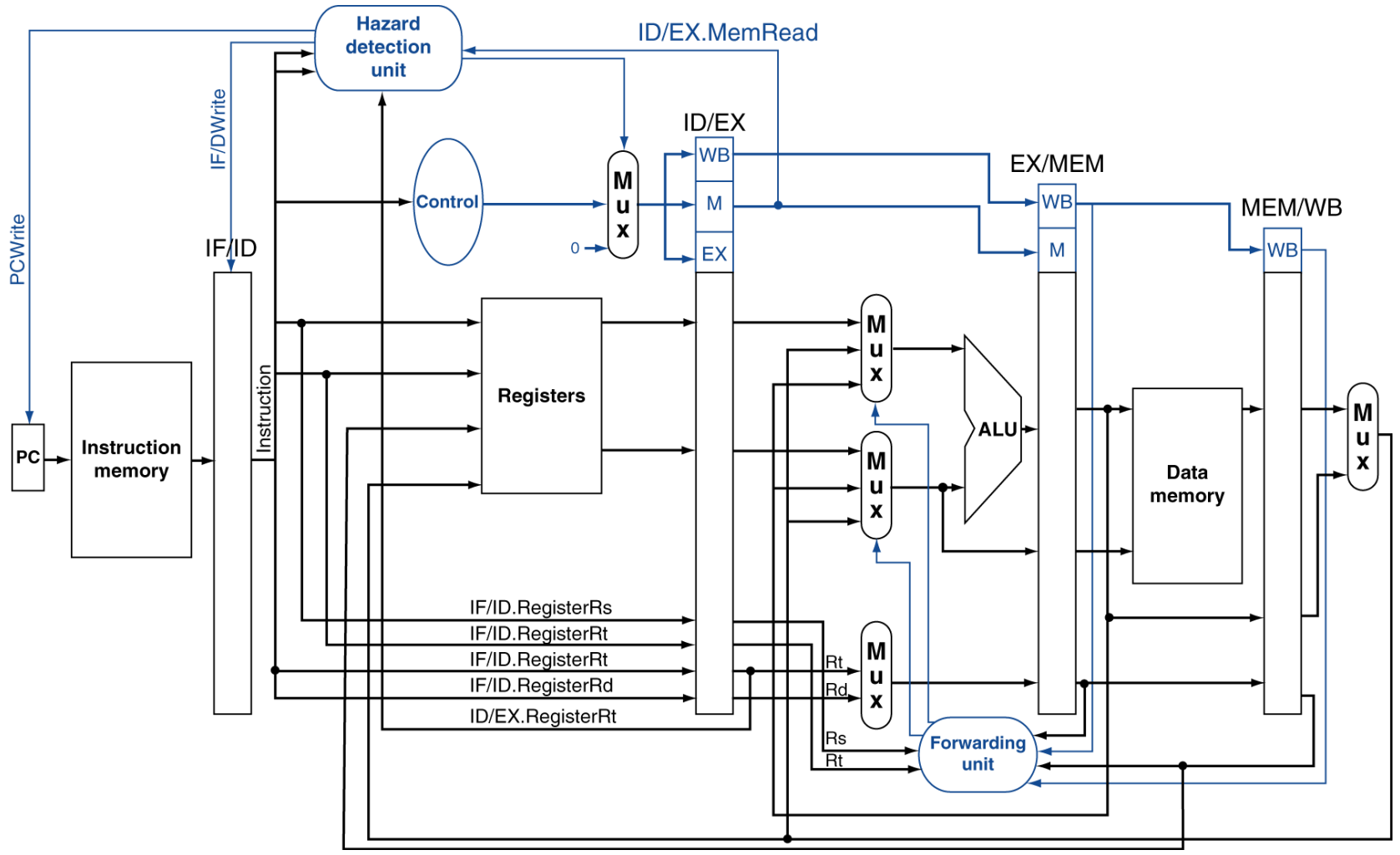


Project 3 - What to Do

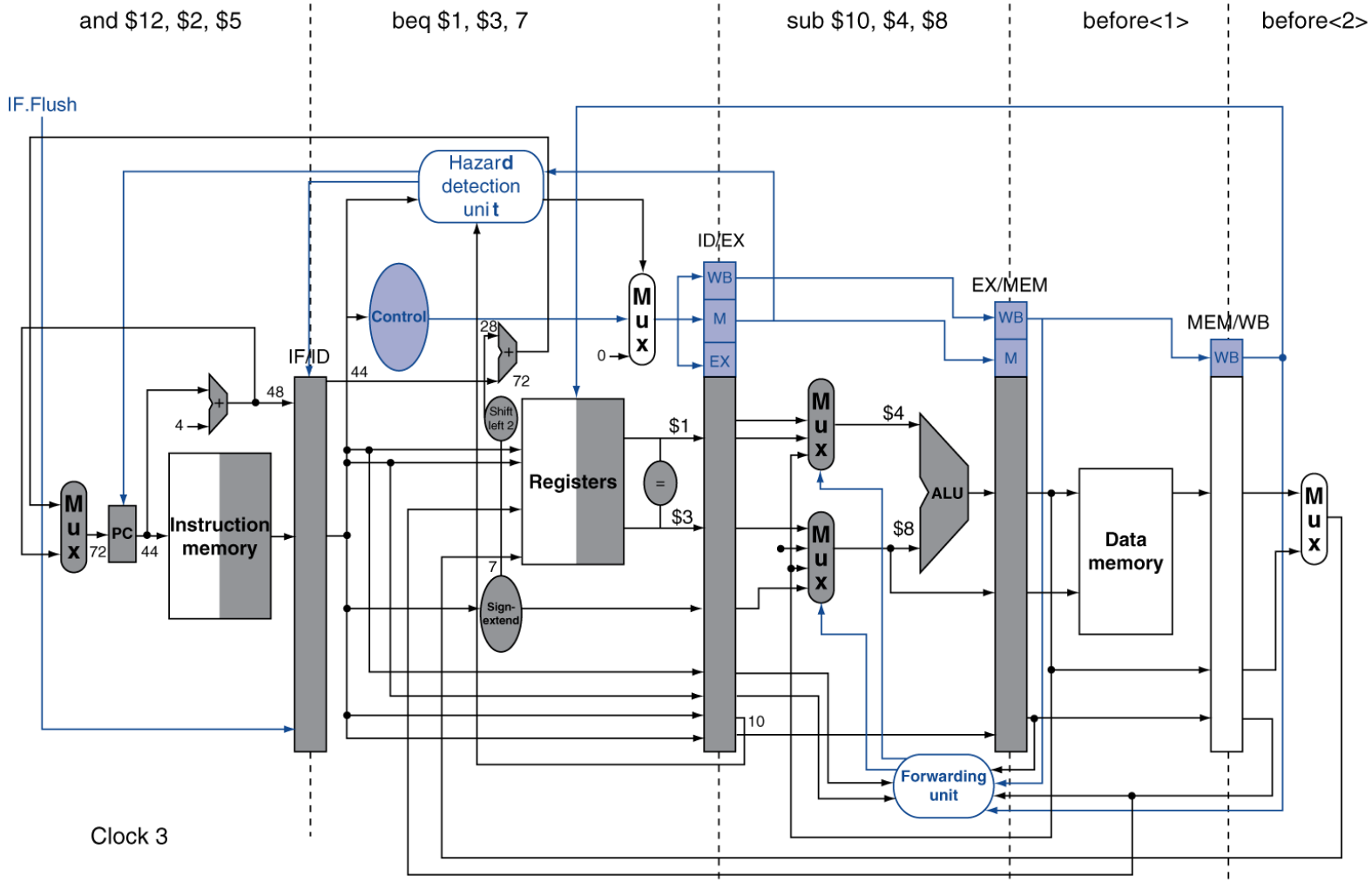
- Download & simulate basic model
- Add some more instructions:
  - `addi` - add immediate
  - `j` - jump
  - `jal` - jump and link
  - `jr` - jump register
- Simulate extended processor to show that it works
- Extend processor to do either
  - Data forwarding + load/use stall OR
  - Branch (and all jumps) implemented in ID including IF.Flush

  You may work in groups of two

Processor w/ Load-Use Hazard Detection



Example: Branch Hardware in ID



Roadmap for the term: major topics

- Overview / Abstractions and Technology
- Performance
- Instruction sets
- Logic & arithmetic
- Processor Implementation
- Memory systems
- Input/Output