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BTECH 3RD YEAR

MIT
Tutorial 6

Ans1: The following code achieves the desired task:-

```

RIM          ; Read Interrupt mask
MOV B, A     ; B ← A
ANI 20H      ; Check whether 6.5 is pending
JNZ NEXT
EI
RET          ; RST 6.5 is not pending
NEXT: MOV A, B ; Get bit pattern
ANI 0DH      ; Enables RST 6.5 by setting D4 = 0
ORI 08H      ; Enable SIM by setting D3 = 1
SIM
JMP SERV    ; Jump to service routine for RST 6.5

```

Ans2: Maskable Interrupts are those which can be disabled or ignored by the microprocessors.
These interrupts are either edge triggered or level triggered, so they can be disabled.
Eg:- INTR, RST 7.5, RST 6.5, RST 5.5

Non-maskable Interrupts are those which cannot be disabled or ignored by microprocessors.
TRAP is a non maskable interrupt.

Interrupt

Ans 3: The RIM means ~~Read~~ Read Instruction Mask which is used to read the status of interrupts which are pending or yet to be executed.

SIM means Set Interrupt Mask which is used to set those interrupts via the value from accumulator.

Ans 4: The instruction to enable all interrupts in 8085 system is:-

EI

Ans 5: DAA :- Decimal Adjust After Addition eg adjust HEX value to BCD value after addition by adding 6.
Eg: DAA ; Makes $A \leftarrow A+6$

DAD :- Adds the operand pair to HL pair exhibiting 16 bit addition.

LXI H 75H

DALXI D 536H

DAD D

; ~~H~~ $HL \leftarrow HL + DE$

XTHL :- Exchanges top of the stack with HL pair.

LXI H 75H ; $HL \leftarrow 75H$

CALL R ; $SP \leftarrow PC$

R: XTHL ; $H \leftarrow PC \text{ value}$

RET ; $PC \leftarrow 75H$

SPHL :- Copies HL pair value to Stack pointer.

Eg:-

LXI H 75H

SPHL ; SP ← HL

PCHL :- Copies HL pair value to PC

Eg:-

LXI H 75H

PCHL ; PC ← HL