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Tutorial 9

Ans 1: 8259 microprocessor is defined as Programmable Interrupt Controller (PIC) microprocessor.

There are 8 blocks in 8259A which are as follows:-

- Data bus buffer:-
This block is used as a mediator between 8259 and 8085/8086 microprocessor by acting as a buffer.
It takes control word from 8085 microprocessor and transfer it to the control logic of 8259 microprocessor.
After the selection of interrupt by 8259, it transfer the opcode of the selected interrupt and address of the Interrupt Service Sub routine to the other connected microprocessor.
It consists of 8 bits represented by D_7 to D_0.

- Read/Write logic:-
This block works only when CS is low. This block is responsible for the flow of data depending on the inputs of WR and RD.

- Control logic:-
It is the center of microprocessor and controls the functioning of blocks.
It has INTR pin which is connected with other microprocessor for taking interrupt request and pin INT for giving the acknowledgement

- Interrupt Request Register (IRR):-
It stores all the interrupt level which are requesting for Interrupt Services.

- Interrupt Service Register (ISR):-
It stores the interrupt level which are currently being executed.

- Interrupt Mask Register (IMR):-
It stores the interrupt level which have to be masked by storing the masking bits of the interrupt level.

- Priority ~~here~~ resolver:-
It examines the priority level of the interrupt using all the three registers and the interrupt with highest priority is set in ISR register. It resets those interrupt levels in IRR which have been serviced.

- Cascade Buffer:-
To increase interrupt handling capability, we can further cascade more number of pins by using cascade buffer.

The sequence of initialisation is as followed:-

```
;ICW1
mov  al, 13h    ; 1→ICW4 on, 1→Single IC, 0→ 8 bit interval
out  20h, al
;ICW2
mov al, 20h
out 21h, al
;ICW3
mov al, 04h
out 21h al
```

```
;ICW4
mov al, 11h          ; I → Nested Mode
out 21h, al
```

Ans 3:-

For ICW1,
the ~~Hexa~~ byte passed is :-

76h

→ 0 1 1 1 0 1 1 0

- ~~I~~ IVA ← No ICW4 configuration needed
- IVA ← Single PIC System
- IVA ← Call address interval is 4 bit
- 1 in PIC ← Operates in edge triggered mode

For ICW2,
the byte passed is :-

20h

Here 20h is the base address passed for the Interrupt Vector.