NIPIN Electrostatic Discharge (ESD) development for asymmetric voltage control using TCAD simulations

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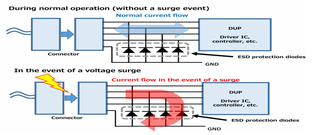
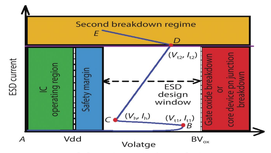
What is ESD

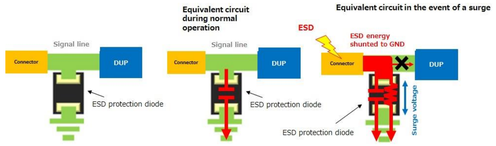
- ESD (Electrostatic Discharge) is the sudden flow of electricity between two charged objects. ESD generates sudden voltage and current transients that can damage solid-state components during manufacturing, assembly, or use.
- An ESD protection diode helps by quickly reacting to these spikes and preventing damage to sensitive parts. On-chip ESD protection devices offer a safe path to ground, shielding ICs from direct exposure to ESD events.
- ESD Design Window is a safe range where protection device activates – above normal operation (V_{dd}) and below breakdown voltage.



[2] Operation of ESD



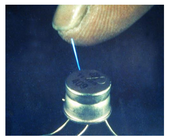
[1] Design Window of ESD



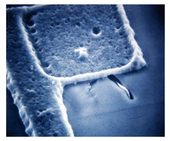
[2] ESD Device under Normal and Surge Operation

- During normal operation, ESD protection diodes behave as capacitors, forming low-pass filters with signal line resistance.
- In case of ESD, the ESD diode shunts much of the surge current into GND through them.

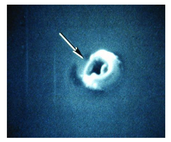
Why ESD Protection



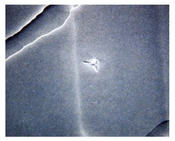
[3] ESD Arching



[3] ESD Damage



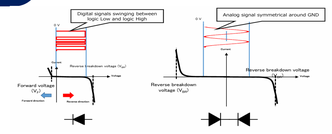
[3] ESD Damage



[3] ESD Damage

Objectives

- To design and develop a low-capacitance, unidirectional and Bidirectional ESD protection device that operates effectively below 1V, suitable for modern high-speed and low-power IC applications.



[2] Unidirectional and Bi-directional ESD

Why Asymmetry

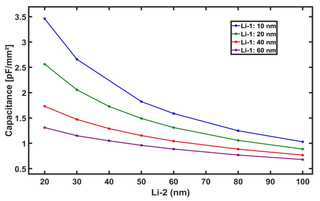
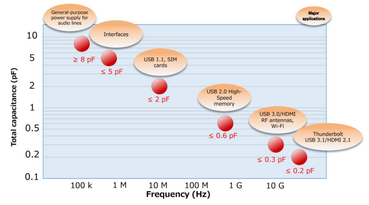


Fig. g



[2] Fig. h

❑ The asymmetric NIPIN diode structure offers advantages in terms of junction capacitance control compared to its symmetric counterpart. By introducing asymmetry, the depletion region can be engineered to extend more effectively toward one side, resulting in a lower junction capacitance under reverse bias conditions. This reduction in capacitance is beneficial for high-speed and ESD applications, as it leads to faster response times and minimized RC delay, thereby improving overall device performance.

Symmetric NIPIN

$$V_{b_0} \approx \frac{q N_a L_i L_{p^+}}{2\epsilon}$$

$$V_b = V_{b_0} - \frac{V_a}{2}$$

where, N_a is the doping concentration of the p+ region, L_i is the length of the intrinsic region, and L_{p+} represents the length of the p+ region. The equilibrium barrier height V_{b0} with different values of L_i , L_{p+} and N_a (as shown in Fig. 1(d)-(e)) aligns well with Equation, up to the point where the barrier height approaches the material's bandgap limit.

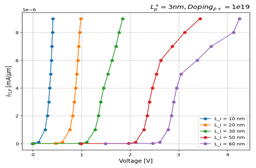


Fig. a

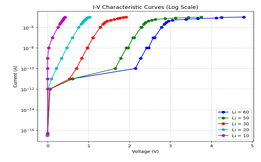


Fig. b

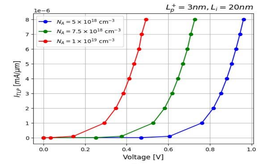


Fig. c

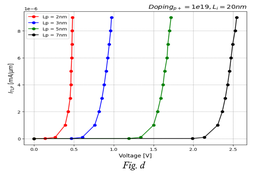


Fig. d

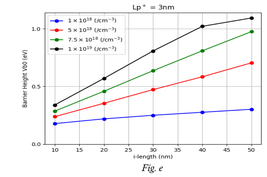


Fig. e

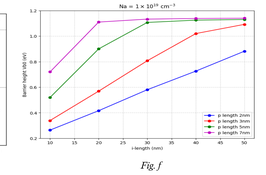
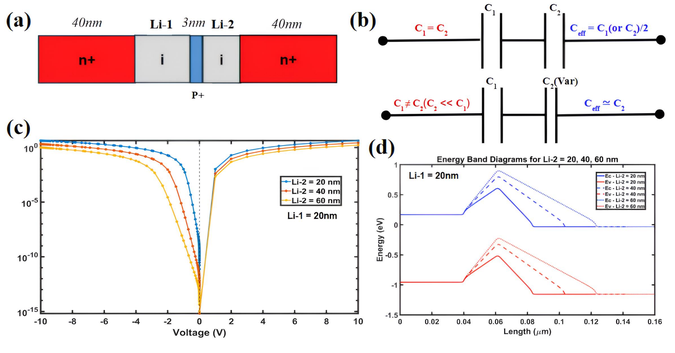


Fig. f

Simulated TLPcurrent vs voltage curve in (a) linear and (b) semi log scale for Li dependence varying from 10nm to 70nm for fixed Lp+ = 3nm and p+ doping of 1 e19/cm3 shows gradual increase in the breakdown voltage, (c) p+ doping dependence for fixed Li = 20 nm and Lp+ = 3nm showing voltage rise with doping, (d) Lp+ dependence for fixed Li = 20 nm and p+ doping of shows slight increase Lp+ increases breakdown voltage significantly

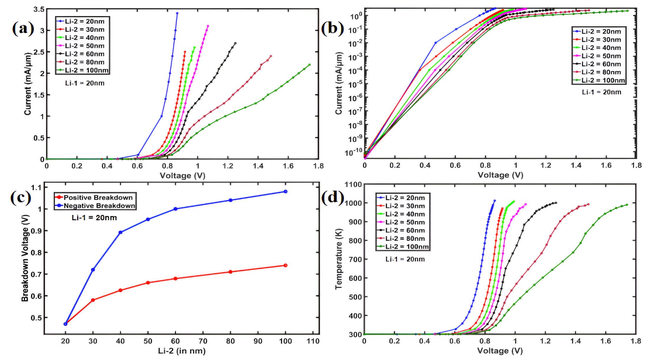
Asymmetric NIPIN

Structural overview and electrical behavior of an asymmetric NIPIN diode



Schematic (a–d) illustrates the asymmetrical NIPIN diode structure, capacitance model, IV response, and band diagrams. Increasing Li-2 leads to reduced C_eff, lower forward current, and delayed impact ionization due to a wider, flatter barrier.

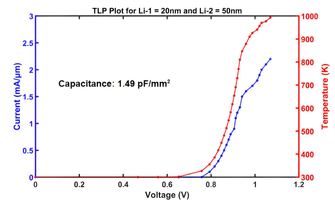
Electrical performance characteristics of the asymmetric NIPIN diode with varying Li-2



(a–d) TLP analysis shows increasing Li-2 raises breakdown voltage, alters leakage and subthreshold behavior, and causes asymmetric polarity response. Simulations also reveal thermal rise and impact ionization onset near breakdown.

Conclusion

TLP curve of the optimized asymmetric NIPIN diode: The plot shows simulated IV and Temp-V characteristics for the diode with Li-1 = 20nm and Li-2 = 50nm. The structure demonstrates sub-bandgap breakdown near 0.7V with a peak current of 2.2mA/μm at 1000K. The extracted junction capacitance is 1.49pF/mm 2 , highlighting the suitability of the design for highspeed, low-voltage system-level ESD protection.



We have submitted this work to SISPAD-2025 Conference

Device Design	Method	Capacitance (pf/mm²)	Polarity
n^+- p^+ - p^- - n^+	Expt.	127	Uni-di
n^+- p - n^+	Expt.	127	Bi-di
n^+- p^+	Expt.	2544	Uni-di
n^+- i - p^+ - i - n^+	Sim.	<2	Bi-di
n^+- i - p^+ - i - n^+ (This Work)	**Sim.**	**1.49 ***	**Uni-di**

Comparison with state-of-the-art devices

** This value corresponds to the case where Li-1 = 20nm and Li-2 = 50nm*

Future work

- *3-D TCAD Implementation of the asymmetrical NIPIN Diode*
- *Fabrication of the physical model of the simulated NIPIN Diode*

References

[1] J. Sakhuja, U. Ganguly, and S. Lashkare, "Low Voltage NIPIN Symmetric and Bi- Directional Diode for System Level ESD Protection," *IEEE Electron Device Letters*, vol. 45, no. 12, pp. 2483–2486, Dec. 2024, doi: https://doi.org/10.1109/led.2024.3477747.

[2] "Basics of TVS Diodes (ESD protection diodes)." Accessed: Apr. 20, 2025. [Online]. Available: https://toshiba.semicon-storage.com/content/dam/toshiba-ss-v3/master/en/semiconductor/knowledge/e-learning/basics-of-tvs-diodes/tvs-basic-e.pdf

[3] "Images of ElectroStatic Discharge Damage - SlideServe," *SlideServe*, Jan. 09, 2013. https://www.slideserve.com/nam/images-of-electrostatic-discharge-damage (accessed Apr. 20, 2025).

[4] J. Wu, Z. Yu, G. Hong, and R. Xie, "Design of GGNMOS ESD protection device for radiation-hardened 0.18 μm CMOS process," *Journal of Semiconductors*, vol. 41, no. 12, pp. 122403–122403, Dec. 2020, doi: https://doi.org/10.1088/1674-4926/41/12/122403.