NIPIN Diode with Designable Asymmetry for Low Voltage and Low Capacitance System Level ESD Protection

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***Abstract*—Scaling of CMOS technologies below 20nm and supply voltages under 1V intensifies the need of low voltage ESD protection. Conventional ESD diodes requires higher breakdown voltage (>>1V) to trigger Avalanche or Zener tunneling mechanism. Recently, symmetric NIPIN structure was shown having low breakdown voltage utilizing the sub-bandgap impact ionization for bi-directional ESD protection. Here, NIPIN strcuture with designbale asymmetry is demonstrated for low voltage unidirectional ESD protection. Further, a reduction in capacitance is demonstrated which is needed for high speed interfaces. The designed NIPIN diode achieves ∼25% less capacitance than symmetric diode with V_{BD}∼0.66V. The design provides an efficient, scalable solution for protecting high-speed, low-voltage I/O interfaces for system level ESD protection.**

***Index Terms*—ESD protection, low voltage, asymmetric diode, punch-through, impact ionization, capacitance reduction**

I. Introduction

Electrostatic Discharge (ESD), characterized by the sudden, transient flow of electricity between two charged objects, generates abrupt voltage and current spikes. These transients pose a significant threat, capable of causing irreversible damage to solid-state components during various stages, including manufacturing, assembly, and end-user interaction. Consequently, effective ESD protection is paramount to ensure the reliability and longevity of electronic systems.

ESD protection devices are designed to provide a safe, conductive path to ground, thereby shielding sensitive ICs from direct exposure to damaging ESD events. These protective measures can be implemented both on-chip for component-level ESD requirements and off-chip for system-level protection. Component-level ESD, often encountered during manufacturing and assembly, is typically addressed by on-chip solutions designed to meet standards such as the Human Body Model (HBM), Machine Model (MM), and Charged Device Model (CDM) [1]. However, the end-user environment introduces much higher ESD stresses, making on-chip protection insufficient. Thus, robust system-level (off-chip) ESD protection, as defined by stringent standards like International Electrotechnical Commission (IEC) 61000-4-2 [2], becomes essential.

The drive towards lower operating voltages in ICs, now often below 1V, necessitates the development of low-voltage system-level ESD protection solutions [3]. Furthermore, a wide array of modern applications, including low-voltage GPIOs for Microcontroller Units , sub-20nm Input/Outputs (I/Os), and high-speed interfaces such as Thunderbolt3, Thunderbolt4, USB Type C, USB3.2 Gen2, and USB4, demand compact ESD solutions with ultra-low capacitance that can operate effectively at or below 1V [4]-[8].

Conventionally, ESD protection has relied on devices like Zener and avalanche diodes. However, these devices often prove unsuitable for modern low-voltage applications due to high leakage currents, large parasitic capacitance, and breakdown voltage limitations. Commercially available system-level ESD protection devices, predominantly p-n diodes, are typically unidirectional and operate in either the avalanche (for >5V working voltage with light doping) or Zener (for <5V working voltage with heavy doping) breakdown regions. The heavy doping required for Zener breakdown at lower voltages leads to increased leakage current and higher capacitance.

These limitations have spurred the development of alternative p-n junction designs for low voltages, including multiple forward-biased diodes [9], punch-through diodes (n+-p-n+) [10], and graded base doping (n+-p+-p–n+) diodes [11], [12]. Nevertheless, these solutions are generally limited to operation around 1V, as the quest for significantly lower breakdown voltages is fundamentally constrained by the material's bandgap

[13]. Recently, novel impact ionization mechanisms have been demonstrated to overcome this bandgap limitation and achieve sub-bandgap voltage operation .

Building on these advancements, this work proposes an asymmetrically engineered punch-through NIPIN (n+–i–p+–i–n+) diode for versatile low-voltage system-level ESD protection. Unlike symmetric NIPIN designs, asymmetry in the device allows increased overall i-region resulting in significantly lower capacitance. A narrow p+ region forms a triangular energy barrier, enabling sub-bandgap breakdown via impact ionization and facilitating voltage control potentially below 0.5V through optimization of intrinsic region lengths and p+ region characteristics . TCAD simulations validate the design, showing tunable breakdown behavior and low capacitive loading. The optimized asymmetric NIPIN diode exhibits sub-bandgap breakdown near 0.7V with a peak current of $2.2mA/\mu m$ and an extracted junction capacitance of 1.49 pF/mm², providing its suitability for high-speed, low-voltage system-level protection with excellent clamping voltage.

II. Device Structure

The NIPIN *(n^+-i-p^+-i-n^+)* diode schematic (Fig. 1(a)) illustrates its layered structure, comprising two n^+ regions with a central p^+ region strategically sandwiched between two intrinsic (i) regions. These intrinsic regions lengths are denoted as L_{i1} and L_{i2} The critical aspect of this design, which differentiates it from its symmetric NIPIN diode, is the variation in the lengths of these intrinsic regions (L_{i1} and L_{i2}).

In this NIPIN structure, the n^+ terminals serve as the emitter and collector of an open-base BJT. The ultra-thin p^+ region, typically ranging from 2nm to 7nm, plays a pivotal role in modulating carrier transport within the device. This ultra-thin p^+ region enables a triangular energy barrier (Fig. 1(d)) with a barrier height (V_{b0}) at equilibrium. The barrier height at equilibrium is proportional to the p^+ region doping concentration (N_a), the intrinsic region length (L_i), and the p^+ region length (L_{p+}).

The mechanism enabling the ultra-low voltage breakdown in the asymmetric NIPIN is sub-bandgap impact ionization . This phenomenon allows the device to conduct current effectively at voltages below the material's inherent bandgap, which is a significant departure from conventional breakdown mechanisms. Electrons residing in the tail of the Boltzmann distribution, even at lower applied biases (¡1V), can gain sufficient kinetic energy ($E > E_c$) to initiate impact ionization, thereby generating electron-hole pairs. Subsequently, the generated holes get trapped in the valence band. These trapped, positively charged holes effectively lower the energy barrier, leading to a substantial increase in the over-the-barrier electron current. This process establishes a positive feedback loop, resulting in a sharp, exponential rise in current at sub-bandgap voltages. The asymmetric NIPIN's design leverages this established sub-bandgap impact ionization mechanism, but controls the electric field profiles through intrinsic region length variations to achieve directional breakdown. Further, the i-region can control the capacitance.

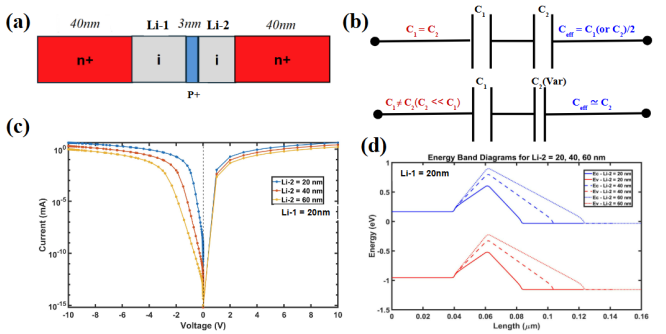

Fig. 1. **Asymmetric NIPIN diode Schematic and Electrical Characteristics:** (a) Schematic of the proposed asymmetrical NIPIN diode structure, showing two intrinsic regions (L_{i1} and L_{i2}) of varying lengths and a central p^+ region to enable punch-through and sub-bandgap impact ionization. (b) Capacitor model of the diode, where total capacitance is modeled as two series capacitors, C_1 and C_2, corresponding to the intrinsic regions. In symmetric, C_1=C_2 and C_{eff}=C_1(or C_2)/2. In asymmetric, $C_{eff} \sim C_2$(as $C_1 >> C_2$). (c) Simulated IV characteristics showing asymmetric breakdown (0.6V at +ve vs 3.2V at -ve breakdown for L_{i2}=50nm) and $\sim$10$\times$ leakage reduction at L_{i2}=100nm. (d) Energy band diagrams for L_{i2} = 20nm, 40nm, and 60nm, illustrating how the triangular barrier becomes wider and flatter with increasing L_{i2}, reducing electric field strength and delaying the onset of impact ionization.

III. Results and Discussion

The device is stressed with Transmission Line Pulse (TLP) of 100ns with 10ns rise/fall time for the devices with Li, Lp+ and p+ doping. The voltage developed across the device is measured by averaging between 70ns to 90ns. The simulations were carried out using Sentaurus TCAD. Along with drift-diffusion (DD) and continuity equations, doping dependence Recombination, Avalanche (UniBo2) and Thermodynamic model is incorporated to the simulations.

A. Breakdown Characteristics and Thermal Behavior

Fig. 2(a) shows the Transmission Line Pulse (TLP) current-voltage characteristics for different L_{i2} values. The breakdown voltage (V_{BD}) increases from $\sim$0.66V to $\sim$0.82V as L_{i2} grows from 20nm to 100nm. This follows the relationship $V_b \propto L_i$, where longer intrinsic regions create higher triangular barriers that require greater voltage to initiate impact ionization.

Fig. 2(b) demonstrates V_{BD} saturation beyond 60nm, where the barrier height approaches silicon's bandgap limit (1.2eV). The asymmetric operation is confirmed by polarity-dependent breakdown: at L_{i2} = 50nm, positive bias breakdown occurs at 0.6V while negative bias requires 1V. This asymmetry indicates structural or doping non-uniformities in the device, leading to direction-dependent impact ionization thresholds.

Fig. 2(c) shows peak temperatures exceeding 1000K during breakdown, with thermal runaway initiating at lower currents for longer L_{i2} (2.5mA/μm at 60nm vs 2.2mA/μm at 100nm) due to higher electric fields accelerating Joule heating. These elevated temperatures pose reliability concerns, as they can lead to material degradation, electromigration, or irreversible damage in nanoscale devices.

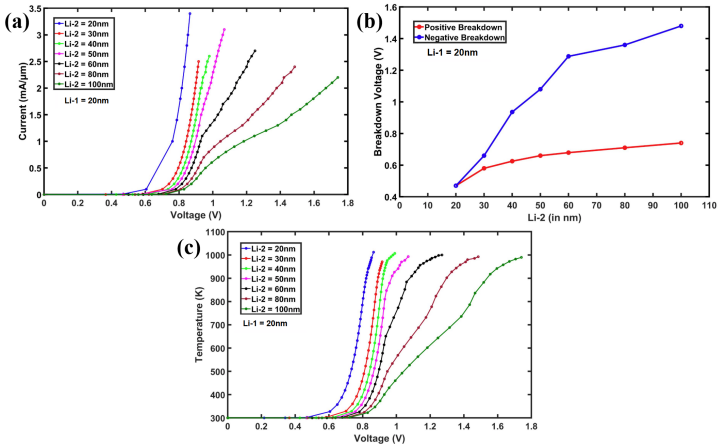

Fig. 2. **Electrical performance characteristics of the asymmetric NIPIN diode with varying L_{i2}:** (a) TLP curves for different L_{i2} values, showing a shift in breakdown voltage with increasing intrinsic length.(b) Breakdown voltage plotted against L_{i2}, showing a steady increase and saturation beyond ∼60nm. In symmetric diode, both polarity breakdown are same but in asymmetric diode, both polarity breakdowns are different. (c) Simulated temperature rise with voltage, indicating the onset of impact ionization and thermal effects at breakdown for different L_{i2} values.

B. Capacitance Reduction via Asymmetric Design

The capacitance reduction mechanism comes from the series capacitor model in Fig. 1(b).

This model explains the inverse relationship between capacitance and intrinsic length shown in Fig. 3. For asymmetric designs ($L_{i1} \neq L_{i2}$), the effective capacitance is dominated by the longer intrinsic region since $C_{\text{eff}} \approx C_2$ when $L_{i1} \ll L_{i2}$ [6].

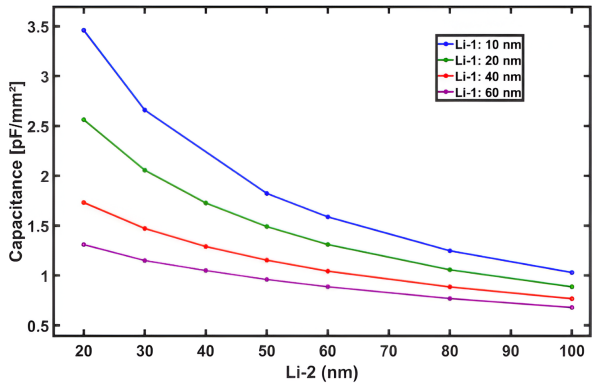

Fig. 3. **Capacitance dependence on intrinsic region lengths in the asymmetric NIPIN diode:** The plot shows the variation of junction capacitance as a function of L_{i2} for different fixed values of L_{i1}. Capacitance decreases consistently with increasing L_{i2}, while lower L_{i1} values exhibit higher overall capacitance. The reduced sensitivity beyond ∼80–100nm in L_{i2} indicates a saturation trend, highlighting design tradeoffs for optimizing ESD protection in high-speed, low-voltage applications.

C. Dynamic Resistance Trade-off

Figure 4 shows R_{dyn} increasing from ∼0.52Ω to ∼0.71Ω as L_{i2} grows from 20nm to 80nm. This occurs because longer intrinsic regions widen the energy barrier, reducing the rate of current increase with voltage ($\partial I/\partial V$) during punch-through conduction.

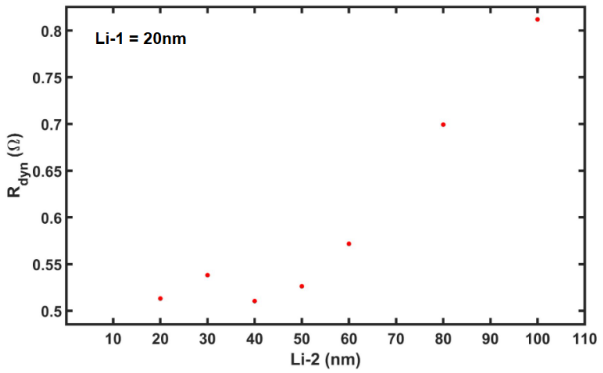

Fig. 4. **Dynamic resistance variation with L_{i2}:** The figure shows the extracted dynamic resistance (R_{dyn}) of the asymmetric NIPIN diode as a function of L_{i2}. The (R_{dyn}) increases with longer intrinsic region length.

The configuration L_{i1} = 20nm and L_{i2} = 50nm (Fig. 5) achieves optimal balance with Sub-bandgap V_{BD}=0.66V at 0.2mA/μm, confirming impact ionization below the silicon band gap [2]. The capacitance reduces to 1.49 pF/mm^2 - 25% lower than the symmetric NIPIN, confirming the impact of the intrinsic length scaling.

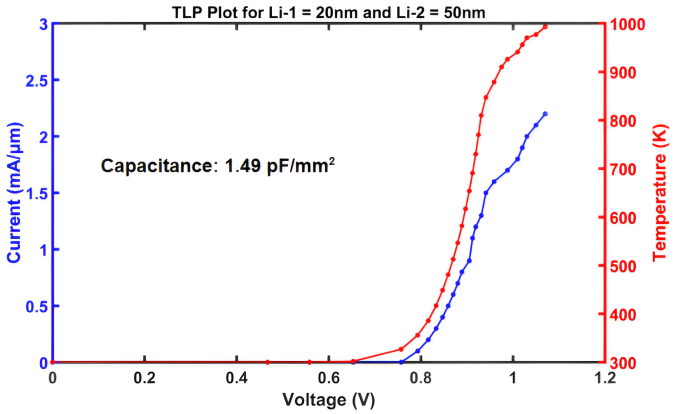

Fig. 5. **TLP measurements of the asymmetric NIPIN diode:** The plot shows simulated IV and Temperature-V characteristics for the diode with L_{i1} = 20nm and L_{i2} = 50nm. The structure demonstrates sub-bandgap breakdown near 0.7V with a peak current of 2.2mA/μm at 1000K. The extracted junction capacitance is 1.49pF/mm^2

TABLE I: Comparison with state-of-the-art devices

Device Design	Capacitance (pf/mm²)	Polarity
n^+- p^+ - p^- - n^+ [14]	127	Uni-di
n^+- p - n^+ [14]	127	Bi-di
n^+- p^+ [14]	2544	Uni-di
n^+- i - p^+ - i - n^+ [6]	<2	Bi-di
n^+- i - p^+ - i - n^+ (This Work)	**1.49 ***	**Controllable**

* This is a particular case where Li-1 = 20nm and Li-2 = 50nm, the capacitance is variable and dependent on intrinsic region length.

Table I demonstrates significant advantages over existing solutions: he table summarizes different device configurations with their physics, junction capacitance, and conduction polarity. Compared to prior experimental and simulated designs, the proposed asymmetrical NIPIN diode achieves the lowest reported capacitance (1.49pF/mm^2) for asymmetric operation. This value corresponds to the case where L_{i1} = 20nm and L_{i2} = 50nm, with overall capacitance tunable based on intrinsic region lengths.

IV. Conclusion

Low-voltage (<1V) ESD protection with low capacitance remains a critical challenge for low voltage high speed interfaces. This work demonstrates an asymmetric NIPIN (n^+–i–p^+–i–n^+) diode engineered through variable intrinsic region lengths. The device achieves sub-bandgap breakdown at 0.66V via triangular barrier-controlled impact ionization. The asymmetric design provides 25% capacitance reduction (1.49 pF/mm^2) versus symmetric counterparts, demonstrating tunable asymmetric protection as needed with high-speed I/O interfaces.

V. ACKNOWLEDGMENT

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References

[1] R. van Dalen, G. E. J. Koops, and O. Pfennigstorf, "Punch-through diodes as replacement for low-voltage zener diodes in ESD protection circuits," J. Electrostatics, vol. 61, nos. 3–4, pp. 149–169, Jul. 2004.

[2] B. Das, S. Sushama, J. Schulze, and U. Ganguly, "Sub-0.2 v impact ionization in Si n-i-p-i-n diode," IEEE Trans. Electron Devices, vol. 63, no. 12, pp. 4668–4673, Dec. 2016.

[3] J. Urresti, S. Hidalgo, D. Flores, J. Roig, I. Cortés, and J. Rebollo, "Lateral punch-through TVS devices for on-chip protection in low-voltage applications," Microelectron. Rel., vol. 45, nos. 7–8, pp. 1181–1186, Jul. 2005.

[4] J. W. Slotboom and H. C. de Graaff, "Bandgap narrowing in silicon bipolar transistors," IEEE Trans. Electron Devices, vol. ED-24, no. 8, pp. 1123–1125, Aug. 1977.

[5] SEMTECH. (Feb. 9, 2021). RClamp1011ZC Femto Farad RailClamp® 1-Line, 200fF ESD Protection. RClamp1011ZC. [Online]. Available: https://www.semtech.com/products/circuit-protection/lowcapacitance/rclamp1011zc

[6] J. Sakhuja, U. Ganguly, and S. Lashkare, "Low Voltage NIPIN Symmetric and Bi-directional Diode for System Level ESD Protection," IEEE Electron Device Lett., 2024.

[7] R. Meshram et al., "High performance triangular barrier engineered NIPIN selector for bipolar RRAM," in Proc. IEEE Int. Memory Workshop, 2014.

[8] W. Simbürger, D. Johnsson, and M. Stecher, "High Current TLP Characterisation: An Effective Tool for the Development of Semiconductor Devices and ESD Protection Solutions," EOS/ESD Symp., 2012.

[9] M. Miao, Y. Zhou, J. A. Salcedo, J.-J. Hajjar, and J. J. Liou, "A New Method to Estimate Failure Temperatures of Semiconductor Devices Under Electrostatic Discharge Stresses," IEEE Electron Device Lett., vol. 37, no. 11, pp. 1477–1480, 2016.

[10] J. Urresti, S. Hidalgo, D. Flores, J. Roig, I. Cortés, and J. Rebollo, "Lateral punch-through TVS devices for on-chip protection in low-voltage applications," Microelectron. Rel., vol. 45, nos. 7–8, pp. 1181–1186, Jul. 2005, doi: 10.1016/j.microrel.2004.10.023.

[11] N. Z. Butt and M. A. Alam, "Scaling limits of double-gate and surround gate Z-RAM cells," IEEE Trans. Electron Devices, vol. 54, no. 9, pp. 2255–2262, Sep. 2007, doi: 10.1109/TED.2007.902691.

[12] J. S. B, Monishmurali, A. Singh, and M. Shrivastava, "3D TCAD studies of snapback driven failure in punch-through TVS diodes under system level ESD stress conditions," in Proc. 42nd Annu. EOS/ESD Symp. (EOS/ESD), 2020, pp. 1–9.

[13] M. Lundstrom, Fundamentals of Carrier Transport, 2nd ed. Cambridge, U.K.: Cambridge Univ. Press, Jul. 2009, ch. 8.

[14] Y.-C. King, B. Yu, J. Pohlman, and C. Hu, "Punchthrough diode as the transient voltage suppressor for low-voltage electronics," IEEE Trans. Electron Devices, vol. 43, no. 11, pp. 2037–2040, Aug. 1996, doi: 10.1109/16.543049.