Low Voltage Asymmetric Uni-Directional NIPIN Diode for System Level ESD Protection

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***Abstract*—Scaling of CMOS technologies below 20nm and supply voltages under 1V intensifies the need for low-capacitance ESD protection. Conventional ESD diodes requires higher breakdown voltage (>>1V) to enable Avalanche or Zener tunneling mechanism. Recently, NIPIN structure was shown having low breakdown voltage. However, the structure is symmetric which is not suitable for unidirectional ESD protection. Further, the capacitance is limited by symmetric structure. Here we propose an asymmetric ESD protection device which can provides ESD protection at lower voltages but also ensures low capacitance. The structure shows reduced capacitance and increased breakdown voltage with longer Li-2, and diminished sensitivity beyond ∼80–100nm. For Li-1 = 20nm and Li-2 = 50nm, it achieves ∼25% less capacitance then symmetric diode with V_{BD}∼0.66V. This design provides an efficient, scalable solution for protecting high-speed, low-voltage I/O interfaces.**

***Index Terms*—Capacitance reduction, High-speed I/O, Low-voltage protection, Unidirectional conduction.**

I. Introduction

As CMOS technologies scale and supply voltages drop below 1V, modern ICs face increased vulnerability to ESD. Conventional protection devices like Zener and avalanche diodes are unsuitable at these voltages due to high leakage, capacitance, or breakdown limits [1]. With growing demand in sub-20nm nodes, high-speed links, and low-voltage GPIOs, compact ESD solutions with minimal capacitance are essential. NIPIN is proposed for low voltage protection [2]. The NIPIN diode utilizes sub-bandgap impact ionization to enable a low voltage ESD protection [3][4]. However, they do not provide a uni-directional protection which is required for various low voltage electronics [5][6]. This work proposes an asymmetrically engineered punch-through NIPIN (n^+–i–p^+–i–n^+) diode, Figure 1(a) for unidirectional, low-voltage system-level ESD protection. By varying intrinsic region lengths, the structure achieves directional conduction and reduced junction capacitance. A narrow p^+ region forms a triangular energy barrier, Figure 1(d), enabling sub-bandgap breakdown via impact ionization. TCAD simulations validate the design, showing tunable breakdown behavior, Figure 1(c), and low capacitive loading suitable for high-speed interfaces.

II. DEVICE STRUCTURE AND CONCEPT

The proposed device is an asymmetric NIPIN (n^+–i–p^+–i–n^+) diode where directional conduction is achieved by extending one intrinsic region (Li-2), thereby breaking the structural symmetry. The n^+terminals function as the emitter and collector of an open-base BJT, while the ultra-thin p^+ region modulates carrier transport.

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III. Results and Discussion

A. TLP Simulations and Device Specifications

The asymmetric NIPIN diode was simulated using 100ns TLP pulses with 10ns rise/fall times in Sentaurus TCAD. Breakdown voltage were found to depend on the Li. In this, we varied the length of one intrinsic region and found that breakdown voltage increases with Li, Figure 2.

B. Capacitance Reduction via Asymmetry

Under the full-depletion approximation, the total capacitance per unit area is given by:

$$C = \frac{\varepsilon}{L_{i1} + L_{i2}} \tag{1}$$

This equation is verified by trend of Figure 4. For L_{i1} = 20nm and L_{i2} = 50nm, it achieves $1.49\,\mathrm{pF/mm^2}$ capacitance and V_{BD} = 0.66V, Figure 5.

IV. Conclusion

The asymmetric NIPIN diode shows decreasing capacitance and increasing breakdown voltage with increasing L_{i2}, higher capacitance for smaller L_{i1}, and reduced sensitivity beyond $\sim$ 80–100 nm. For L_{i1} = 20nm and L_{i2} = 50nm, it achieves reduction of ∼25% capacitance with V_{BD} = 0.66V (<1V) suitable for high-speed GPIO protection.

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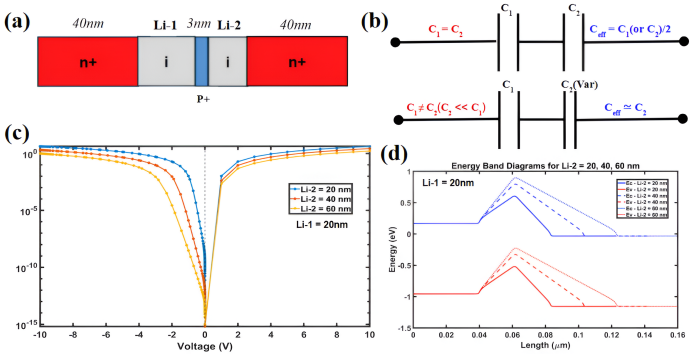

Fig. 1. **Structural overview and electrical behavior of the asymmetric NIPIN diode:** (a) Schematic of the proposed asymmetrical NIPIN diode structure, showing two intrinsic regions (Li-1 and Li-2) of varying lengths and a central p^+ region to enable punch-through and impact ionization. (b) Capacitor model of the diode, where total capacitance is modeled as two series capacitors, C_1 and C_2, corresponding to the intrinsic regions. In symmetric, C_1=C_2 and C_eff=C_1(or C_2)/2. In asymmetric, $C_eff \sim C_2$(as $C_1 >> C_2$). (c) Simulated IV characteristics for varying Li-2 values under positive and negative bias, showing unidirectional current conduction as breakdown voltages are different for opposite polarity and reduced forward current with increasing Li-2. (d) Energy band diagrams for Li-2 = 20, 40, and 60nm, illustrating how the triangular barrier becomes wider and flatter with increasing Li-2, reducing electric field strength and delaying the onset of impact ionization.

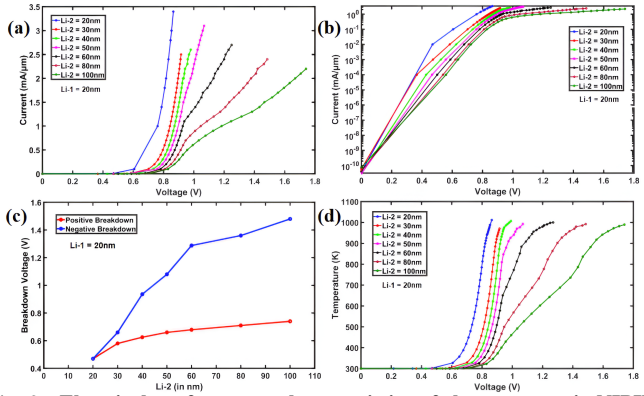

Fig. 2. **Electrical performance characteristics of the asymmetric NIPIN diode with varying Li-2:** (a) TLP curves for different Li-2 values, showing a shift in breakdown voltage with increasing intrinsic length. (b) Corresponding log-scale plot emphasizing leakage behavior and subthreshold conduction. (c) Breakdown voltage plotted against Li-2, showing a steady increase and saturation beyond ∼80–100nm. In symmetric diode, both polarity breakdown are same but in asymmetric diode, both polarity breakdowns are different. (d) Simulated temperature rise with voltage, indicating the onset of impact ionization and thermal effects at breakdown for different Li-2 values.

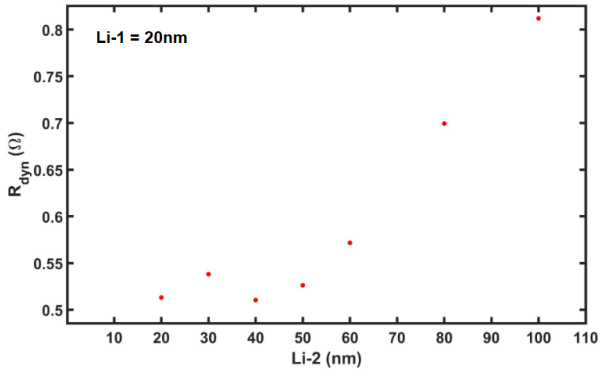

Fig. 3. **Dynamic resistance variation with Li-2:** The figure shows the extracted dynamic resistance (R_{dyn}) of the asymmetric NIPIN diode as a function of Li-2. It increase with longer intrinsic region length.

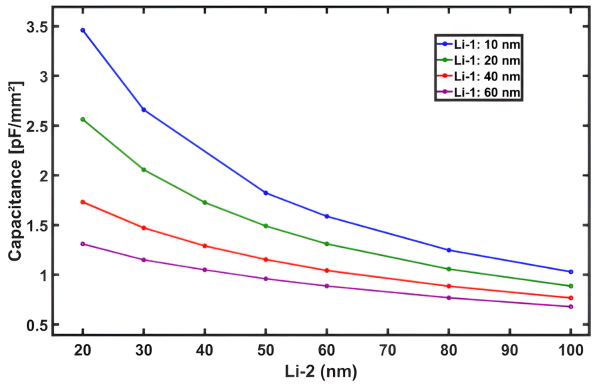

Fig. 4. **Capacitance dependence on intrinsic region lengths in the asymmetric NIPIN diode:** The plot shows the variation of junction capacitance as a function of Li-2 for different fixed values of Li-1. Capacitance decreases consistently with increasing Li-2, while lower Li-1 values exhibit higher overall capacitance. The reduced sensitivity beyond ∼80–100nm in Li-2 indicates a saturation trend, highlighting design tradeoffs for optimizing ESD protection in high-speed, low-voltage applications.

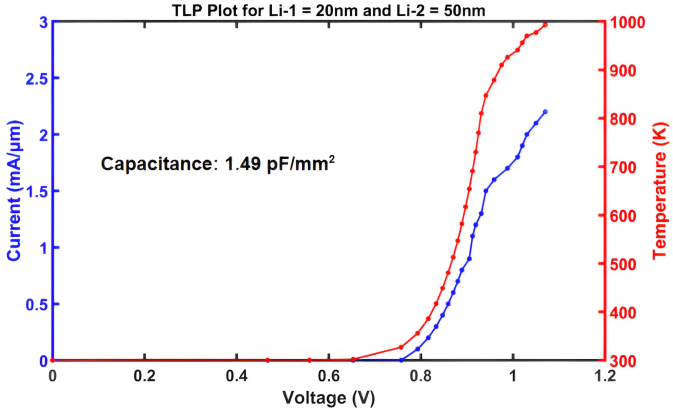

Fig. 5. **TLP curve of the optimized asymmetric NIPIN diode:** The plot shows simulated IV and Temp-V characteristics for the diode with Li-1 = 20nm and Li-2 = 50nm. The structure demonstrates sub-bandgap breakdown near 0.7V with a peak current of 2.2mA/μm at 1000K. The extracted junction capacitance is 1.49pF/mm^2, highlighting the suitability of the design for high-speed, low-voltage system-level ESD protection.

Device Design	Physics	Capacitance (pf/mm²)	Polarity
n^+- p^+ - p^- - n^+	Open Base BJT	127	Uni-di
n^+- p - n^+	Open Base BJT	127	Bi-di
n^+- p^+	Zener	2544	Uni-di
n^+- i - p^+ - i - n^+	Sub Band-Gap Impact Ionisation	<2	Bi-di
n^+- i - p^+ - i - n^+ (This Work)	**Sub Band-Gap Impact Ionisation**	**1.49 ***	**Uni-di**

* This is a particular case where Li-1 = 20nm and Li-2 = 50nm, the capacitance is variable and dependent on intrinsic region length.

Fig. 6. **Comparison with state-of-the-art devices:** The table summarizes different device configurations with their physics, junction capacitance, and conduction polarity. Compared to prior experimental and simulated designs, the proposed asymmetrical NIPIN diode achieves the lowest reported capacitance (1.49pF/mm^2) for unidirectional operation. This value corresponds to the case where Li-1 = 20nm and Li-2 = 50nm, with overall capacitance tunable based on intrinsic region lengths.