

Low Voltage NIPIN Symmetric and Bi-Directional Diode for System Level ESD Protection

Jayatika Sakhija^{ID}, Graduate Student Member, IEEE, Udayan Ganguly^{ID}, Senior Member, IEEE, and Sandip Lashkare^{ID}, Member, IEEE

Abstract— Low voltage (<1V) bi-directional and symmetric electrostatic discharge (ESD) protection devices are essential for system level ESD protection of low voltage electronics such as Low voltage GPIO for MCU, Sub-20nm I/O's, and potentially for next gen interfaces USB3.2 Gen2, Thunderbolt 4. Here, a triangular barrier designed Silicon NIPIN (n^+ -i- p^+ -i- n^+) punch-through diode with variable voltage <0.5V to 2V is proposed for low-voltage system level ESD protection. The NIPIN diode utilizes the sub-bandgap voltage impact ionization to enable the ultra-low voltage breakdown. The control over the breakdown voltage is demonstrated via TCAD simulations by controlling the lengths of intrinsic, and p^+ -doped regions and the doping of p^+ -doped region. Finally, standoff voltage and clamping voltages are compared with other low voltage protection devices and demonstrate near ideal voltage performance of the NIPIN protection device. Such a low voltage ESD protection with low clamping voltage is a critical development for low-voltage electronics.

Index Terms— System level ESD, low-voltage, punch-through, impact ionization.

I. INTRODUCTION

ELCTROSTATIC discharge (ESD) is a major threat for the solid state components failure in an electronic system. The ESD events are voltage and current transients which are a result of sudden discharge of the stored charge. These ESD events can damage integrated circuits (ICs) at various stages during manufacturing, assembly to end-user interaction. Hence, it is essential to have ESD protection devices which can provide the ESD events a conductive path towards ground avoiding any interaction with the IC. The ESD protection devices can be designed on-chip. The on-chip ESD protection

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Jayatika Sakhija and Udayan Ganguly are with the Electrical Engineering Department, Indian Institute of Technology Bombay, Mumbai 400076, India.

Sandip Lashkare is with the Department of Electrical Engineering, Indian Institute of Technology Gandhinagar, Palaj, Gujarat 382055, India (e-mail: sandip.lashkare@iitgn.ac.in).

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devices are designed for *component level ESD* requirements which may occur during the manufacturing and assembly where the ESD events are much more controlled. The component level ESD test models are the Human Body Model (HBM), the Machine Model (MM) and the Charged Device Model (CDM) [1].

However, in the end-user environment, the ESD events can be much greater than the component level ESD requirements where the on-chip protection becomes insufficient. Hence, a *system level (off-chip) ESD protection* is essential to protect the ICs from ESD events at the end-user environments defined in International Electrotechnical Commission (IEC) 61000-4-2 [2]. The requirements of IEC are much more stringent than what is required for the component level ESD protection.

With the technological advancements, the operating voltages of ICs have reduced to <1V. Hence, to protect the ICs, such low voltage system level ESD protection is required [3]. Further, various applications like Low voltage GPIO for MCU, Sub-20nm I/O's, and high speed interfaces such as Thunderbolt3, Thunderbolt4, USB Type C, USB3.2 Gen2 and USB4 interfaces require a low voltage ($\leq 1V$) ESD protection [4], [5], [6], [7], [8]. Hence, a symmetry controllable, bi-directional designable low voltage device is critical [9]. The commercially available system level ESD protection devices are majorly p-n diodes which are unidirectional and are designed to operate in Avalanche or Zener breakdown region. For >5V working voltage, the p-n region is designed with light doping where the breakdown is initiated by Avalanche mechanism. For <5V working voltage, the p-n region is heavily doped where breakdown is initiated by Zener mechanism. However, the high doping leads to higher leakage current and increase in capacitance.

These limitations of Zener diodes led to various developments of p-n junctions targeted for low voltages such as multiple forward biased diodes [10], punch-through diode (n^+ - p - n^+) [11], graded base doping (n^+ - p^+ - p - n^+) diode [9], [10], [12]. However, the solutions are limited to ~1V. The quest of lowering the breakdown voltage is typically limited by bandgap of the material [13]. Recently, to further lower the voltage below bandgap, a sub-bandgap voltage enabled impact ionization mechanism was demonstrated [16], [17], [18], [19].

In this work, a triangular barrier engineered punch-through NIPIN (n^+ -i- p^+ -i- n^+) diode is proposed and demonstrated for low voltage bi-directional and symmetry controllable system

level ESD protection. Here, a triangular barrier is designed and controlled with ultra-thin p⁺ region. The impact ionization in triangular barrier allows the voltage control lower than 0.5V by having control over i-region length, p⁺ region doping and length through TCAD simulations. Further, the controllable symmetric/asymmetric structure enables the bi-directional/uni-directional along with voltage control. Finally, clamping voltage is compared with literature to demonstrate close to ideal performance of the NIPIN diode.

II. DEVICE STRUCTURE AND CONCEPT

The device schematic with n⁺-i-p⁺-i-n⁺ layers is shown in Fig. 1 (a). The n⁺ regions form emitter and collector of an open base BJT. The base region is formed of p⁺ region sandwiched between two intrinsic (i) region [20]. This structure can be modelled as a simple two capacitor in series model (Fig. 1(b)). Here, the p⁺ region is ultra-thin (2nm to 7nm) which leads to the triangular barrier with barrier height V_{b0} at equilibrium (1) as shown in (Fig. 1(c)). The non-linear current change is enabled by the barrier modulation (V_{b0}) for the applied voltage (V_a) as given in (2).

$$V_{b0} \approx \frac{qN_aL_iL_{p^+}}{2\epsilon} \quad (1)$$

$$V_b = V_{b0} - \frac{V_a}{2} \quad (2)$$

where, N_a is p⁺ region doping, L_i is i-region length and L_{p⁺} is p⁺ region length. The barrier height modulation at equilibrium (V_{b0}) for various L_i, L_{p⁺} and N_a (Fig. 1(d)-(e)) shows consistency with (1) until the maximum barrier height close to bandgap is reached. The results for the experimental NIPIN device is shown in Fig. 1(f). The details of the device fabrication process are described in [19] and [20]. The doping profile in simulations is modified according to the experimental SIMS data which leads to similar simulated dc-iv results with experimental dc-iv. The simulations with impact ionization turned on shows good match with experiments. The effect of sub-bandgap impact ionization can be observed in (Fig. 1(g)) where experimentally calibrated dc-iv with and without impact ionization shows sharp current rise below <1V.

The impact ionization is caused by electrons which possess sufficient kinetic energy (E > E_G). Typically, when the applied bias is more than the bandgap, few electrons gain sufficient energy (E > E_G) and enable impact ionization. Previously, for the lower applied bias (<1V), impact ionization was demonstrated by the electrons in the tail of the Boltzmann distribution which have sufficient energy (E > E_G) to impact ionize and generate electron (e)-hole (h) pairs [14]. The electrons escape to the contact. However, holes get trapped in the valence band well. These stored holes being positively charged, lower the energy barrier increasing the over the barrier electron current. This leads to the positive feedback and gives rise to the exponential rise in current [19], [20].

III. RESULTS AND DISCUSSION

The device is stressed with Transmission Line Pulse (TLP) of 100ns with 10ns rise/fall time for the devices with L_i, L_{p⁺} and p⁺ doping [12], [21]. The voltage developed across the device is measurement by averaging between 70ns to 90ns. The simulations were carried out using Sentaurus TCAD. Along with drift-diffusion (DD) and continuity equations,

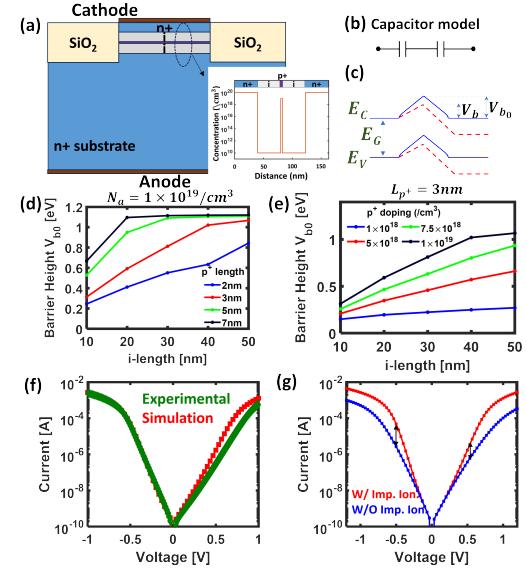


Fig. 1. (a) A device schematic with n⁺-i-p⁺-i-n⁺ layers with inset showing doping profile, (b) a simple capacitor model for NIPIN structure, (c) Simulated (blue) band diagram with barrier height at equilibrium (blue) and under applied bias (red), Simulated barrier height for various i-region lengths along with (d) p⁺ length for fixed p⁺ doping (N_a) of 1 × 10¹⁹/cm³, (e) p⁺ doping for fixed L_{p⁺} = 3nm showing that barrier height is proportional to i- and p⁺ lengths, p⁺ doping, (f) Experimental and simulations with impact ionization turned on showing good match, (g) experimentally calibrated dc-iv showing with and without impact ionization showing the sub-bandgap impact ionization at <1V.

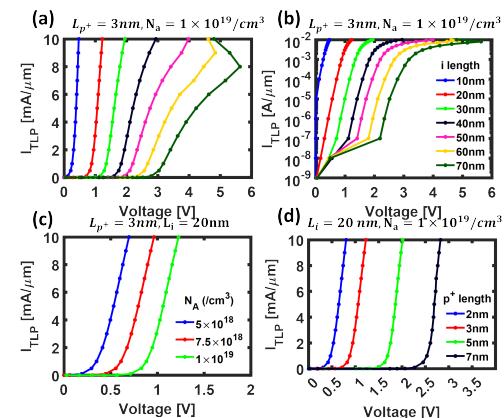


Fig. 2. Simulated TLP current vs voltage curve in (a) linear and (b) semi-log scale for L_i dependence varying from 10nm to 70nm for fixed L_{p⁺} = 3nm and p⁺ doping of 1 × 10¹⁹/cm³ shows gradual increase in the breakdown voltage, (c) p⁺ doping dependence for fixed L_i = 20 nm and L_{p⁺} = 3nm showing voltage rise with doping, (d) L_{p⁺} dependence for fixed L_i = 20 nm and p⁺ doping of shows slight increase L_{p⁺} increases breakdown voltage significantly.

doping dependence Recombination, Avalanche (UniBo2) and Thermodynamic model is incorporated to the simulations. The leakage current and breakdown voltage of the NIPIN diode is dependent the initial barrier height (1). The barrier height can be controlled by L_i, L_{p⁺} and p⁺ doping.

A. Li Dependence

The impact of L_i is shown in Fig. 2(a)- 2(b). Here, the p⁺ is fixed with doping of 1×10¹⁹ /cm³ and p⁺ length of 3nm. It is observed that, for L_i = 10nm to 70nm, the breakdown voltage increased from ~0.2V to 3V. This is consistent

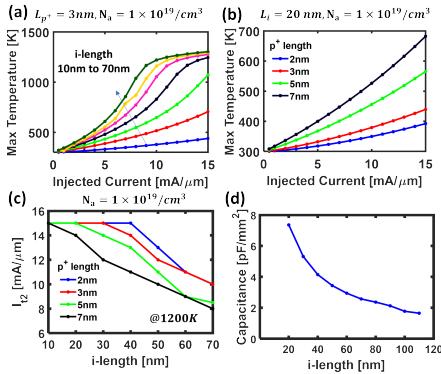


Fig. 3. (a) Maximum temperature in the device for fixed injected currents with L_i , and (b) L_{p^+} , as the lengths and injected current increases, the temperature rises significantly due to high E-fields at higher voltages, (c) The failure current is calculated when the maximum temperature exceeds 1200°K , (d) Decrease in capacitance with increasing i-length showing inverse relationship.

with (1). Due to low barrier height for $L_i = 10\text{nm}$, a large leakage can be observed (blue curve) in Fig. 2(b). This leakage decreases as L_i is increased due to increase in the barrier height (Fig. 1(c)). For larger lengths, the failure currents (I_{t2}) can be observed for lower currents i.e. $9\text{mA}/\mu\text{m}$ at $L_i = 60\text{nm}$ and $8\text{mA}/\mu\text{m}$ at $L_i = 70\text{nm}$ due to high voltages and subsequent increase in electric field led temperature rise.

B. p^+ Doping Dependence

Similar to L_i , gradual breakdown voltage control can be seen with p^+ doping (Fig. 2(c)). It is important to note that the p^+ doping needs to be on higher side to make sure the triangular barrier with larger barrier height to suppress leakage current. Slight lower doping ($5 \times 10^{18}/\text{cm}^3$) reduces the barrier height leading to larger leakage current.

C. L_{p^+} Dependence

Further, a significant change in breakdown voltage can be seen for L_{p^+} (Fig. 2(d)). This can be correlated with hitting the maximum barrier height at higher L_{p^+} and disappearance of triangular barrier.

Next, maximum temperature (T_{max}) in the device is analysed. For a given injected current, T_{max} is found out by first finding the maximum spatial temperature across the device for different time instants in the TLP simulations. Then, T_{max} is noted from after one complete TLP simulation. The T_{max} for different injected currents with L_i and L_{p^+} shows temperature rise and saturation for higher L_i (Fig. 3(a-b)) when injected current reaches $\sim 10\text{mA}/\mu\text{m}$. The failure current (I_{t2}) for different lengths is shown in Fig. 3(c). The I_{t2} is measured when device is assumed to have failed at 1200K [12], [22]. The I_{t2} are in the range of $8 - 15\text{mA}/\mu\text{m}$. Further, the capacitance decreases with increasing i-length due to inverse relationship (Fig. 3(d)). This low capacitance makes NIPIN suitable for high-speed interface circuits [4], [5], [6], [7], [8].

The breakdown voltage dependence is shown for various L_i and L_{p^+} (Fig. 4(a)). Similar to L_i dependence, increase in L_{p^+} lengths lead to increase in the breakdown voltage. This is consistent with (1). The breakdown voltage is considered at $1\text{mA}/\mu\text{m}$ where device start to show conductive behaviour. The standoff voltage is considered at 80% of the breakdown

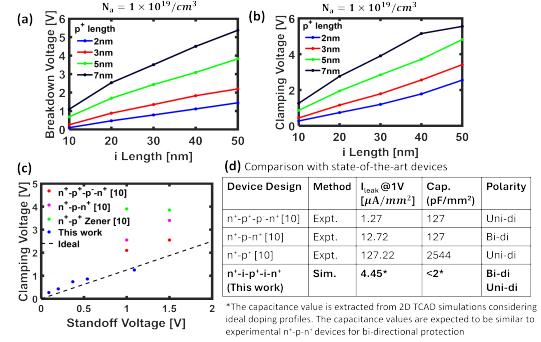


Fig. 4. (a) Breakdown and (b) Clamping voltage for various p^+ region lengths, (c)-(d) comparison of various other ESD protection devices with the proposed NIPIN diode. The NIPIN shows lower standoff voltage ($<0.5\text{V}$) and have near ideal performance (dotted line) due to lower clamping voltages with competitive leakage and capacitance performance.

voltage [10]. The clamping voltage is considered at $8\text{mA}/\mu\text{m}$. The breakdown voltage and clamping voltage for different lengths are shown in (Fig. 4(a)-4(b)). As the lengths increase, the breakdown voltage and clamping voltages increases.

Finally, the NIPIN device is compared with other TVS devices i.e. Zener diode, punch-through (n^+-p-n^+) diode and graded punch-through ($n^+-p^+-p^-n^+$) diode (Fig. 4(c)). The NIPIN results are TCAD 2D simulation results and the results are more ideal. Experimental packaged device will add the parasitic and may degrade the performance. Ideally, clamping voltage should be equal to breakdown voltage i.e. negligible dynamic resistance. This line is shown by dotted black line. It can be observed that the NIPIN device not only shows the lower and controllable stand-off voltage ($<0.5\text{V}$), but also has lower dynamic resistance reducing clamping voltage significantly. Further, the leakage and capacitance is competitive with other TVS devices (Fig. 4(d)). For the similar area ($0.6\text{mm} \times 0.3\text{mm}$) of [4], the capacitance can be reduced $<0.3\text{pF}$. Although this capacitance is smaller, the device assumes an ideal junction having uniform doping, abrupt junctions and scaling from 2D TCAD simulations (Fig. 1(a)). The capacitance value will be higher for the experimental devices for graded doping profiles (which will effectively reduce i-region increasing capacitance) with experimental parasitic and will be similar to N+-P-N+ device capacitance. The subsequent work will explore the limitations and scope for improvements in the capacitance to be used for high-speed interfaces.

IV. CONCLUSION

The low voltage ($<1\text{V}$) system level silicon based ESD protection is extremely challenging. Here, the implementation of a triangular barrier engineered device is demonstrated for low-voltage system level ESD protection. The punch-through diode is implemented with $n^+-i-p^+-i-n^+$ to allow triangular barrier control and enable impact ionization at sub-bandgap voltages ($<0.5\text{V}$). Along with the low voltages, the device symmetry allows to have a symmetry controllable bi-directional diode. Such a device having voltage control beyond 1V can play a significant role for low-voltage electronics interfaces.

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