3C7 Integrated System Design

Lab Session A

Aim:

The purpose of this session is to familiarise yourself with the Vivado environment for behavioural simulation.

Learning Outcomes:

On completing this lab session you will be able to:

- Simulate a basic design in Vivado
- Create, modify and organise projects within Vivado
- Use the waveform window to monitor a simulation
- Gather useful skills for future write-ups

Instructions:

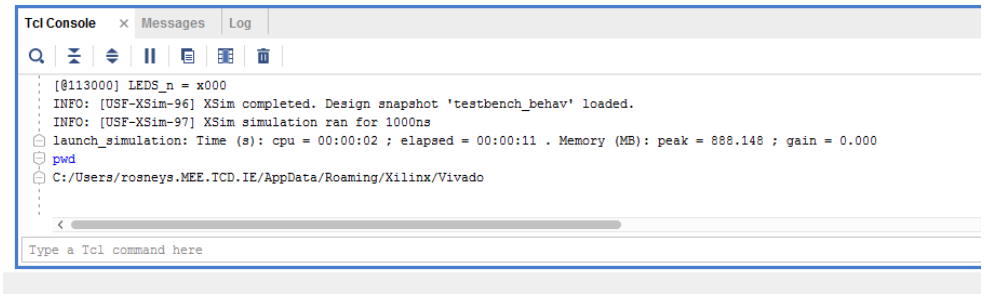
1. The tutorial you will follow is documented in **Vivado_tutorial.pdf**. This is supplied with the LabA files. The document title is "Vivado Design Suite Tutorial". Open it up (and check you have the correct document!).
2. Go through all parts of the tutorial. Follow the instructions in each chapter. *Note that for each chapter you have extra tasks listed below to allow assessment of your progress. You should open a blank MS Word document to start saving some of the outputs required.*

   Anywhere you see this symbol, be sure to read the note I have added.

Figure 1: Note symbol in the PDF

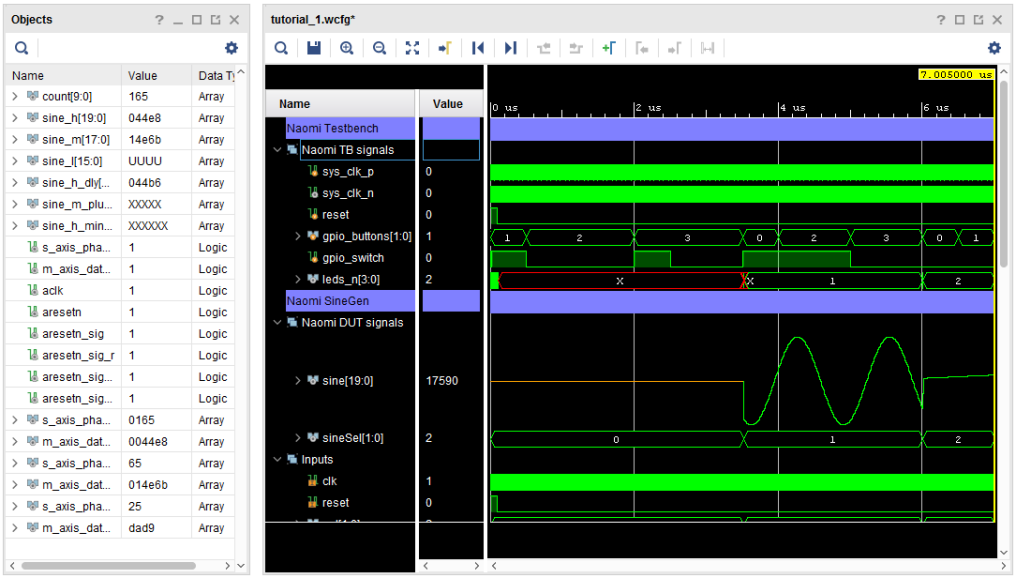
3. A short description of each part is provided below. Save your work at the specified points in each part (by taking screenshots, e.g. with Snipping Tool).
   - Vivado Simulator Overview
     Read through this chapter. At this stage, you do not need to worry about the specifics of what the design does. We are just using the tutorial to learn about the simulation environment.

   - Lab 1: Running the Simulator in Vivado IDE
     This is where your work begins. Follow the steps, remembering to read the added notes. When you first run the behavioural simulation (Step 3, no. 5), type pwd in the Console window. This will display your working directory. Do a screen grab to show you have gotten this far. Crop it to just show the console; it should look something like this:



- Lab 2: Debugging the Design
  In this chapter are the skills that you will be using again and again in 3C7.

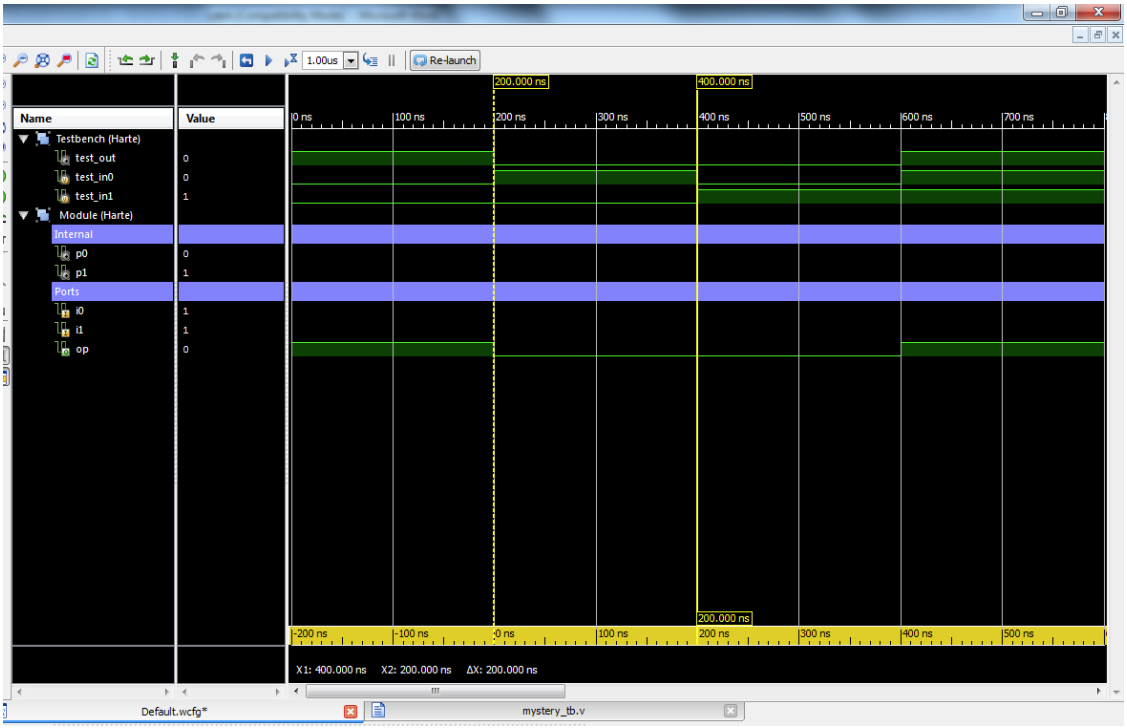
  After adding the signal groups and dividers, capture your own version of Figure 21. First, edit the groups and dividers to include your surname. Once again crop it to the relevant region.



Your version of Figure 21 should look something like this

Under the Using Markers, Cursors and Measuring Time section (Step 8), capture your own version of Figure 27, after completing no. 13.

4. Now you are on your own! I have supplied a Verilog module and testbench called mystery_module.v and mystery_tb.v. You need to make a new project and add these files to it. Then you need to show you have run a behavioural simulation of the design. Add signals to the waveform, use appropriate naming for dividers and group names for signals and the other things you have learnt in the tutorial.
5. Save a suitably complete and organised waveform, also showing that the transition time between testvectors is 200ns. An example of what this will look like is shown below.



Example of final waveform

6. Determine the function of the mystery module!

Submission:
You must submit the following parts, contained in a single PDF, via Blackboard:

- Labelled waveforms demonstrating the design is working where instructed
- A short description explaining the function of the mystery module

Name it LabA_surnameinitial.pdf, e.g. LabA_harten.pdf.

Deadline: Wednesday 30th Jan 2019. Refer to handbook for Late Assignment Policy.

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And do this tutorial:
https://libguides.tcd.ie/friendly.php?s=plagiarism/ready-steady-write

Plagiarism will result in loss of **ALL** marks for this assignment.