Trinity College Dublin
Coláiste na Tríonóide, Baile Átha Cliath
The University of Dublin

3C7 DIGITAL SYSTEM DESIGN LABORATORY

Lab Session B

Department of Electronic and Electrical Engineering

(e-Report submission)

Lab:

1. 2-bit equal comparator
2. 8-bit gate-level greater-than-or-equal-to circuit

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Lab 1. 2-bit equal comparator

The given assignment starts with initialization of new project with the provided testbench and dependent modules. The provided module eq2 provided had following errors which were resolved.

After adding these design sources and making the fixes to module eq2, finally the behavioural simulation was started.

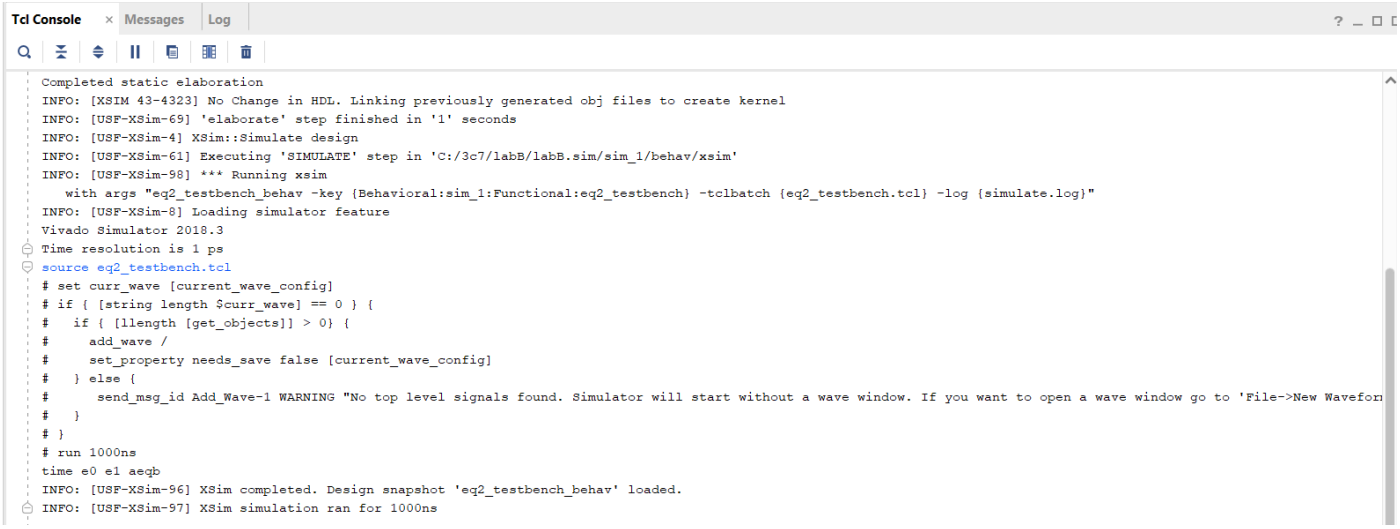

Figure 1.1. TCL Console

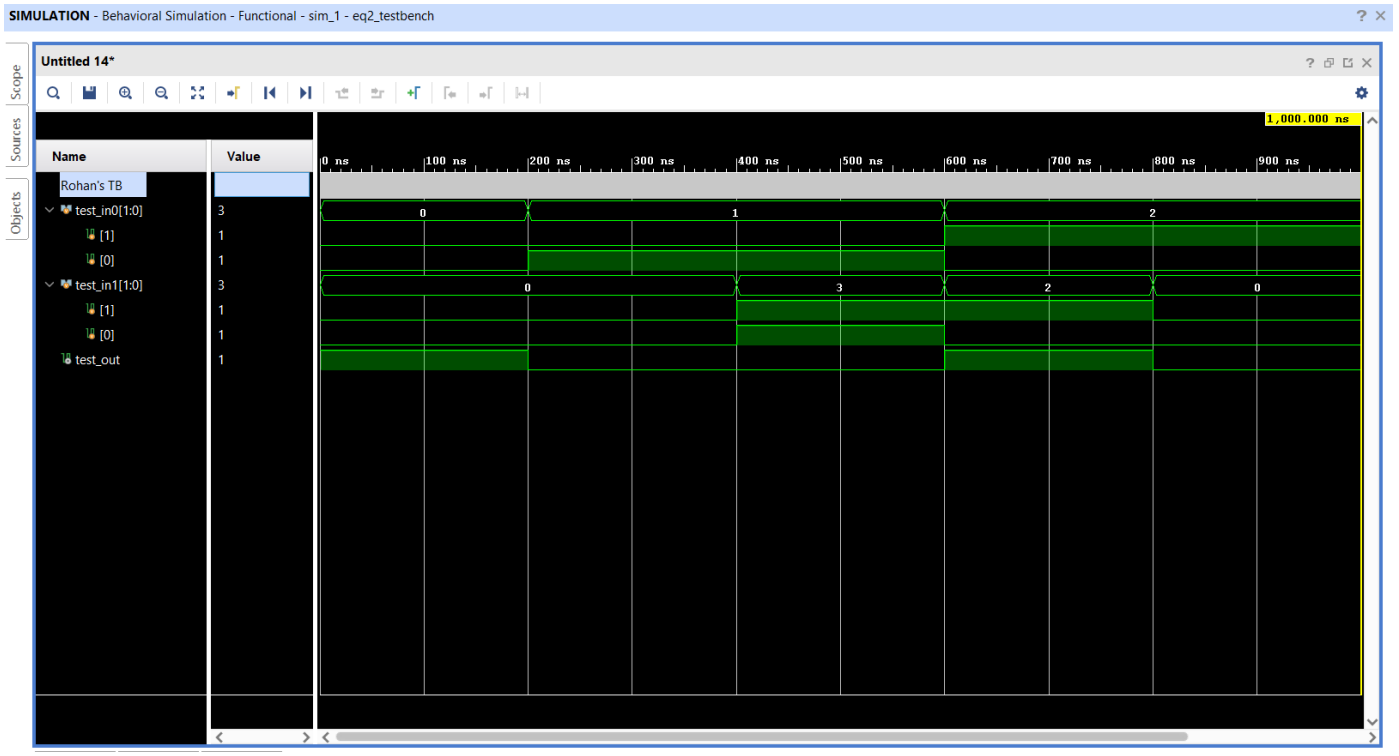

Figure 1.2. 2-bit comparator waveform

Lab 2. 8-bit gate-level greater-than-or-equal-to circuit

After modifying the Verilog coded module eq2 and eq1. It was made compatible to work for 2-bit greater than and equal.

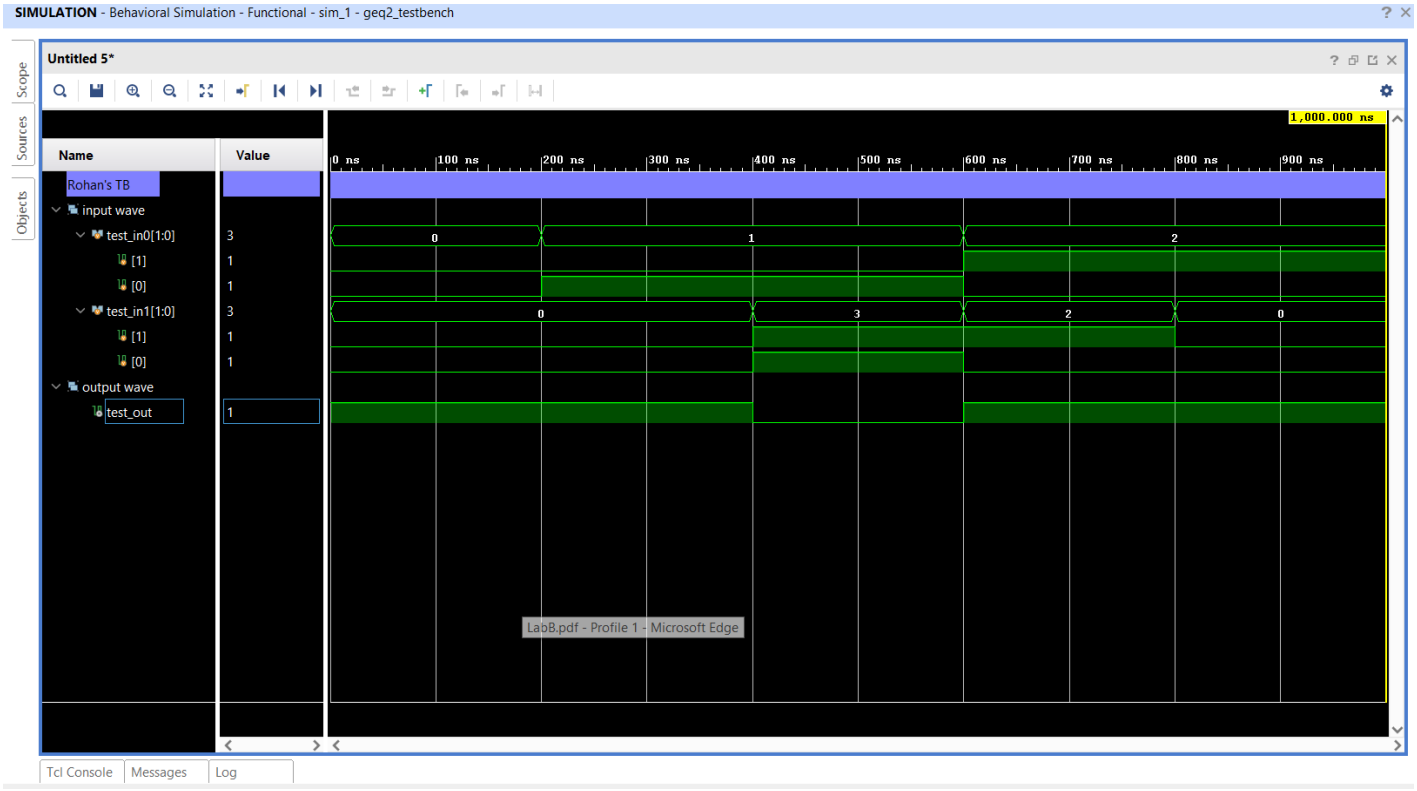

Figure 2.1. 2-bit comparator in bit0 greater than equal to bit1

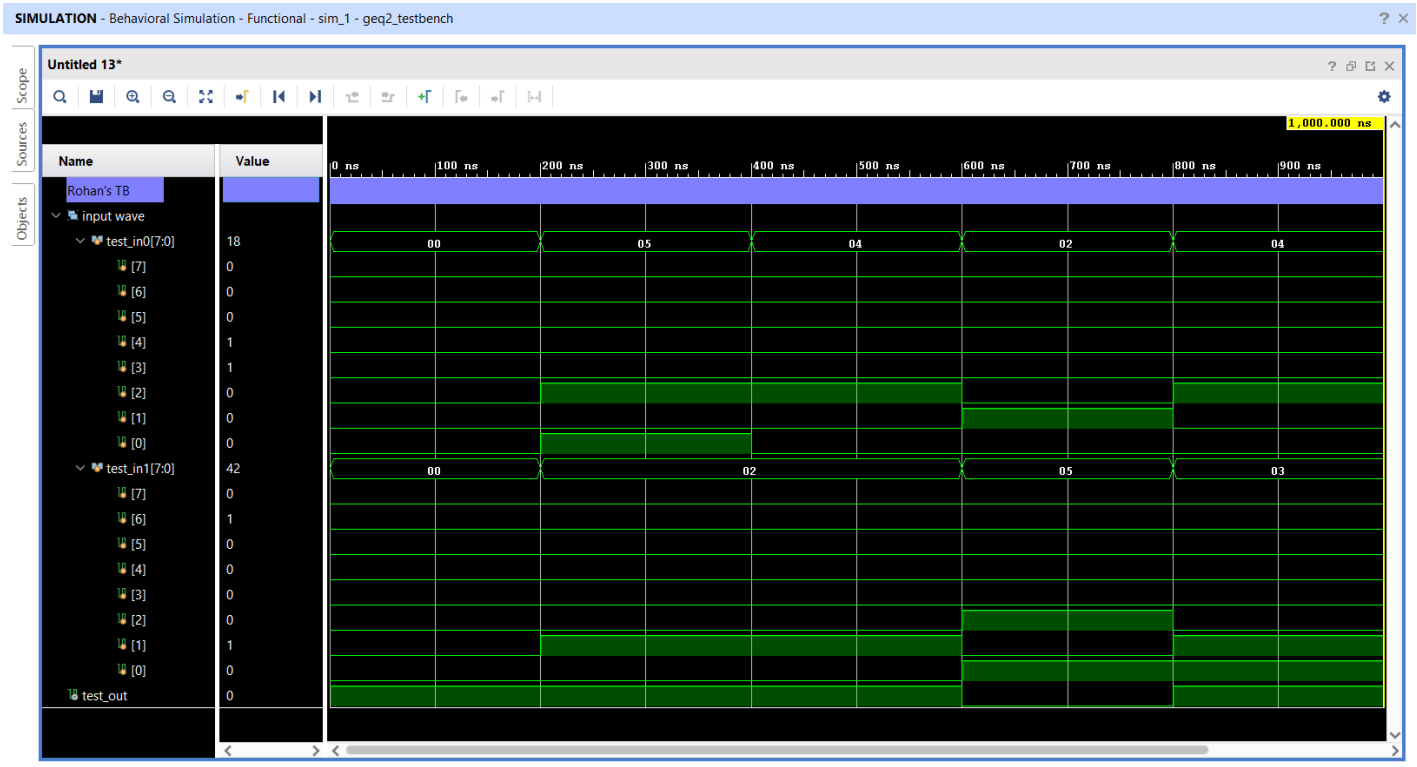

Figure 2.2. 8-bit comparator using 2-bit comparator module

The output waveform is for 8-bit comparator using 2-bit comparator module with additional support for misc. possible cases.