



Trinity College Dublin
Coláiste na Tríonóide, Baile Átha Cliath
The University of Dublin

3C7 DIGITAL SYSTEM DESIGN LABORATORY

Lab Session B

Department of Electronic and Electrical Engineering
(e-Report submission)



Lab:

1. 2-bit equal comparator
2. 8-bit gate-level greater-than-or-equal-to circuit

Submitted by:

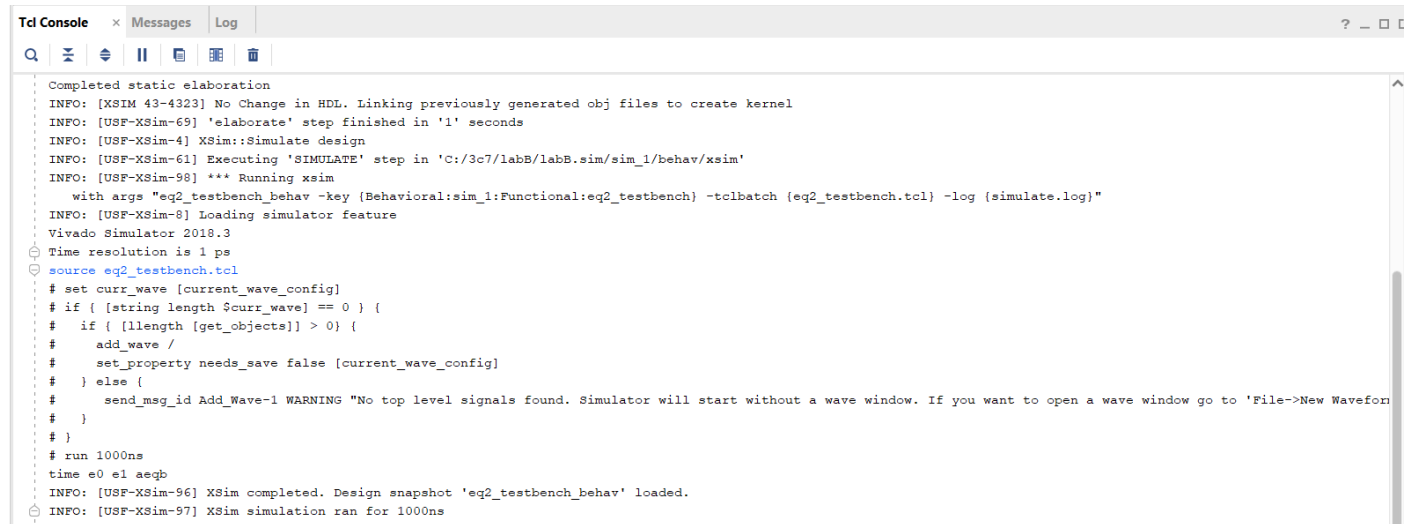
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Lab 1. 2-bit equal comparator

The given assignment starts with initialization of new project with the provided testbench and dependent modules. The provided module eq2 provided had following errors which were resolved.

After adding these design sources and making the fixes to module eq2, finally the behavioural simulation was started.



```
Tcl Console x Messages Log
Completed static elaboration
INFO: [XSIM 43-4323] No Change in HDL. Linking previously generated obj files to create kernel
INFO: [USF-XSim-69] 'elaborate' step finished in '1' seconds
INFO: [USF-XSim-4] XSim::Simulate design
INFO: [USF-XSim-61] Executing 'SIMULATE' step in 'C:/3c7/labB/labB.sim/sim_1/behav/xsim'
INFO: [USF-XSim-98] *** Running xsim
with args "eq2_testbench_behav -key {Behavioral:sim_1:Functional:eq2_testbench} -tclbatch {eq2_testbench.tcl} -log {simulate.log}"
INFO: [USF-XSim-8] Loading simulator feature
Vivado Simulator 2018.3
Time resolution is 1 ps
source eq2_testbench.tcl
# set curr_wave [current_wave_config]
# if { [string length $curr_wave] == 0 } {
#   if { [llength [get_objects]] > 0 } {
#     add_wave /
#     set_property needs_save false [current_wave_config]
#   } else {
#     send_msg_id Add_Wave-1 WARNING "No top level signals found. Simulator will start without a wave window. If you want to open a wave window go to 'File->New Waveform'"
#   }
# }
# run 1000ns
time e0 e1 aeqb
INFO: [USF-XSim-96] XSim completed. Design snapshot 'eq2_testbench_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
```

Figure 1.1. TCL Console

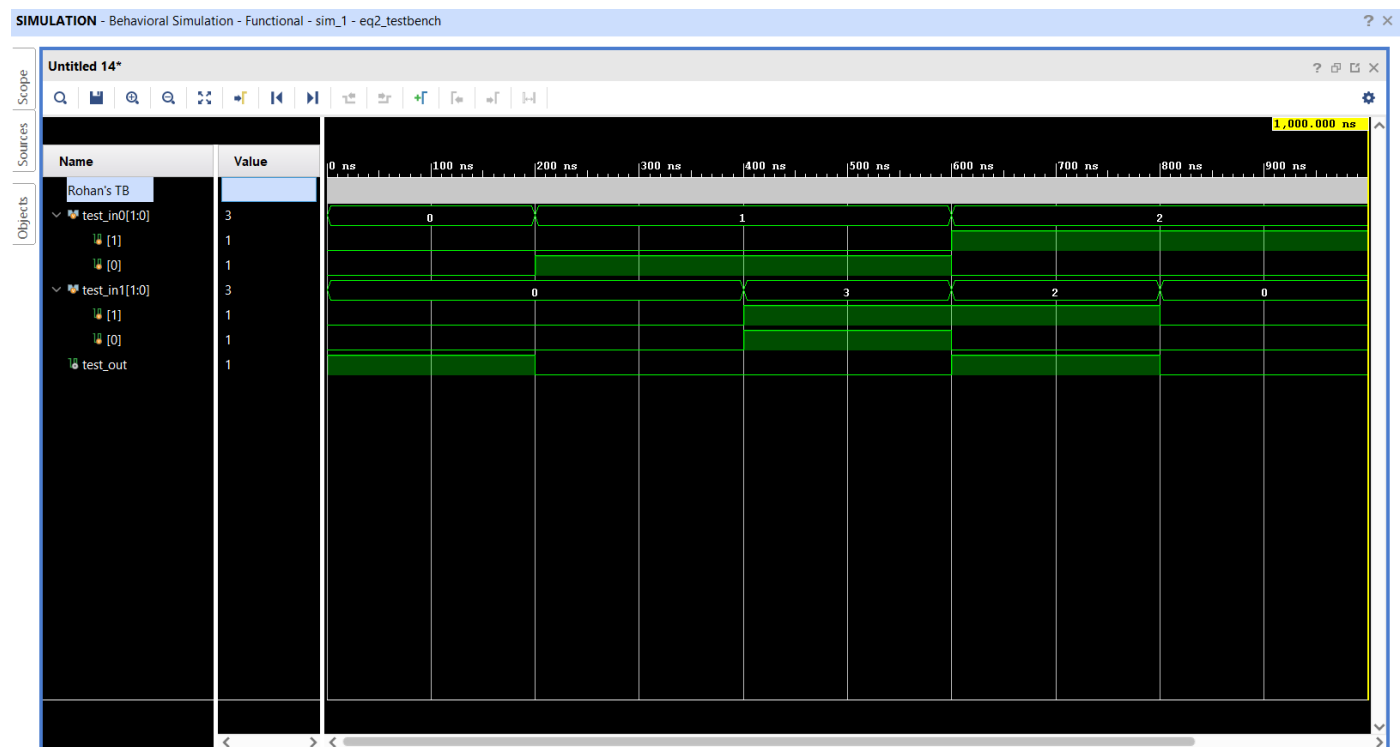


Figure 1.2. 2-bit comparator waveform

Lab 2. 8-bit gate-level greater-than-or-equal-to circuit

After modifying the Verilog coded module eq2 and eq1. It was made compatible to work for 2-bit greater than and equal.

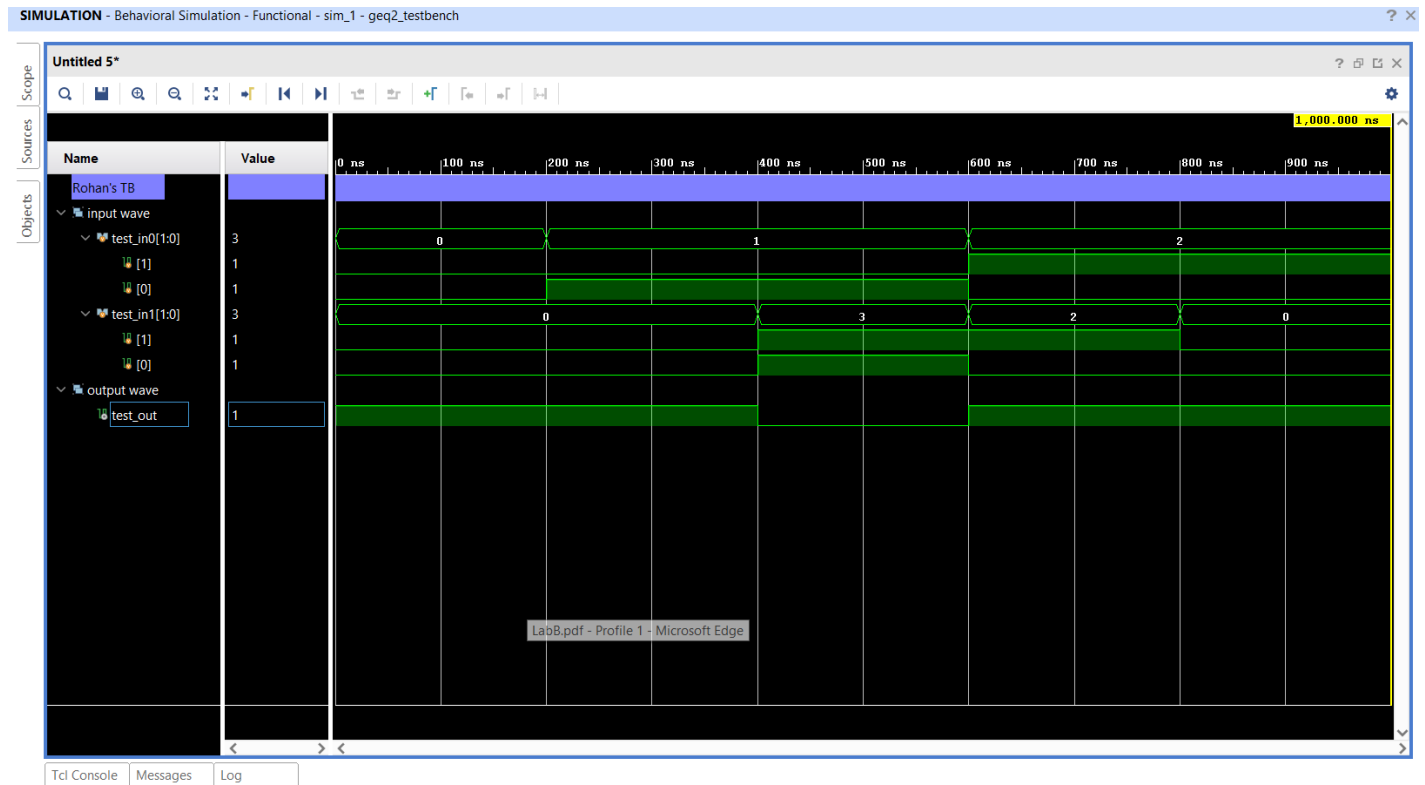


Figure 2.1. 2-bit comparator in bit0 greater than equal to bit1



Figure 2.2. 8-bit comparator using 2-bit comparator module

The output waveform is for 8-bit comparator using 2-bit comparator module with additional support for misc. possible cases.