

Qspice - Device Reference Guide by KSKelvin

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B. Behavioral Source

B. Behavioral Source : Instance Parameters

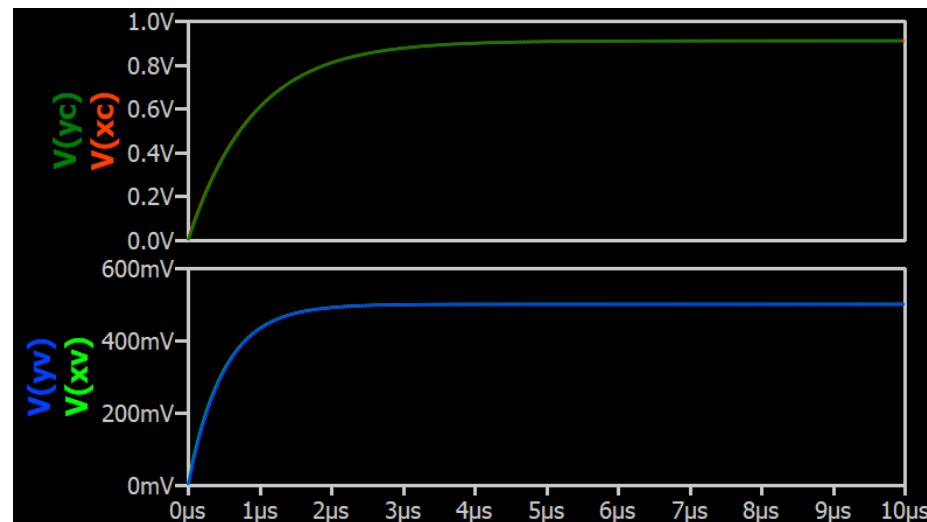
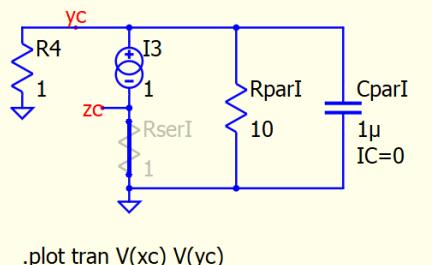
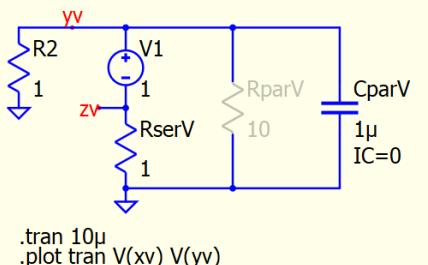
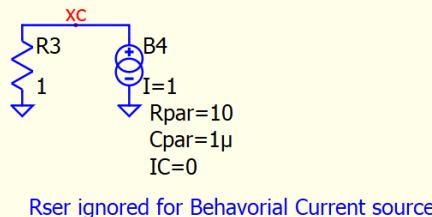
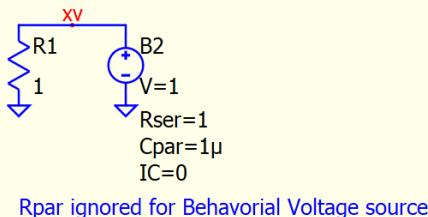
Behavioral Source Instance Parameters

Name	Description	Units	Default
CPAR	Parallel capacitance	F	0.0
I ¹	Expression for current	A	(not set)
IC	Initial value	A or V	0.0
LAPLACE	Frequency dependence		(none)
NORTON	Use a Norton equivalent for a behavioral resistance		(not set)
R ¹	Expression for resistance	Ω	(not set)
RPAR	Parallel resistance Ignore in V	Ω	Infinite
RSER	Series resistance Ignore in I and R (Norton)	Ω	0.0
SYNTHESIZE	Use the synthesized Laplacian circuit even for .AC		(not set)
THEVENIN	Use the Thévenin equivalent for a behavioral resistance		(not set)
V ¹	Expression for voltage	V	(not set)

B. Instance Params : Rser, Rpar and Cpar

Qspice : B Source - Rpar Rser Cpar in V and I.qsch

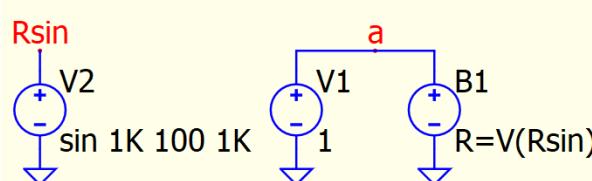
- Rser, Rpar and Cpar in Behavioral Voltage and Current Source
 - Behavioral Voltage ($V=<\text{expression}>$) : Only Rser and Cpar are active
 - Behavioral Current ($I=<\text{expression}>$) : Only Rpar and Cpar are active
 - I don't recommend to use Rser and Rpar in Behavioral Resistance as it will be very confusing depends on Norton or Thevenin equivalent
 - In this example, IC initial value is used to allow 0V or 0A for transient simulation. As behavioral source not have effect in .ac (except for Laplace), .tran is used to reveal these parameters characteristic



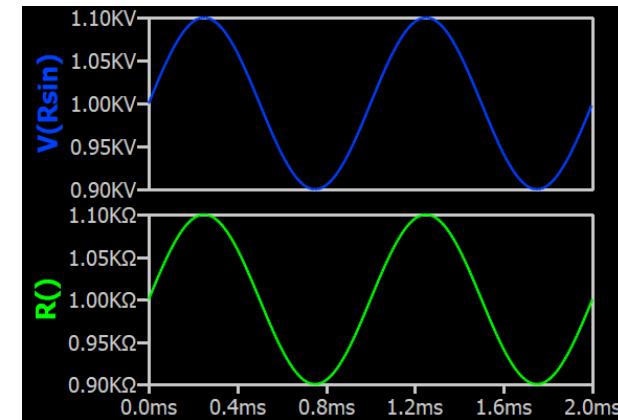
B. Instance Params : Behavioral Resistor

Qspice : B Source - Behavioral R.qsch

- Behavioral Resistor
 - Syntax : Bnnn n001 n002
 $R = <\text{expression}>$



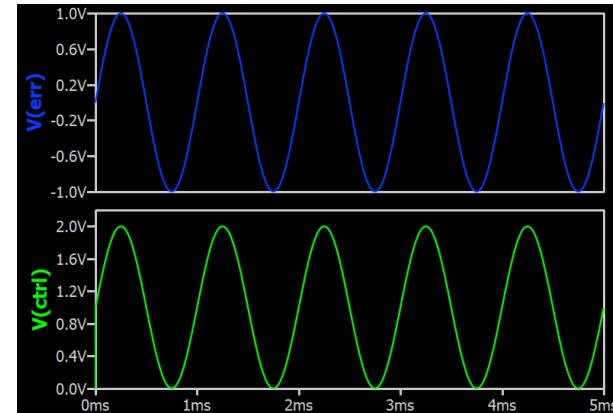
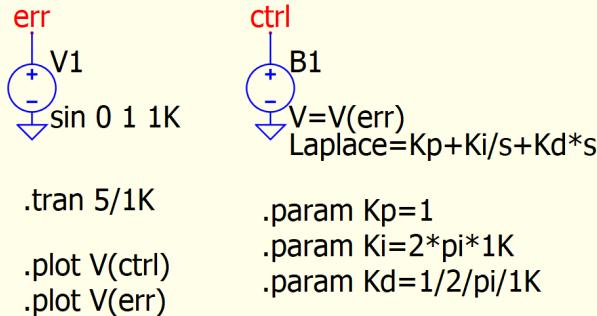
```
.tran 2m
.func R() V(a)/I(B1)
.plot R()
.plot V(Rsin)
```



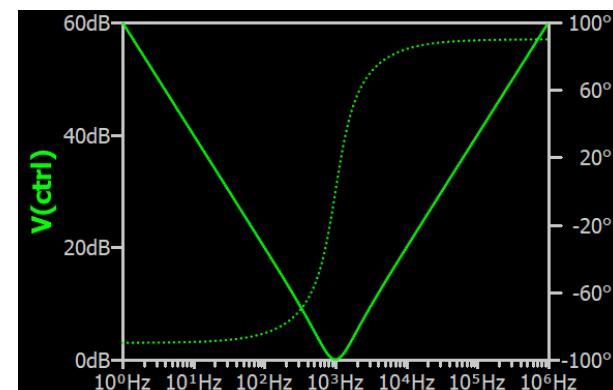
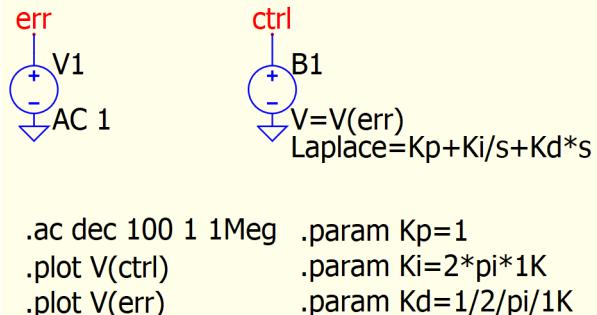
B. Instance Params : Laplace

Qspice : B Source - Laplace (.tran).qsch ; B Source - Laplace (.ac).qsch

- Laplace (.tran)
 - Use Laplace equation, by adding a new attribute Laplace
- In this simulation
 - $v_{ctrl} = \left(K_p + \frac{K_i}{s} + K_d s \right) v_{err}$



- Laplace (.ac)
 - Laplace supports .ac analysis



B. Function and Operators

HELP > Simulator > Device Reference > B. Behavioral Sources

Functions

Name	Description
abs(x)	Absolute value of x
acos(x)	arc cosine of x
arccos(x)	Synonym for acos()
acosh(x)	arc hyperbolic cosine of x
asin(x)	arc sine of x
arcsin(x)	Synonym for asin()
asinh(x)	Arc hyperbolic sine
atan(x)	Arc tangent of x
arctan(x)	Synonym for atan()
atan2(y,x)	Four quadrant arc tangent of y/x
atanh(x)	Arc hyperbolic tangent
buf(x)	1 if x > .5, else 0
ceil(x)	Integer equal or greater than x
cos(x)	Cosine of x
cosh(x)	Hyperbolic cosine of x
ddt(x)	Time derivative x
delay(x,y)	x delayed by y
delay(x,y,z)	x delayed by y, but store no more than z history
dlim(x,y,z)	x bounded by y which it asymptotically starts to approach at y+z as a first inverse order Laurent series
exp(x)	e to the x
floor(x)	Integer equal to or less than x
hypot(x,y)	$\sqrt{x^2 + y^2}$
idt(x,y,z)	Time integral of x with initial condition of y reset when z > .5 $\int x \, dtimes + y$

if(x,y,z)	If x > .5, then y else z
int(x)	Convert x to integer
inv(x)	0. if x > .5, else 1.
limit(x,y,z)	Intermediate value of x, y, and z
In(x)	Natural logarithm of x
log(x)	Alternate syntax for ln()
log10(x)	Base 10 logarithm
max(x,y)	The greater of x or y
min(x,y)	The smaller of x or y
pow(x,y)	x^y
pwr(x,y)	$ x ^y$
pwrs(x,y)	$abs(x)^y$ $sgn(x)*abs(x)^y$
random(x)	Random number from 0. to 1. depending on the integer value of x. Interpolation between random numbers is linear for non-integer x.
sin(x)	Sin x
sinh(x)	Hyperbolic sine of x
sqrt(x)	\sqrt{x}
table(x,a,b,c,d,...)	Interpolate x from the look-up table given as a set of pairs of constant values.
tan(x)	Tangent of x.
tanh(x)	Hyperbolic tangent of x
ulim(x,y,z)	x bounded by y which it asymptotically starts to approach at y-z as a first inverse order Laurent series

Operators grouped in reverse order of precedence of evaluation

Operand	Description
&	Boolean AND
	Boolean OR
>	True if expression on the left is greater than the expression on the right.
<	True if expression on the left is less than the expression on the right.
>=	True if expression on the left is greater than or equal the expression on the right.
<=	True if expression on the left is less than or equal the expression on the right.
+	Addition
-	Subtraction
*	Multiplication
/	Division
**	** / ^ Raise left hand side to power of right hand side. Same as '^'.
!	Boolean not the following expression.

Available Function in B source not listed

- Trunc(x) ; floor(x) ; int(x) : rounded down integer
- Rint(x) ; round(x) : rounded to nearest integer
- Ceil(x) : rounded up integer
- Ustep(x) : $x > 0 ? 1 : 0$
- Uramp(x) : $x > 0 ? x : 0$

Available Variable or Constant not listed in HELP

- Time : Simulation Time
- Temp : Temperature
- PI : 3.14159265358979323846
- E : 2.7182818284590452354
- K : 1.380649e-23 J/K
- Q : 1.602176487e-19 Coulomb

B. Function and Operators – delay(x,y) or delay(x,y,z)

Qspice : B Source - delay fix.qsch

- delay(x,y) or delay(x,y,z)
 - Delay(x,y,z) can reduce the amount of waveform memory that must be stored

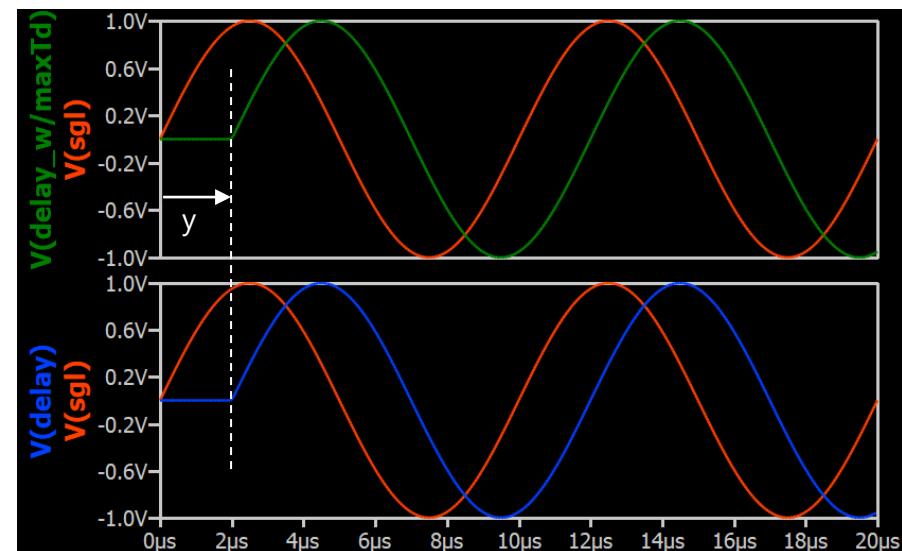
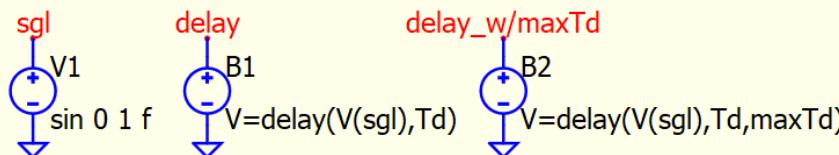
delay(x,y)	x delayed by y
delay(x,y,z) ¹	x delayed by y, but store no more than z history

- y can be parameter and z must be fixed constant
- y must less than z or error will return

Syntax : delay(x,y) - x delayed by y

Syntax : delay(x,y,z) - x delayed by y, but store no more than z history

```
.param f = 100K  
.param Td = 2μ  
.param maxTd = 5μ
```



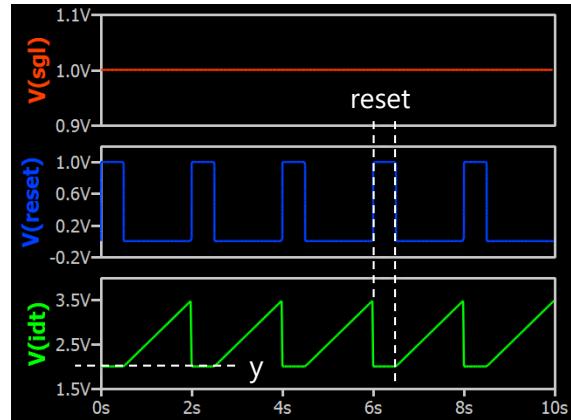
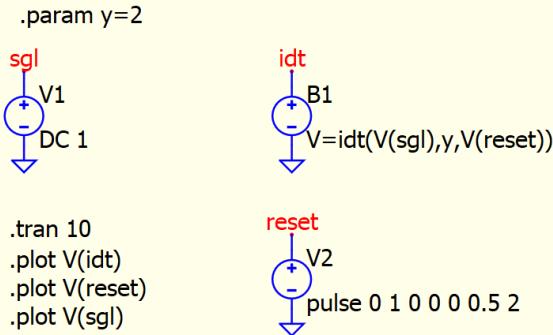
B. Function and Operators – Integral and Time Derivative idt(x,y,z) and ddt(x)

Qspice : B Source - idt.qsch ; B Source - ddt.qsch

- $\text{idt}(x,y,z)$

- Time Integral of x
- $= \int x dt + y$
- y is initial condition equivalent DC value during integral reset
- z is to reset integral

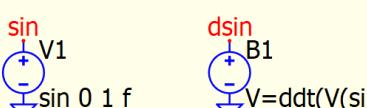
Syntax : $\text{idt}(x,y,z)$
Time integral of x with initial condition of y reset when z > .5



- $\text{ddt}(x)$

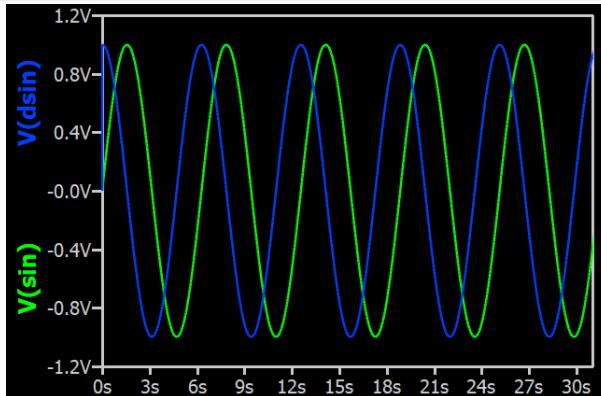
- Time derivative
- $= \frac{dx}{dt}$

Syntax : $\text{ddt}(x)$
Time derivative x



Formula
 $d(\sin(\omega t))/dt = \omega \cos(\omega t)$

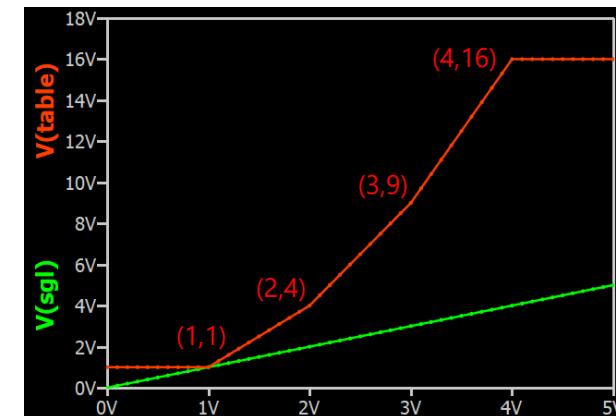
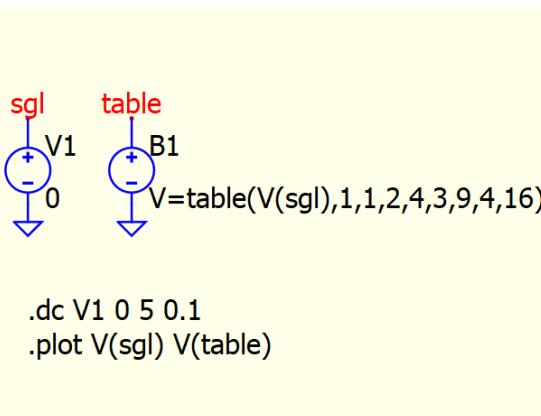
```
.param f=1/2/pi
.param omega=2*pi*f
.tran 5/f
.plot V(sin) V(dsin)
```



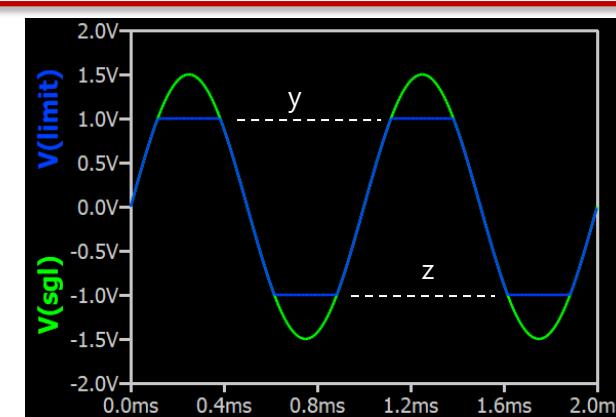
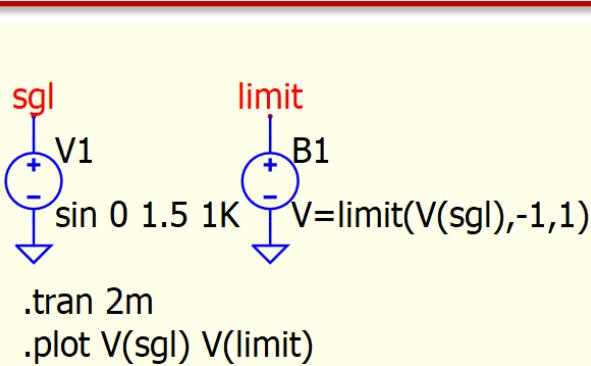
B. Function and Operators – $\text{table}(x,a,b,c,d,\dots)$ and $\text{limit}(x,y,z)$

Qspice : B Source - `table.qsch` ; B Source - `limit.qsch`

- $\text{Table}(x,a,b,c,d,\dots)$
 - Interpolate x from the look-up table given as a set of pairs of constant values



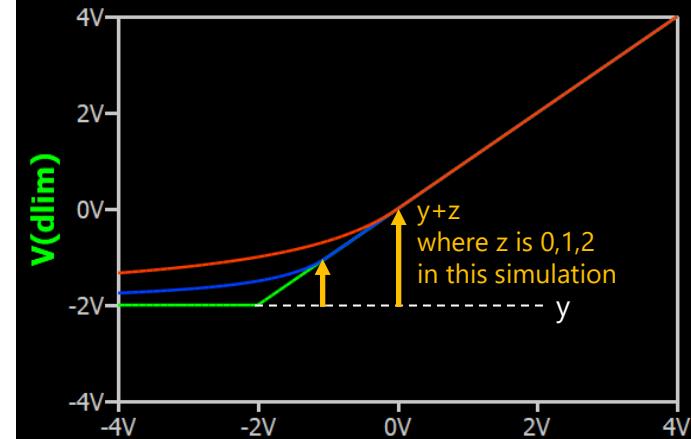
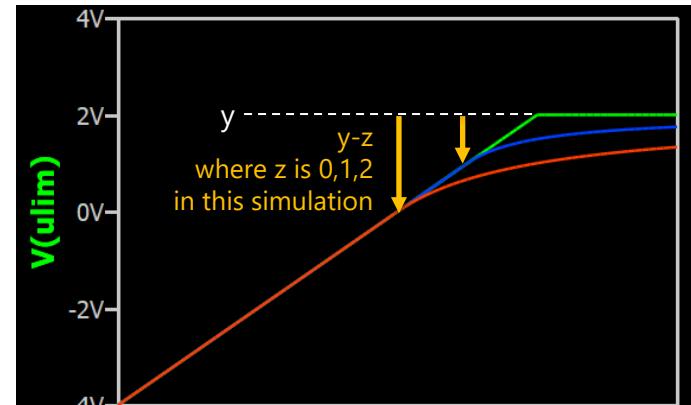
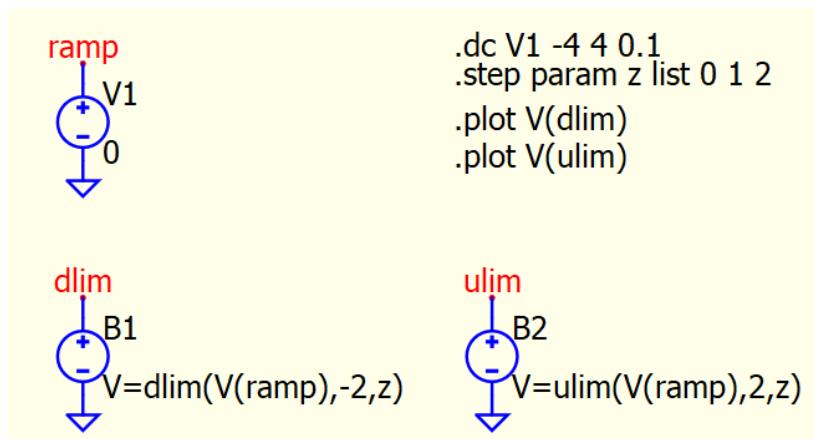
- $\text{limit}(x,y,z)$
 - Intermediate value of x, y, and z



B. Function and Operators – dlim(x,y,z) and ulim(x,y,z)

Qspice : B Source - dlim ulim.qsch

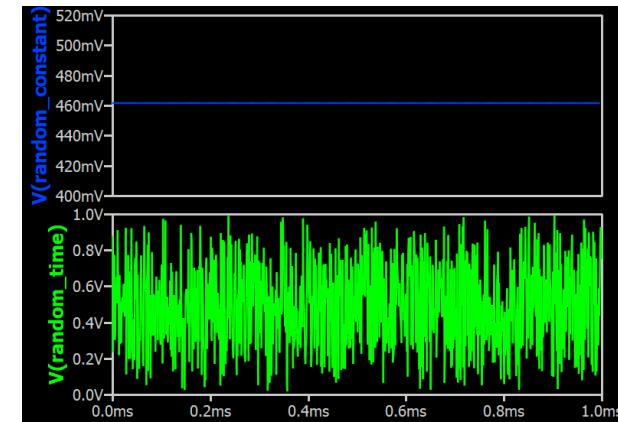
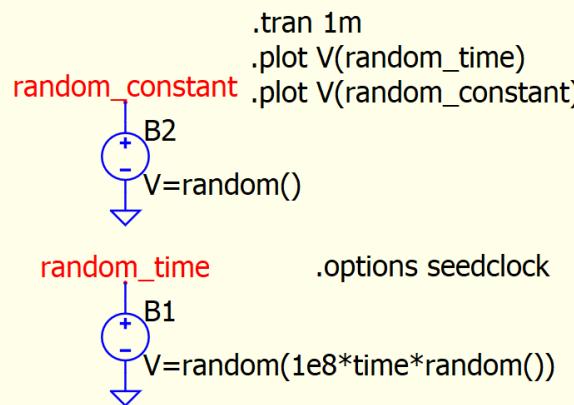
- dlim(x,y,z) and ulim(x,y,z)
 - dlim(x,y,z) : x bounded by y which it asymptotically starts to approach at $y+z$ as a first inverse order Laurent series
 - ulim(x,y,z) : x bounded by y which it asymptotically starts to approach at $y-z$ as a first inverse order Laurent series
 - These functions are used for soft limit



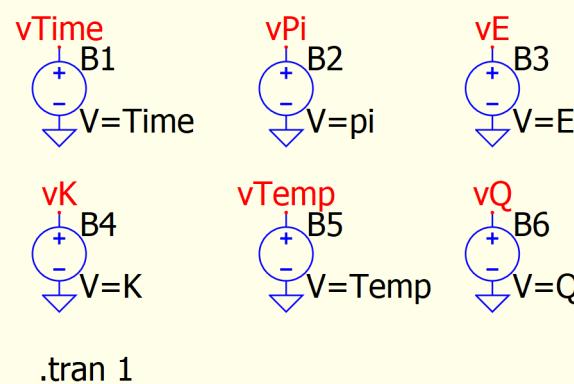
B. Function and Operators – random(x), variable/constant

Qspice : B Source – random.qsch ; B Source - Buildin Variable Constant.qsch

- Random(x)
 - Random number from 0. to 1. depending on the integer value of x
 - The one without arguments must be processed in the preprocessor (explained by Mike Engelhardt)
 - To create a random sequence in transient, x must change in each time step : i.e. random(1e8*time), multiple with 1e8 is for x to be a large integer for random generation



- Build-in Variable / Constant
 - Time : Simulation Time
 - Temp : Temperature
 - PI : 3.14159265358979323846
 - E : 2.7182818284590452354
 - K : 1.380649e-23 J/°K
 - Q : 1.602176487e-19 Coulomb



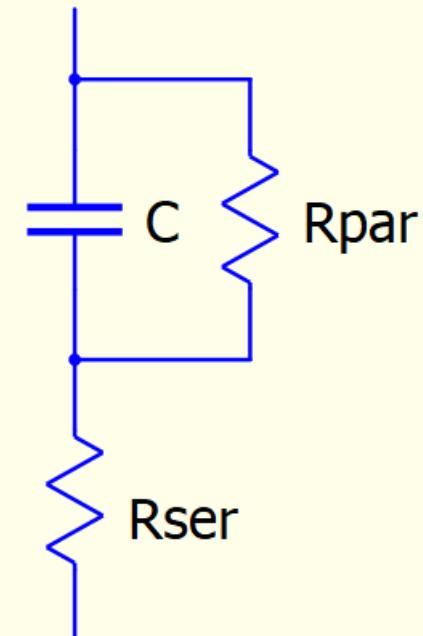
C. Capacitor

Capacitor C Instance Parameters in Qspice HELP

Rpar and Rser in C model

Capacitor Instance Parameters

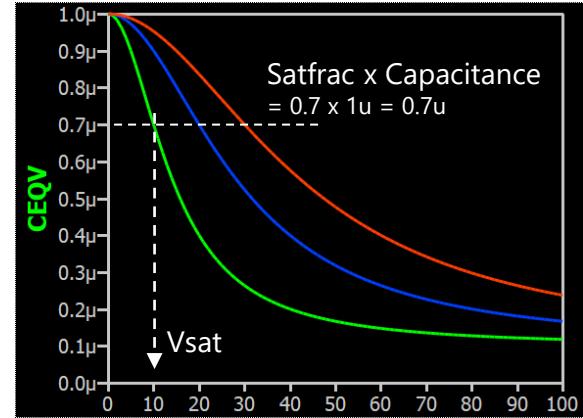
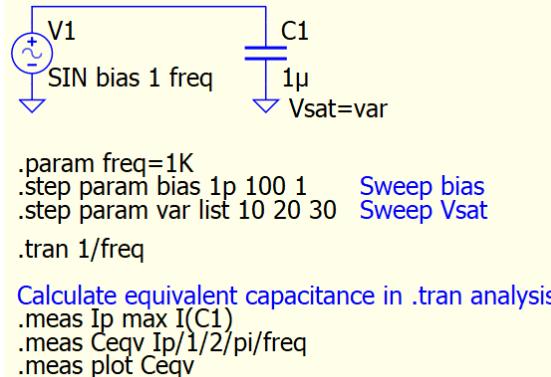
Name	Description	Units	Default
CAPACITANCE	Capacitance(not usually labeled)	F	0.0
CSAT	Capacitance asymptotically approached in saturation	F	10% of CAPACITANCE
IC	Initial voltage on capacitor	V	0.0
L ¹	Length	m	0.0
M	Number of identical parallel devices		1.0
RPAR	Equivalent parallel resistance	Ω	Infinite
RSER	Equivalent series resistance	Ω	0.0
SATFRAC	Fractional drop in capacitance at VSAT		0.7
TEMP	Instance temperature	$^{\circ}\text{C}$	Circuit temperature
VSAT	Voltage that drops capacitance to SATFRAC×CAPACITANCE	V	Infinite
W ¹	Width	m	0.0



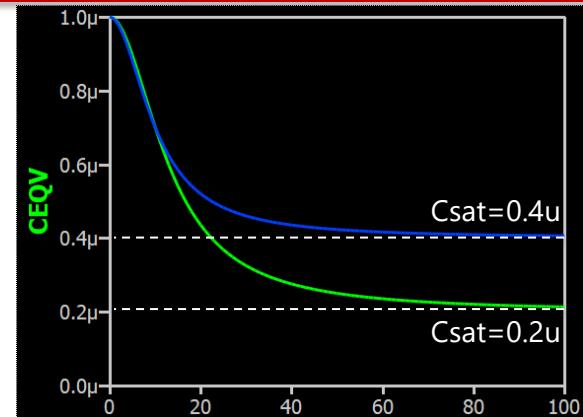
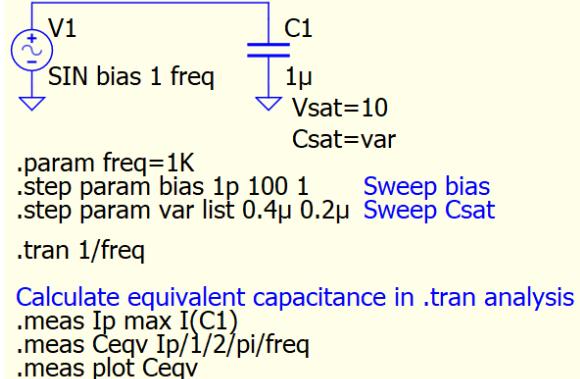
C. Instance Params : Vsat, Csat, Satfrac : For Nonlinear Capacitance

Qspice : C Capacitor - Vsat (.ac).qsch ; C Capacitor - Csat (.tran).qsch

- Vsat and Satfrac
 - **Vsat** : Voltage that drops capacitance to **Satfrac x Capacitance**
 - **Satfrac** : Fractional drop in capacitance at Vsat
 - default = 0.7



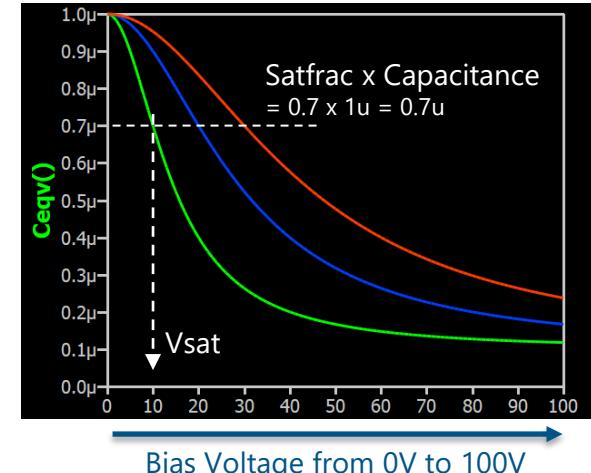
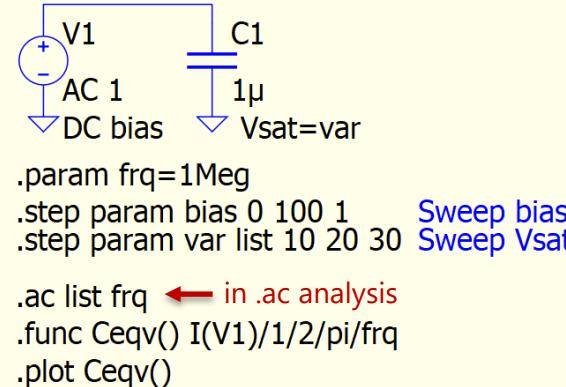
- Csat
 - **Csat** : Capacitance asymptotically approached in saturation
 - ** Vsat must be set to see its effect



C. Instance Params : Replicate previous graph with .ac analysis

Qspice : C Capacitor - Vsat (.ac).qsch

- Vsat and Satfrac
 - **Vsat** : Voltage that drops capacitance to **Satfrac x Capacitance**
 - **Satfrac** : Fractional drop in capacitance at Vsat
 - default = 0.7

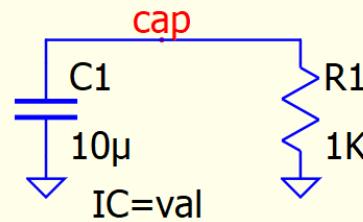


- Capacitance equation
 - $X_C = \frac{1}{\omega C} = \frac{V_c}{I_c}$
 - $C = \frac{|I_c|}{|V_c| \omega} = \frac{|I_c|}{2\pi f |V_c|}$
 - This formula is used to calculate equivalent capacitance (small signal model) at different capacitor bias voltage

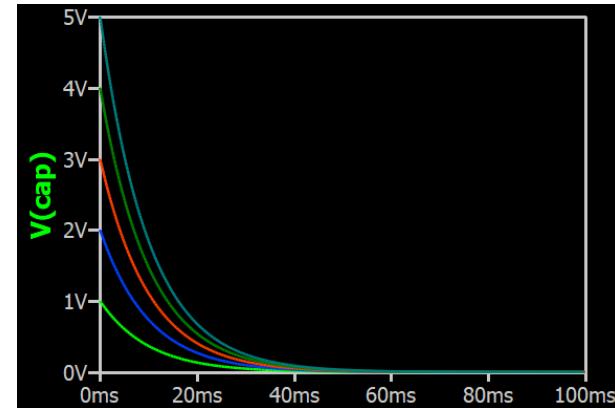
C. Instance Params : IC Initial Condition

Qspice : Capacitor - IC.qsch

- IC
 - IC : Initial Condition
 - **Default IC=0**
 - Use in transient analysis for initial voltage of capacitor at time=0s



```
.step param val 1 5 1  
.tran 100m  
.plot V(cap)
```



D. Diode

Behavioral Diode Model Parameters

Behavioral Diode Model Parameters in Qspice HELP

QSPICE includes a simplified, behavioral, diode. To use those device equations, specify a non-zero RON.

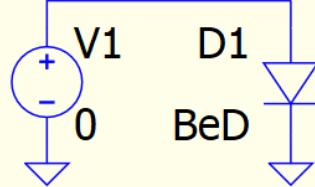
Behavioral Diode Model Parameters

Name	Description	Units	Default
RON	Forward on resistance	Ω	0.0^3
ROFF	Off resistance	Ω	$1./GMIN$
RZEN	Breakdown resistance(aka RREV)	Ω	RON
VFWD	Forward voltage drop	V	0.0
VREV	Reverse voltage drop	V	0.0
EPSILON	Width of quadratic region splining off and on regions	V	0.0
REVEPSILON	Width of quadratic region splining breakdown and on regions	V	0.0
CJO	Shunt capacitance	F	0.0

^{3]} The value of zero means don't use these equations, but the conventional SPICE semiconductor diode equations.

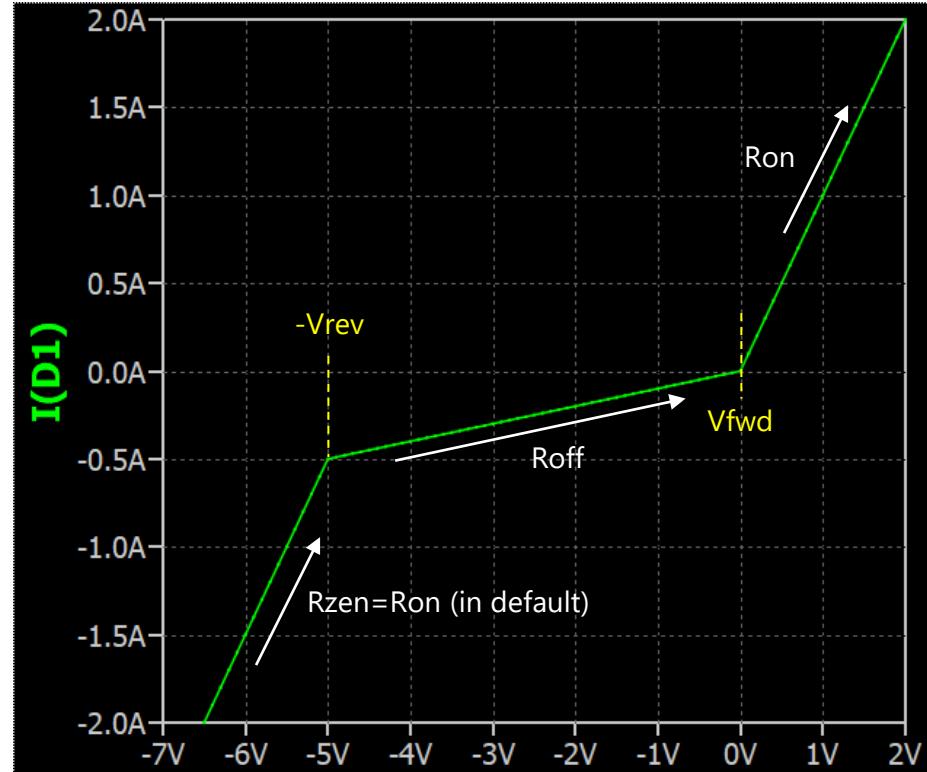
Behavioral Diode Model Params : Ron, Roff, Vfwd, Vrev

Qspice : Behavioral Diode Model - Ron Roff Vfwd Vrev.qsch



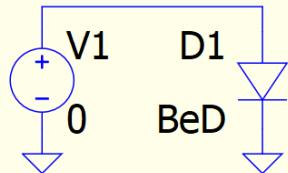
```
.model BeD D Ron=1 Roff=10 Vfwd=0 Vrev=5  
+ Epsilon=0 Revepsilon=0
```

```
.dc V1 -7 2 0.1  
.plot I(D1)
```



Behavioral Diode Model Params : Rzen, Epsilon, Revepsilon

Qspice : Behavioral Diode Model - Epsilon Revepsilon Rzen.qsch



```
.model BeD D Ron=1 Roff=10Meg Vfwd=0 Vrev=5  
+ Epsilon={val} Revepsilon={val} Rzen=0.5
```

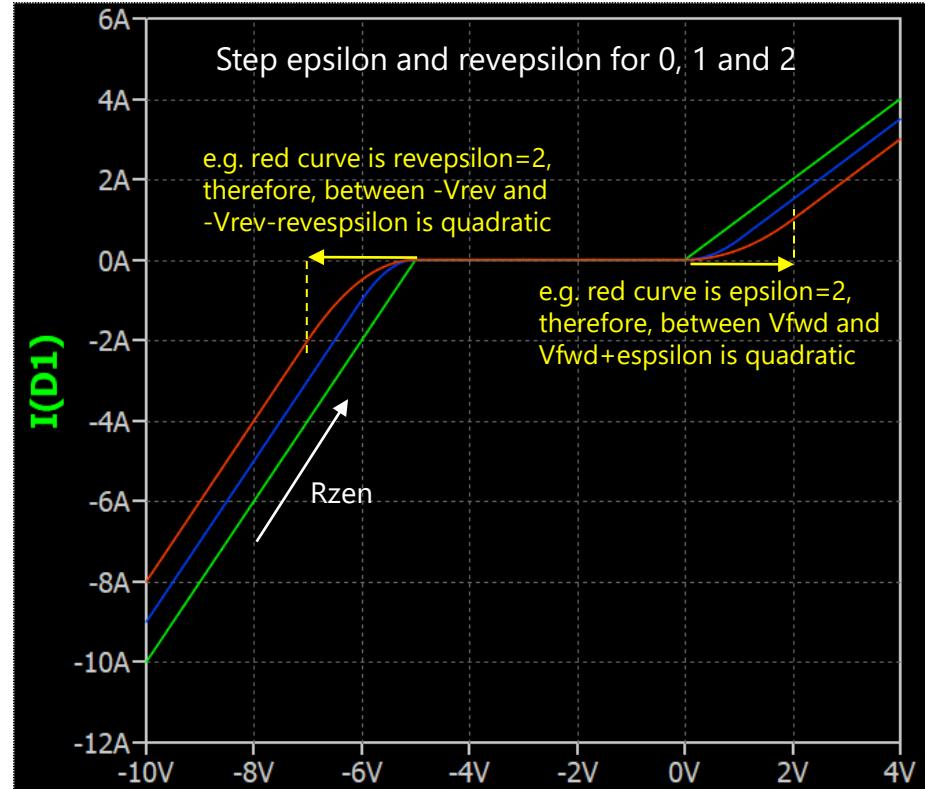
```
.dc V1 -10 4 0.1
```

```
.plot I(D1)
```

```
.param val=0
```

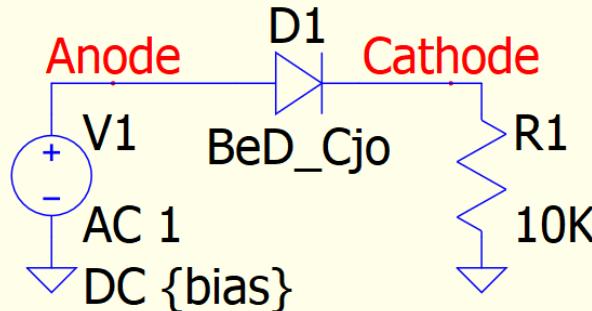
```
.step param val 0 2 1
```

* Roff change to 10Meg in this study



Behavioral Diode Model Params : Cjo

Qspice : Behavioral Diode Model - Cjo.qsch



```
.param bias = 0
```

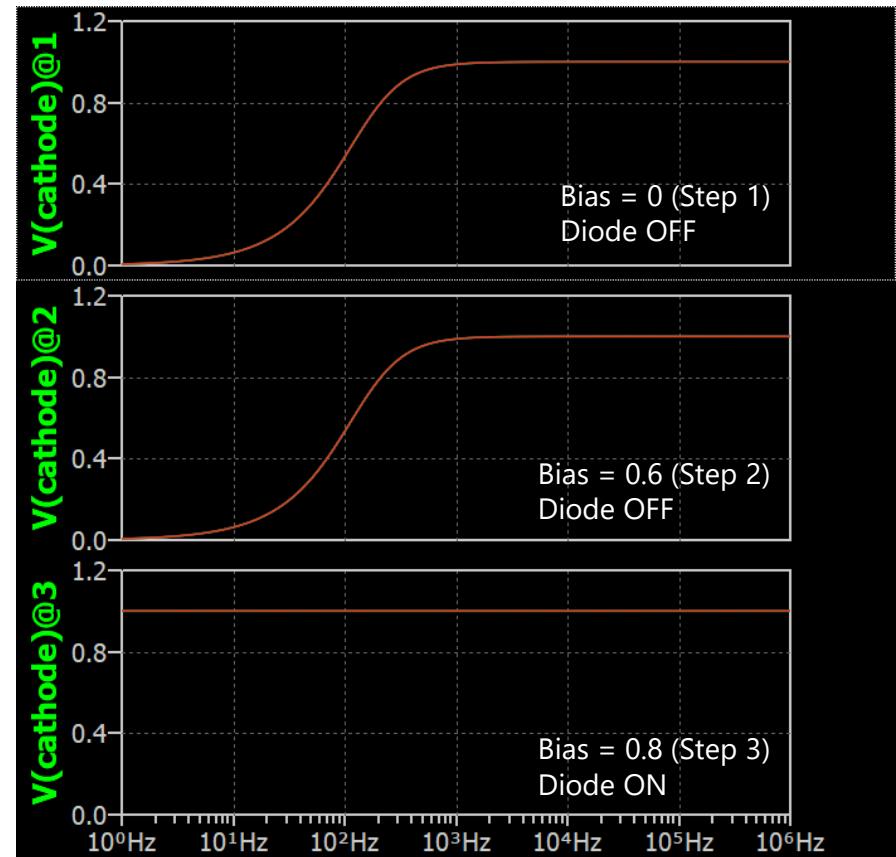
```
.model BeD_Cjo D Ron=1m Roff=1Meg
```

```
+ Vfwd=0.7 Cjo=100n
```

Cjo is equivalent to a capacitor parallel the behavioral diode

```
.ac dec 100 1 1Meg
```

```
.step param bias list 0 0.6 0.8
```

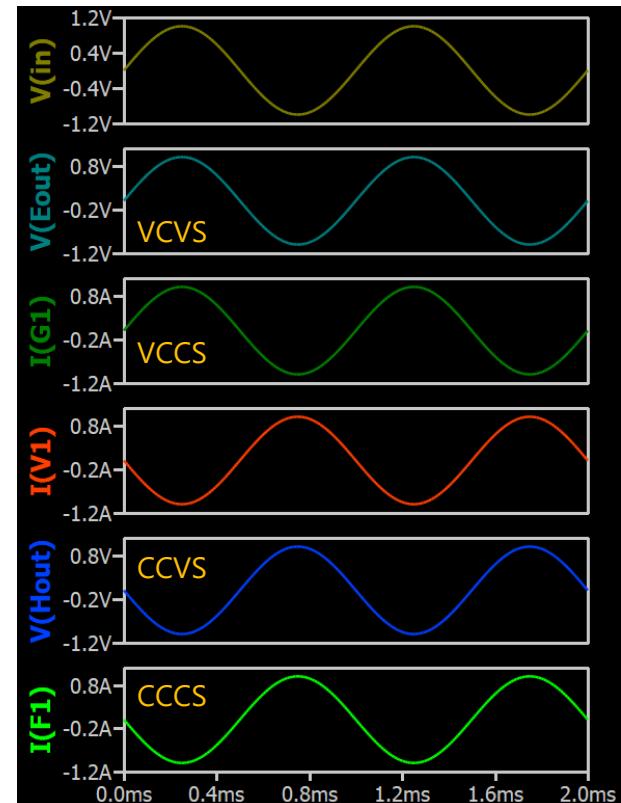
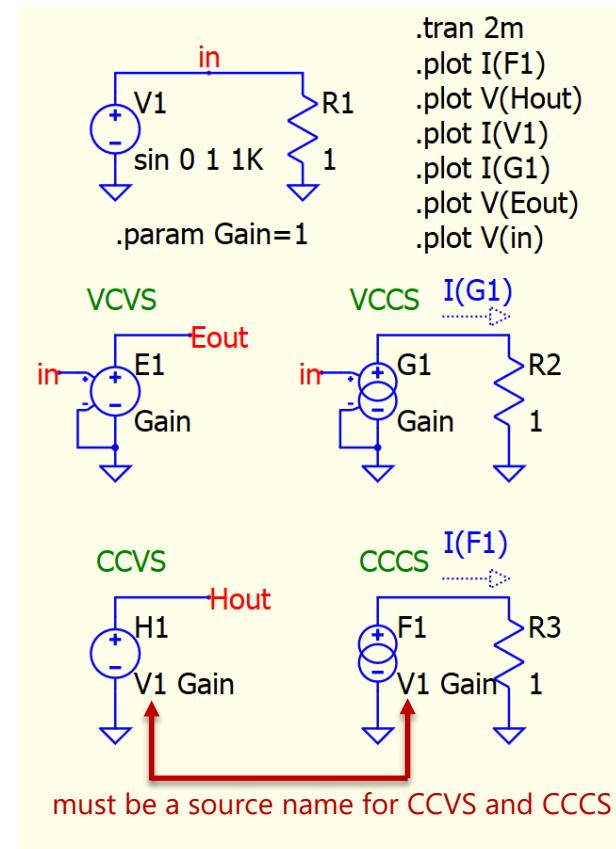


E. F. G. H. Dependent Sources

E. F. G. H. Dependent Sources

Qspice : Dependent Source - Basic.qsch

- Dependent Sources
 - [E] VCVS : Voltage Dependent Voltage Source
 - [G] VCCS : Voltage Dependent Current Source
 - [H] CCVS : Current Dependent Voltage Source
 - [F] CCCS : Current Dependent Current Source



I. Current Source

I. Current Source : Instance Parameters

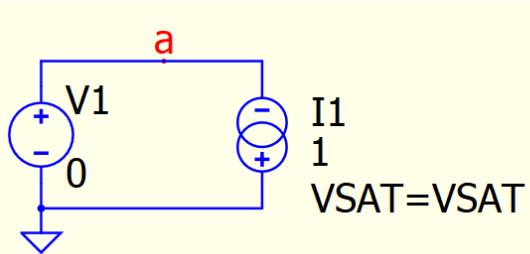
Current Source Instance Parameters

Name	Description	Units	Default
AC	AC magnitude, optionally followed by phase angle	A, °	0.
ACMAG	AC magnitude	A	0.
ACPHASE	AC phase	°	0.
DC	DC value of source	A	0.
EXP	Exponential source description		
LOG	Interpolate between PWL and CHIRP points		(not set)
PULSE	Pulse description		
PWL	Piecewise linear description		
SFFM	Single frequency FM description		
SINE	Sinusoidal source description(aka SIN)		
TIMECTRL	Time step control, one of NONE, LIMITS ¹ , BREAKS ² , or BOTH	String	LIMITS
VSAT ³	Don't source power(example)	V	0.
VSAT2	Don't source power and don't conduct in reverse	V	0.
XTRAP	Extrapolate beyond PWL and CHIRP points		(not set)

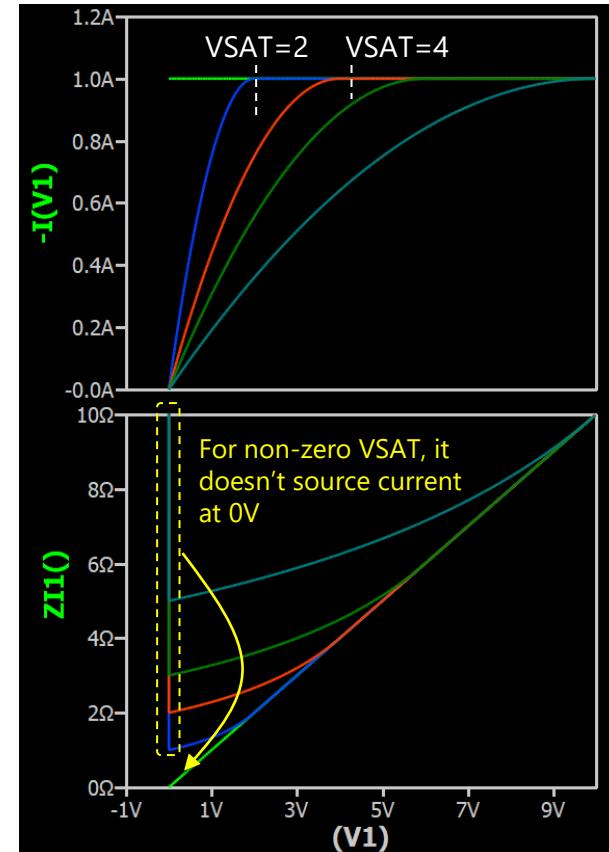
I. Instance Params : VSAT

Qspice : I Source - VSAT.qsch

- VSAT
 - VSAT : Don't source power
 - Characteristic
 - Only source current when $V(-ve,+ve) > VSAT$
 - Current source doesn't source current at $V(-ve,+ve)=0$
 - Equivalent to Open
 - Not to apply negative voltage between $V(-ve,+ve)$ as it will have current flow out from -ve
 - Usage
 - Useful for modeling an active load or a bias current in a macromodel



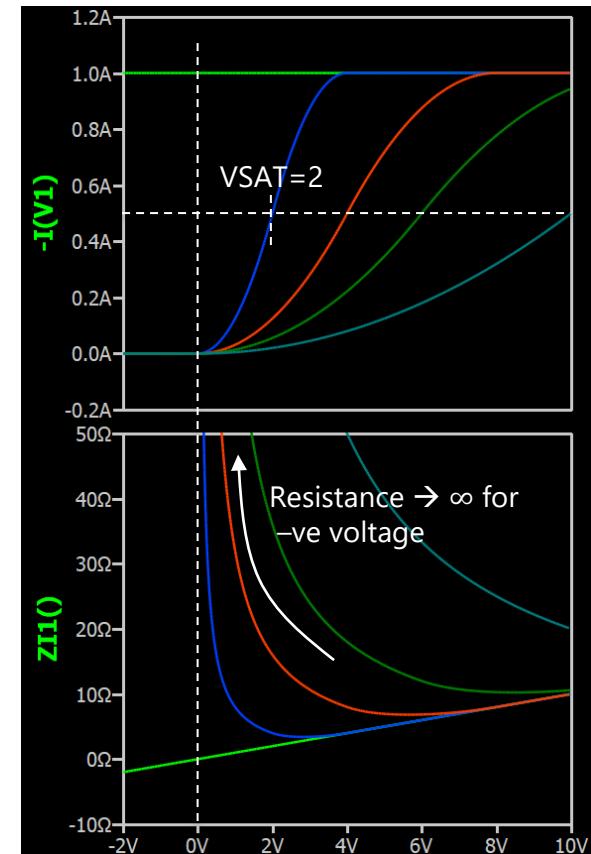
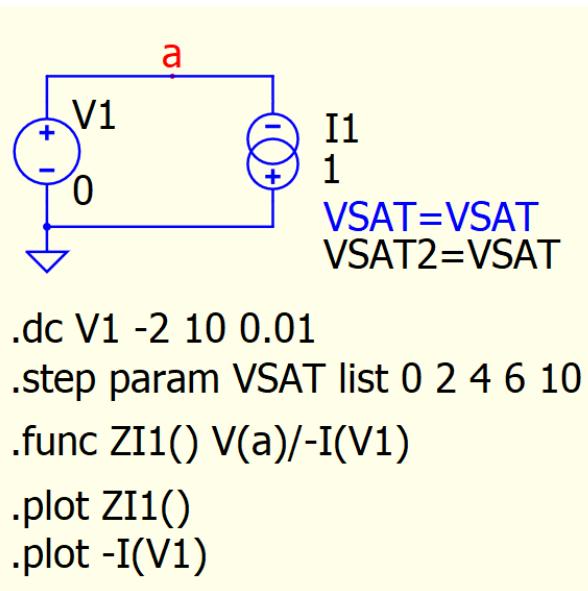
```
.dc V1 0 10 0.1  
.step param VSAT list 0 2 4 6 10  
.func ZI1() V(a)/-I(V1)  
.plot ZI1()  
.plot -I(V1)
```



I. Instance Params : VSAT2

Qspice : I Source - VSAT2.qsch

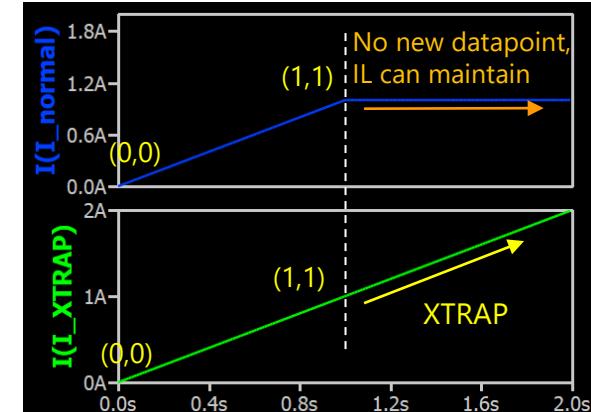
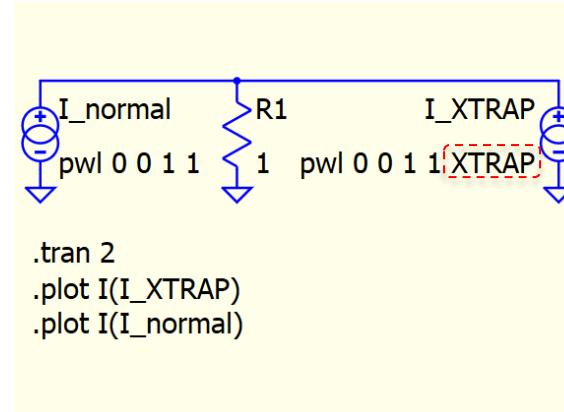
- VSAT2
 - VSAT2 : Don't source power and don't conduct in reverse
 - If VSAT2 is used, VSAT will be override



I. Instance Params : XTRAP

Qspice : I Source - XTRAP.qsch

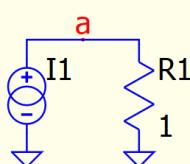
- XTRAP
 - Extrapolate beyond PWL and CHIRP points
 - Without XTRAP, for times after the last time, the current is the last current.



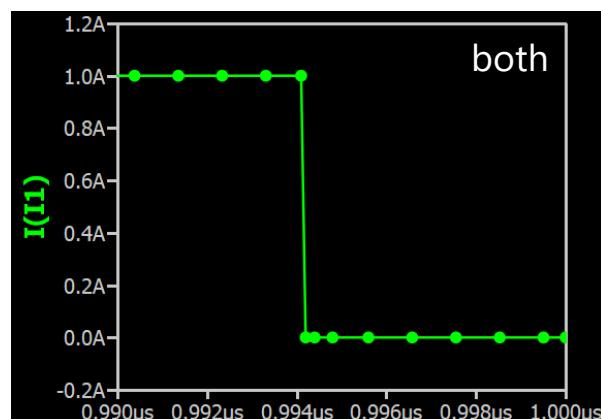
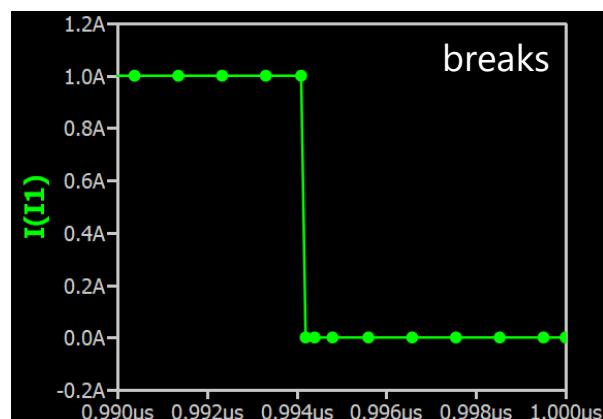
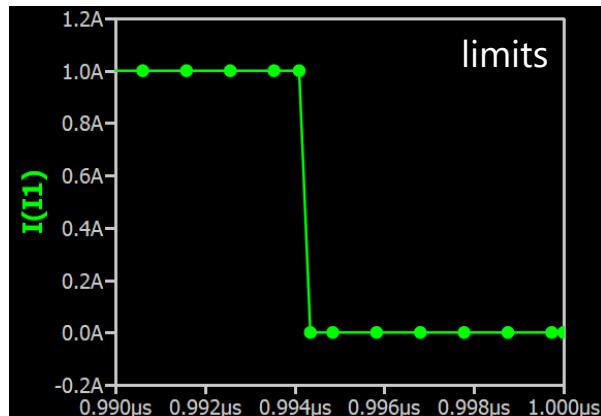
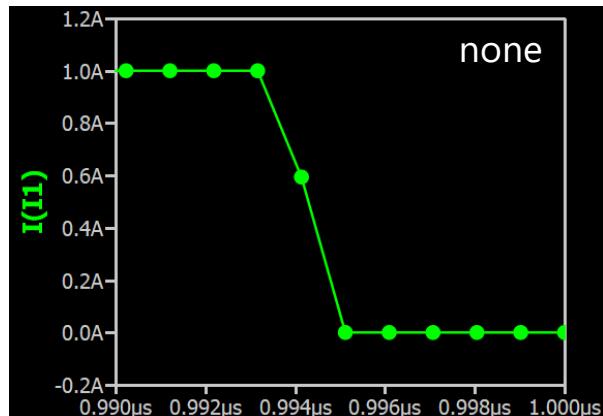
I. Instance Params : Timectrl

Qspice : I Source - TIMECTRL.qsch

- TIMECTRL
 - Timectrl : Time step control
 - None
 - Limits
 - Breaks
 - Both
 - **Default Timectrl=Limits**



```
pulse 0 1 4n 0 0 10n 20n  
Timectrl=none  
Timectrl=limits  
Timectrl=breaks  
Timectrl=both  
.tran 1000n  
.plot I(I1) I(I2)
```



K. Mutual Inductance

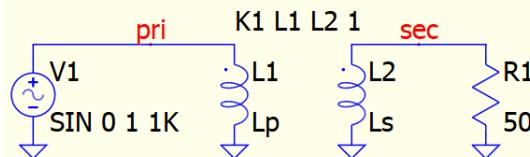
K. Mutual Inductance

Qspice : K Mutual - Two Winding.qsch / K Mutual - Three Winding.qsch

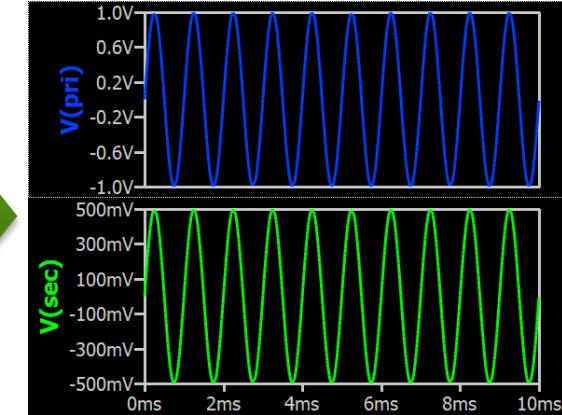
- K Mutual Inductance
 - K is coupling coefficient of coupled inductors
 - Ideal coupling : 1
 - Range : -1 to 1
 - Two or more coupled inductors are required
 - Press L two times to get symbol with a dot notation (not necessary, but recommend for current direction)

- Inductors as Transformer
 - $\frac{L_p}{N_p^2} = \frac{L_s}{N_s^2}$ and $n = \frac{N_p}{N_s}$
 - N is number of turns
 - $L_p = n^2 L_s$ or $L_s = \frac{1}{n^2} L_p$
 - In practice, L_p is measured from primary with secondary open

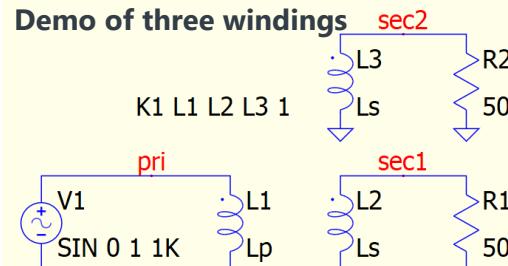
Demo of two windings



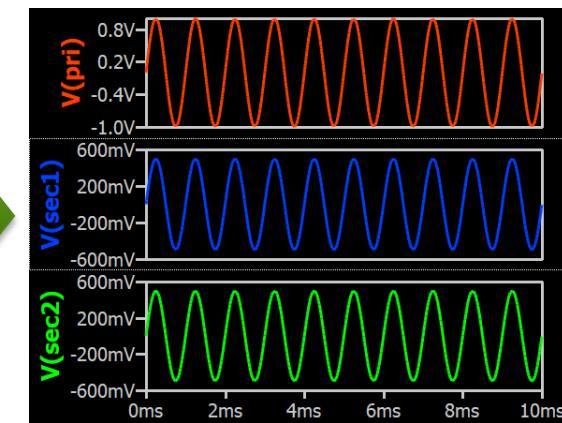
```
.tran 10/1K  
.plot V(pri)  
.plot V(sec)  
.param n=2  
.param Lp=100μ  
.param Ls=Lp/n**2
```



Demo of three windings



```
.tran 10/1K  
.plot V(pri)  
.plot V(sec1)  
.plot V(sec2)  
.param n=2  
.param Lp=100μ  
.param Ls=Lp/n**2
```



L. Inductor

Inductor L Instance Parameters in Qspice HELP

Inductor Instance Parameters

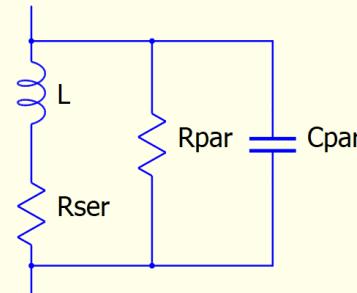
Name	Description	Units	Default
AG	Wire or stripline is made of gold		
AL	Wire or stripline is made of aluminum		see below
AU	Wire or stripline is made of silver		
BEND	Fractional inductance correction for wire bend or proximity effects		1.
CPAR	Parallel capacitance	F	0.
CU	Wire or stripline is made of copper		see below
DIAMETER	Diameter of wire or air coil	m	
FREQUENCY	Frequency at Q. Also used to compute Rser due to skin effect		
HEIGHT	Height of PCB stripline above ground plane	m	
IC	Initial current if uic is specified on .tran statement	A	none
INDUCTANCE	Inductance of inductor	H	0.0
ISAT	Current causing inductance to drop to SATFRAC×INDUCTANCE	A	Infinite
LENGTH	Length of wire, stripline, or air coil	m	
LSAT	Inductance asymptotically approached in saturation	H	10% of INDUCTANCE
M	Number of parallel inductors		1.0
NI	Wire is made of nickel		
Q	Quality factor at FREQUENCY		
RPAR	Equivalent parallel resistance	Ω	Infinite
RSER	Equivalent series resistance	Ω	0.0
SATFRAC	Fractional drop in inductance at ISAT		0.7
THICK	Thickness of stripline on top of a PCB	m	0.0
TURNS	Number of turns of an air coil		
VERBOSE	Print wire L, Rser, Rpar results on the console		(not set)
WIDTH	Width of stripline on top of a PCB	m	

Arbitrary Inductance Device

QSPICE also supports an arbitrary inductance device. To use it, give an equation for the flux due to the inductor. The equation can include any circuit node voltages or device currents of devices modeled as Thévenin equivalents(V-, L-, E-, or H-devices). In the interest of completeness, the device supports transinductance.

Syntax: Cnnn N1 N2 Q=<expression> [additional instance parameters]

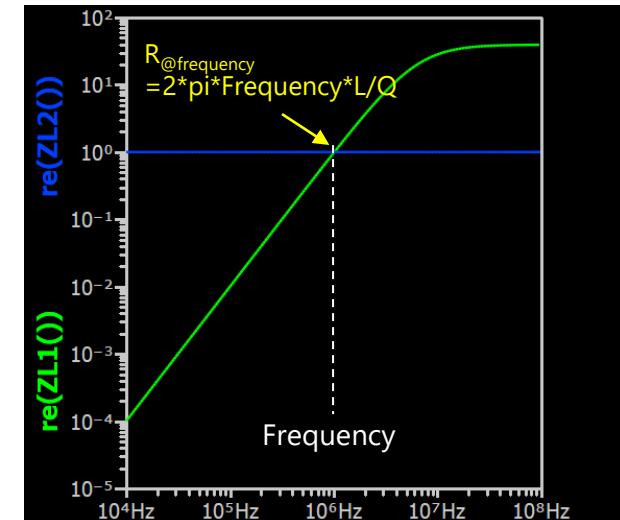
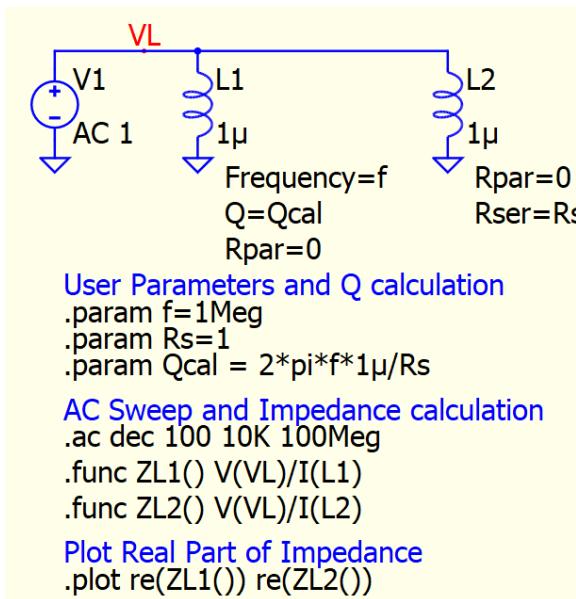
Name	Description	Units	Default
FLUX	Equation of flux(aka F)	Weber	
IC	Initial flux due to the inductor	Weber	
M	Number of identical parallel devices		1.0
RPAR	Equivalent parallel resistance	Ω	Infinite
RSER	Equivalent series resistance	Ω	0.0
NOISELESS	Ignore the noise contribution from RPAR and RSER		not set
TEMP	Instance temperature	°C	Circuit temperature



L. Instance Params : Frequency and Q

Qspice : Inductor - Frequency Q.qsch

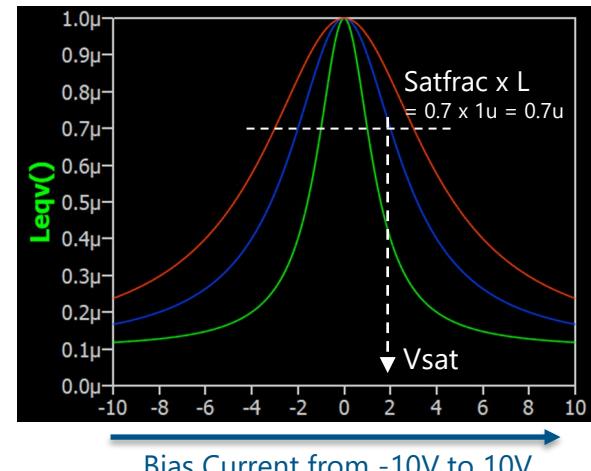
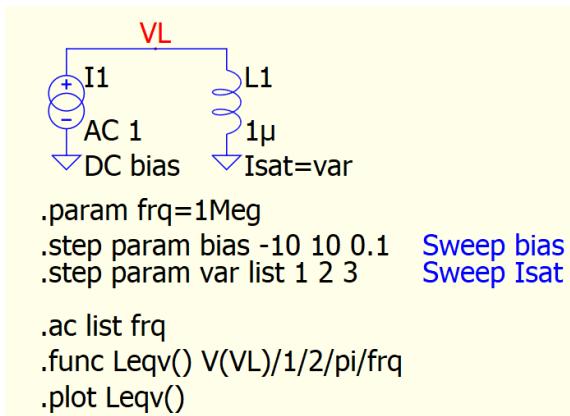
- Frequency and Q
 - Frequency : Frequency at Q
 - Also used to compute Rser due to skin effect
 - Q : Quality factor at FREQUENCY
- Formula
 - $Q = \frac{X_L}{R} = \frac{2\pi f L}{R_{@f}}$
 - Using Frequency and Q is not same as using Rser modeling
 - Rser is a constant over frequency but Frequency/Q pair give Rser with skin effect



L. Instance Params : Isat, Lsat, Satfrac : For Nonlinear Inductance

Qspice : L Inductor (AC) - Vsat.qsch

- **Isat** and **Satfrac**
 - **Isat** : Current that drops inductance to **Satfrac x Inductance**
 - **Satfrac** : Fractional drop in inductance at Isat
 - default = 0.7
 - Nonlinear effect is valid in +ve and -ve current direction

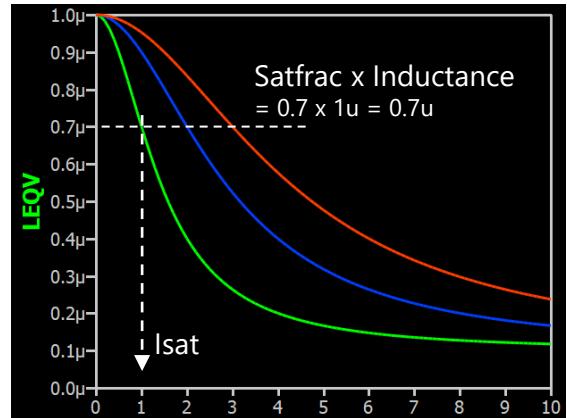
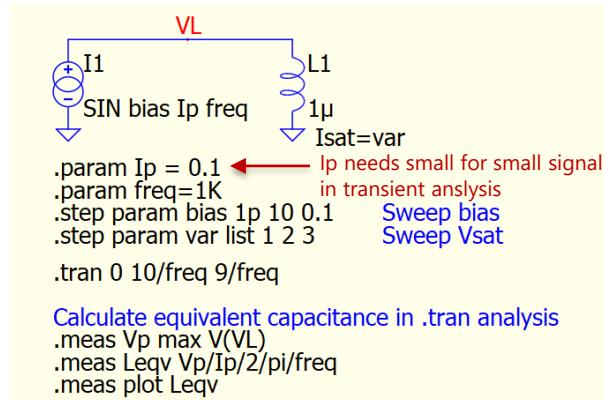


- Inductance equation
 - $X_L = \omega L = \frac{V_L}{I_L}$
 - $L = \frac{|V_L|}{|I_L|} \frac{1}{\omega} = \frac{|V_L|}{2\pi f |I_L|}$
 - This formula is used to calculate equivalent inductance (small signal model) at different inductor bias current

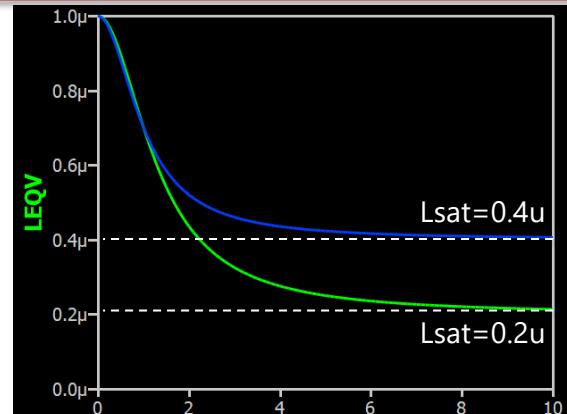
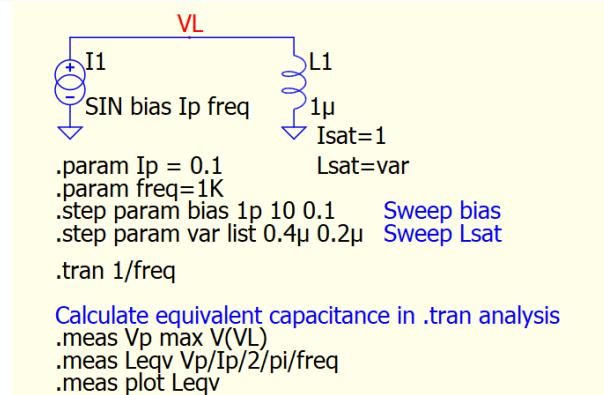
L. Instance Params : Isat, Lsat, Satfrac : For Nonlinear Inductance

Qspice : L Inductor (Tran) - Vsat.qsch ; L Inductor (Tran) - Lsat.qsch

- Isat and Satfrac
 - **Isat** : Current that drops inductance to **Satfrac x Inductance**
 - **Satfrac** : Fractional drop in inductance at Isat
 - default = 0.7



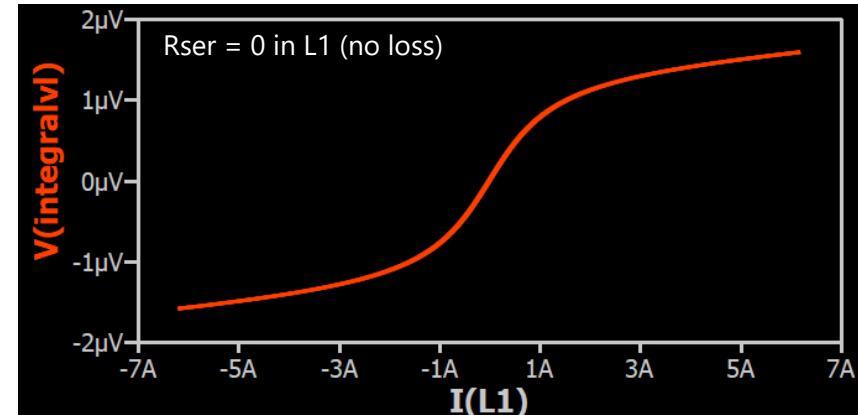
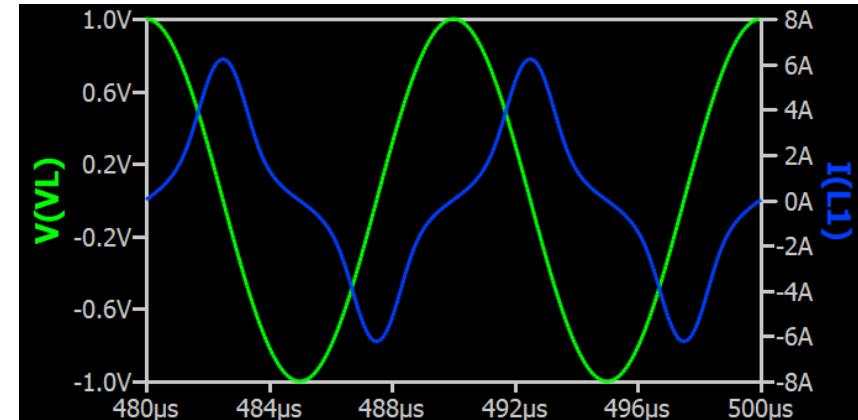
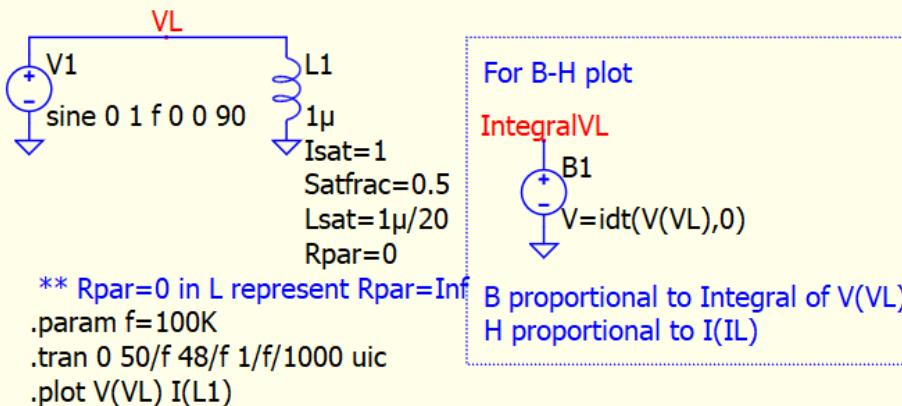
- Lsat
 - **Lsat** : Inductance asymptotically approached in saturation
 - ** Lsat must be set to see its effect



Demonstration of Nonlinear Inductor (model B-H saturation)

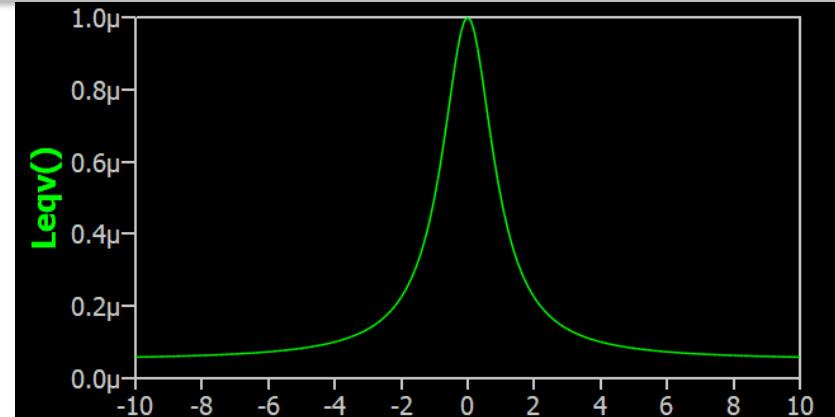
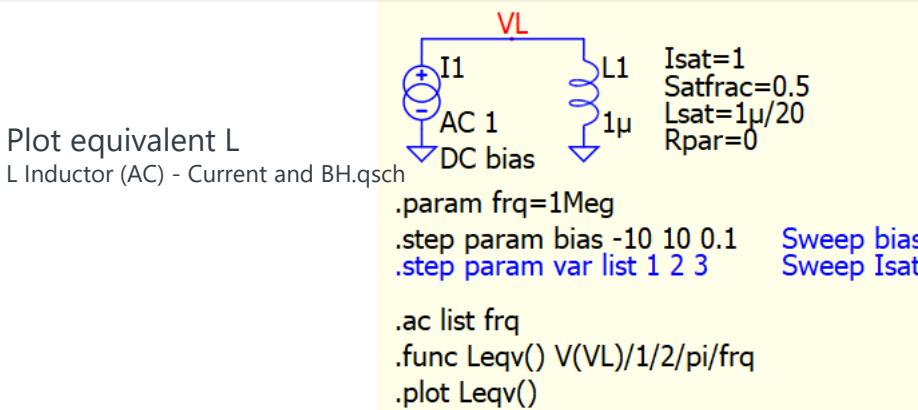
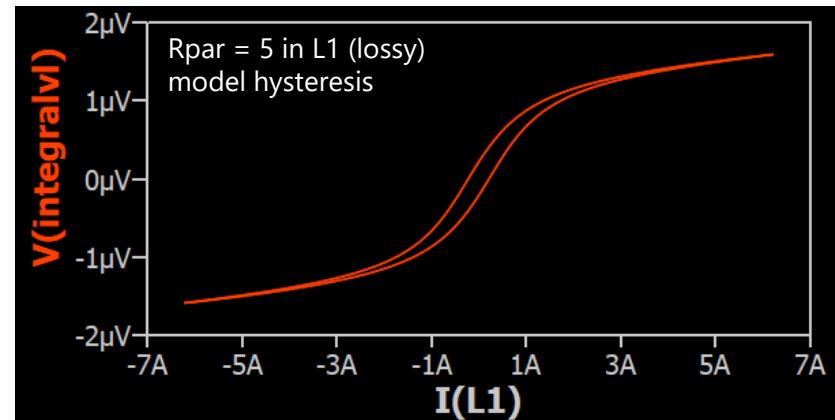
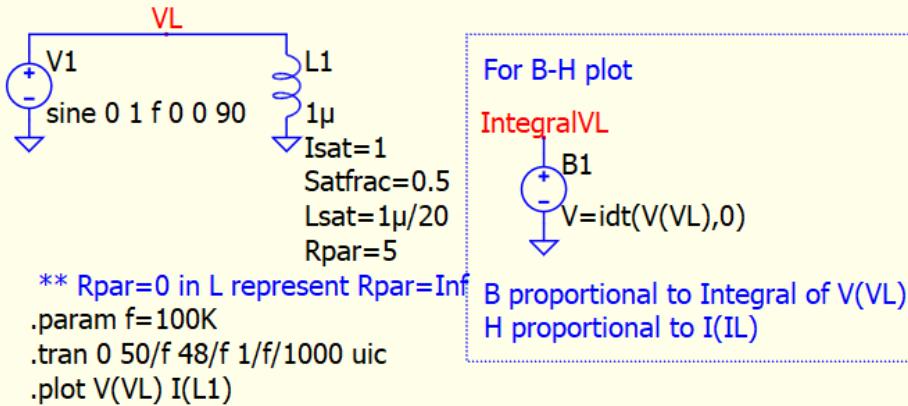
Qspice : L Inductor Nonlinear (Tran) - Current and BH.qsch

- Nonlinear Inductor in Qspice
 - This simulation demonstrate transient of non-linear inductor with a sinusoidal voltage source, which can expect a non-linear current
- Reference : B and H for inductor
 - Magnetic field intensity $H = \frac{B}{\mu} = \frac{N}{l_e} i_L$ (unit : A/m)
 - Magnetic field strength $B = \frac{\phi_B}{A_e} = \frac{1}{N A_e} \int v_L dt$ (unit : Tesla)
 - B also called magnetic flux density



Demonstration of Nonlinear Inductor (model B-H hysteresis : lossy)

Qspice : L Inductor Nonlinear (Tran) - Current and BH.qsch



Comment about Saturation and Hysteresis of B-H curve

Isat, Lsat and Satfrac are key parameters in Qspice for non-linear inductance modeling. General interest is just a saturating include. This represents inductor saturating when current reach certain level (i.e. inductance drop according to current, which can model by Isat, Lsat and Satfrac). This characteristic is saturation in B-H curve.

For hysteresis of B-H curve, it can generally model with a parallel resistor Rpar to represent loss.

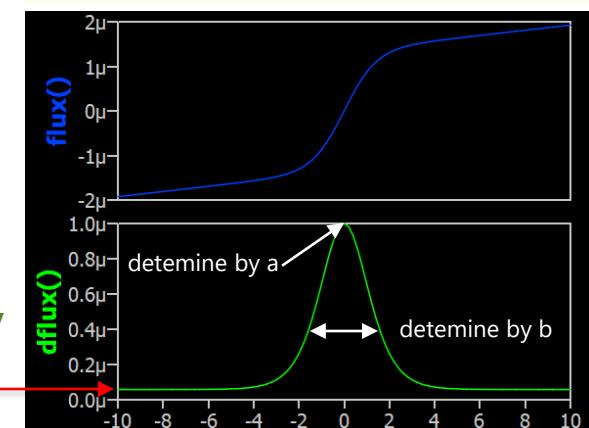
May be some people prefer to model non-linear inductor with other way, but I found Qspice definition generally good enough as L vs bias current can be easily measure practically.

L. Arbitrary Inductance : Inductor modeling with FLUX

Qspice : Flux formula.qsch

- Basic equation of Inductor
 - [equation 1] : Voltage v_L and Flux ϕ Relationship : $v_L = \frac{d\phi}{dt}$
 - [equation 2] : Voltage v_L and Current i_L Relationship : $v_L = L \frac{di_L}{dt}$
 - Therefore, by $\frac{d\phi}{dt} = L \frac{di_L}{dt}$, **Inductor $L = \frac{d\phi}{di_L}$**
- Qspice inductor modeling with Flux ϕ
 - For linear inductor, $\frac{d\phi}{di_L}$ is constant $\rightarrow \phi = L i_L$
 - Therefore, $L = \frac{\phi}{i_L}$
 - In Qspice : $\text{flux} = L * I(L1)$, where L1 is inductor name
 - For nonlinear inductor, ϕ can be approximate by $\phi = a \tanh(b i_L)$
 - Therefore, $L = \frac{d\phi}{di_L} = \frac{d a \tanh(b i_L)}{di_L} = a b (1 - \tanh^2(b i_L))$
 - In Qspice : $\text{flux} = a * \tanh(b * I(L1))$
 - L0A @ 0A = $a * b$
 - b determines the spread
 - If $b i_L$ is large, $(1 - \tanh^2(b i_L)) = 0$, therefore, this formula will give 0H inductance when i_L is large
 - It can combine nonlinear and linear to handle 0H inductance when i_L is large
 - In Qspice : $\text{flux} = a * \tanh(b * I(Ln)) + Lmin * I(Ln)$
 - L0A @ $i_L = 0$: $a * b - Lmin$
 - Lmin @ $i_L = \infty$: $Lmin$
 - b determines the spread

```
V1  
.param b = 0.7  
.param L0A = 1μ  
.param a = (L0A-Lmin)/b  
.param Lmin=58n  
.func flux() a*tanh(b*IL)+Lmin*IL  
Calculate dflux/dIL  
.func dflux() D(flux())  
Sweep IL from -10A to 10A  
.step param IL -10 10 0.2  
.op  
.plot dflux()  
.plot flux()
```



$$dflux() = Leqv$$

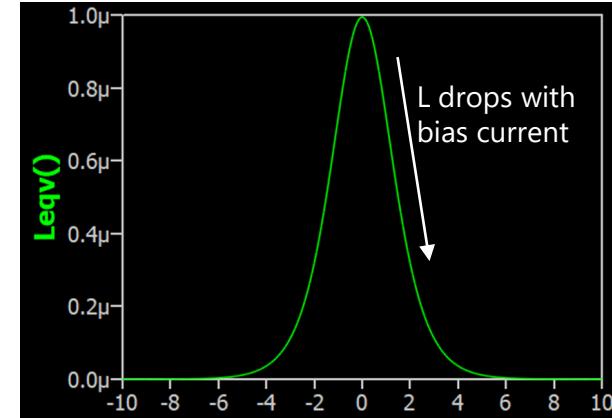
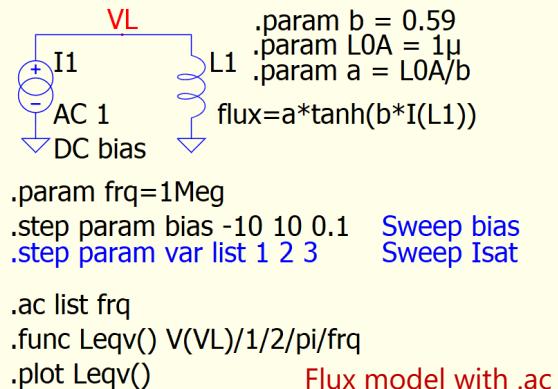
determine by $Lmin$

L. Arbitrary Inductance : Inductor modeling with FLUX

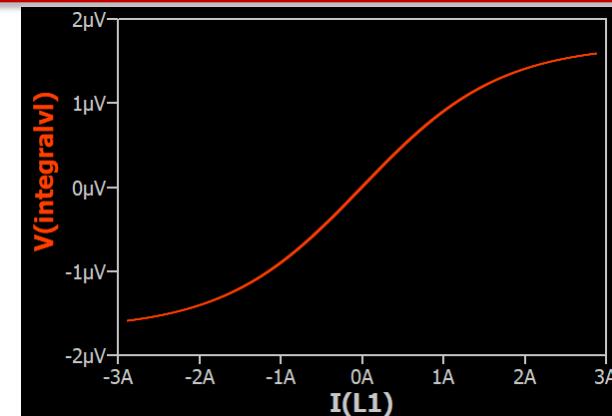
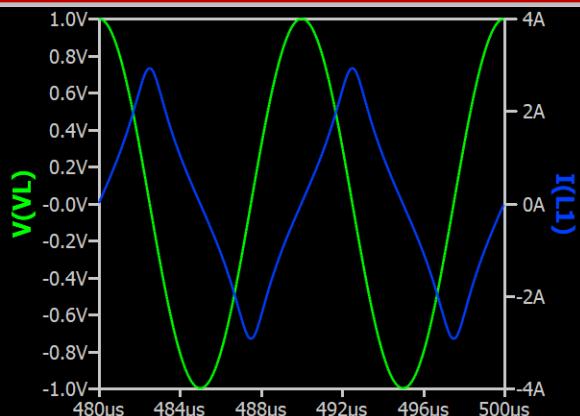
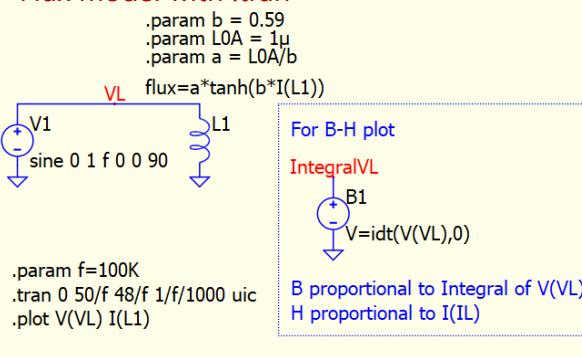
Qspice : L Inductor (AC) - Flux eqn 1.qsch ; L Inductor Nonlinear (Tran) - Flux eqn 1.qsch

- Flux model

- .ac is used to calculate inductance and bias current relationship
- .tran is used to demonstrate non-linear inductor current and proportional B-H curve
- Flux equation uses format
 - $\text{Flux} = a * \tanh(b * I(L1))$



Flux model with .tran



L. Arbitrary Inductance : Inductor modeling with FLUX – Nonlinear with Lmin

Qspice : L Inductor (AC) - Flux eqn 2.qsch ; L Inductor Nonlinear (Tran) - Flux eqn 2.qsch

- Flux Model

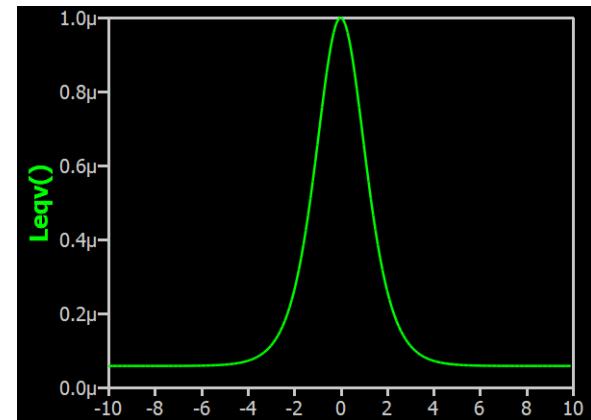
- This is nonlinear flux model include Lmin at large inductor current
- Flux equation uses format
 - $\text{Flux} = a * \tanh(b * I(L1)) + Lmin * I(L1)$

```

.param b = 0.7
.param LOA = 1μ
.param a = (LOA-Lmin)/b
.param Lmin=58n
flux=a*tanh(b*I(L1))+Lmin*I(L1)

.param frq=1Meg
.step param bias -10 10 0.1 Sweep bias
.step param var list 1 2 3 Sweep Isat

.ac list frq
.func Leqv() V(VL)/1/2/pi/frq
.plot Leqv()
  
```



```

.param b = 0.7
.param LOA = 1μ
.param a = (LOA-Lmin)/b
.param Lmin=58n
flux=a*tanh(b*I(L1))+Lmin*I(L1)

.sine V1 0 1 f 0 0 90

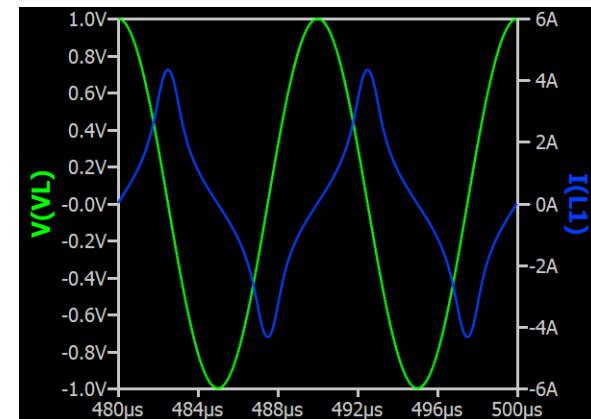
.param f=100K
.tran 0 50/f 48/f 1/f/1000 uic
.plot V(VL) I(L1)
  
```

For B-H plot

Integral_{VL} B1

$V = \text{idt}(V(VL), 0)$

B proportional to Integral of V(VL)
H proportional to I(IL)



L. Inductor

Parameter : Rpar
(Special Topic)

Inductor L Parameter : Rpar

- In Help, L. Inductor section, RPAR is mentioned default = Infinite

RPAR	Equivalent parallel resistance	Ω	Infinite
RSER	Equivalent series resistance	Ω	0.0

- However, this is not absolute truth according to Mike Engelhardt in a Qspice forum, default Rpar = $\frac{1\text{Meg}}{L}$

 Engelhardt 17d

I think it's hard to find an inductor with less parallel loss than the minimum added by default in QSPICE.

But if you don't like QSPICE'S help on this, you can add an attribute "Rpar=0" to the inductor.

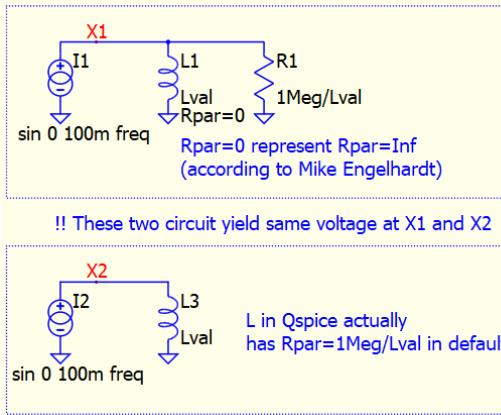
You might want to do the same for the capacitors.

- Setting Rpar = 0 can force equivalent parallel resistance to truly infinite

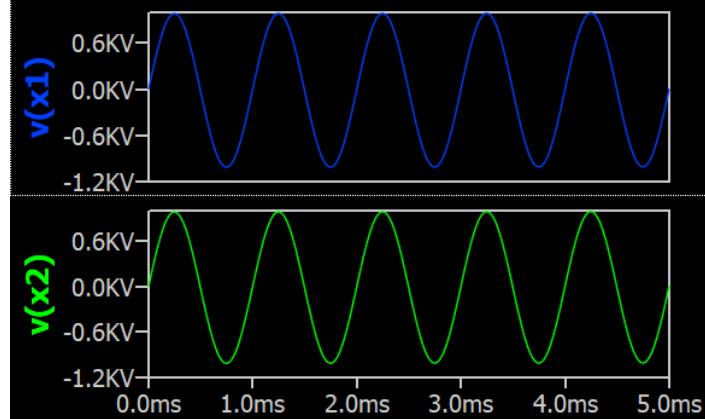
Prove Rpar = 1Meg/L in Default

Actual Rpar in Default L model - Tran.qsch

In .tran
Forced Rpar=0 (equal INF)
By adding a 1Meg/L resistor in parallel to L1, its simulation result is same as default L3

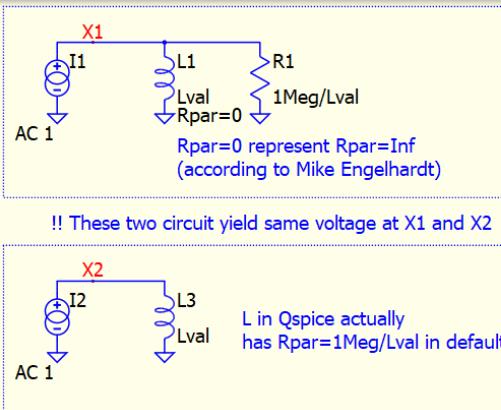


```
.param freq=1000
.tran 5/freq uic
.plot v(x2)
.plot v(x1)
.param Lval=100
```

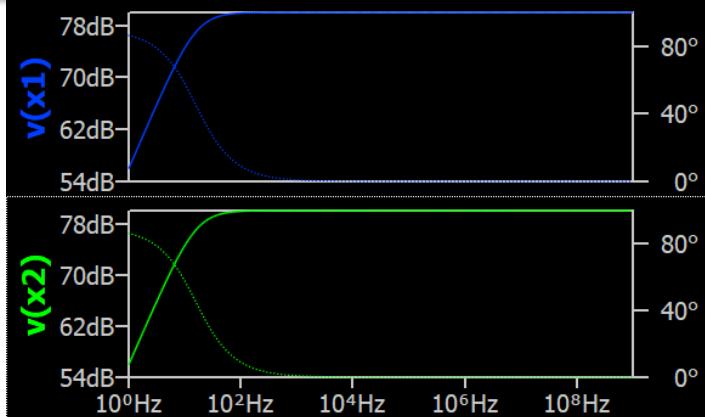


Actual Rpar in Default L model - AC.qsch

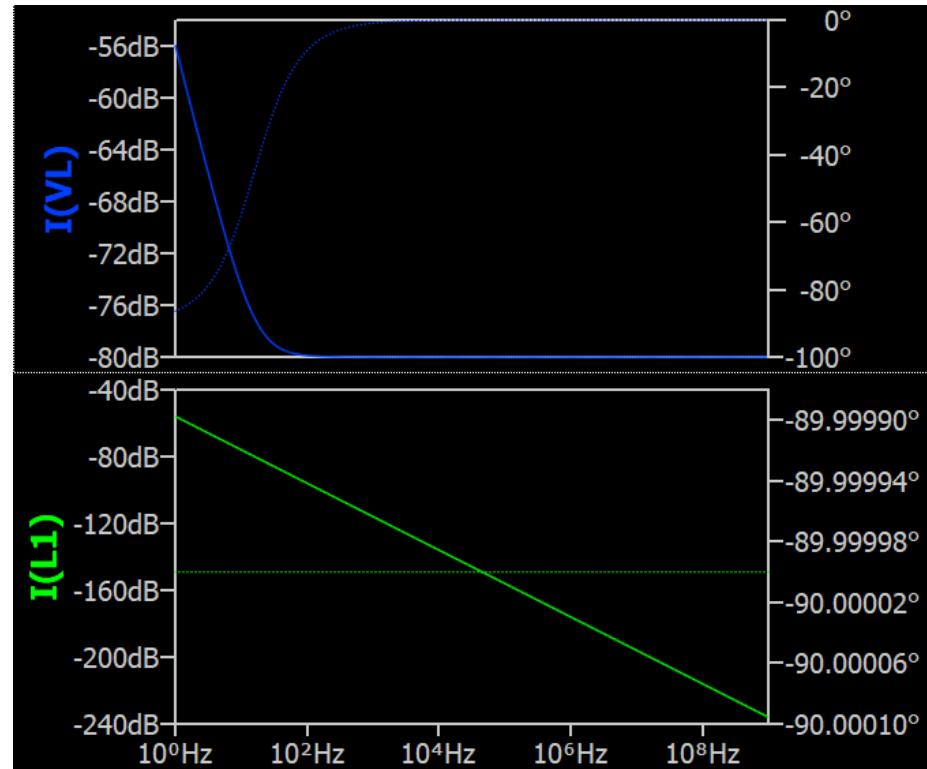
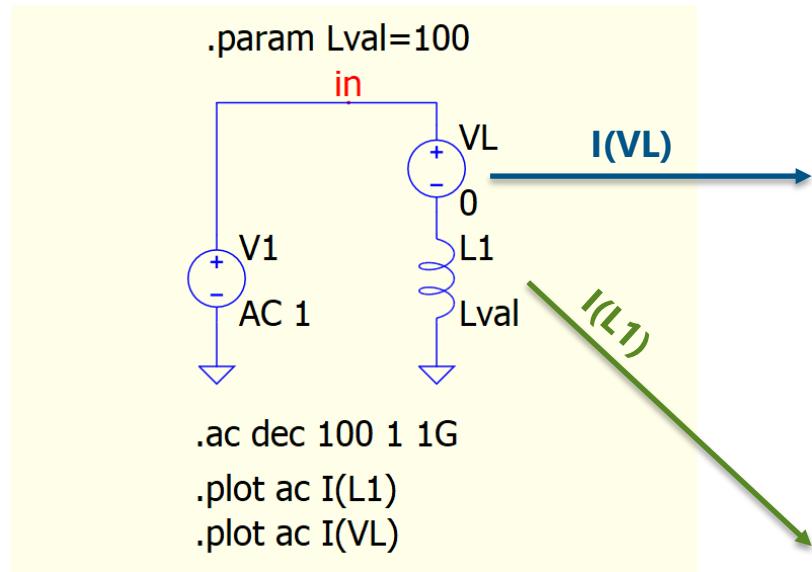
In .ac
Forced Rpar=0 (equal INF)
By adding a 1Meg/L resistor in parallel to L1, its simulation result is same as default L3



```
.ac dec 100 1 1G
.plot v(x2)
.plot v(x1)
.param Lval=100
```



What Inductor Current Actually Measured?



L1 has a $R_{par} = 1\text{Meg/L}$ resistor in parallel

But current probe $I(L1)$ only return current through L but not R_{par} ,
that is why $I(VL) \neq I(L1)$ as $I(VL)$ measures total current of L and R_{par}

Therefore, user may not aware there is a finite R_{par} if using voltage source across L and measure current of it

R. Resistor

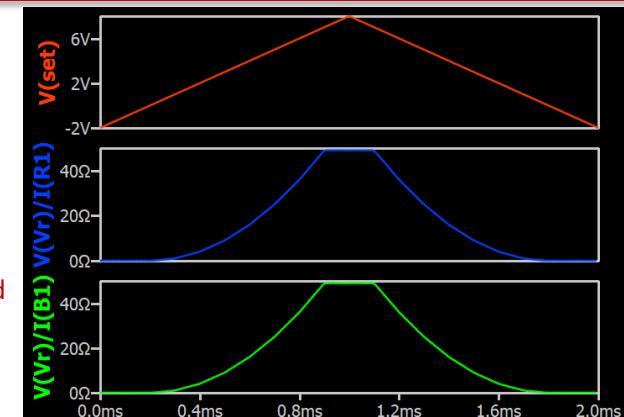
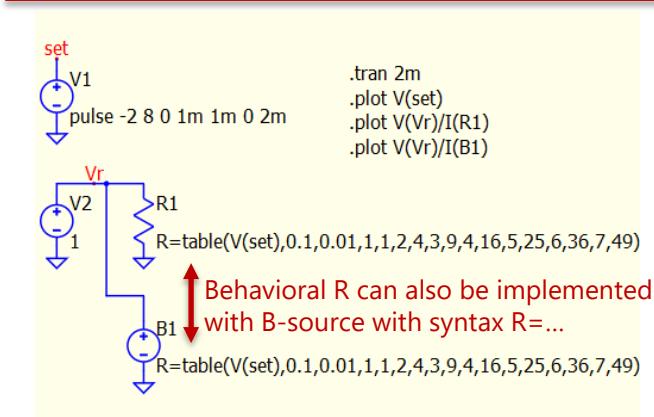
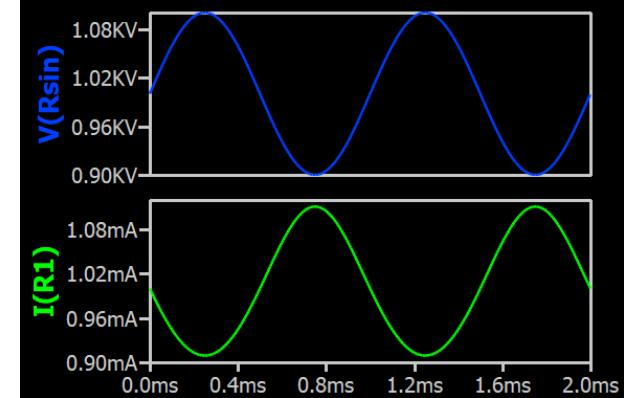
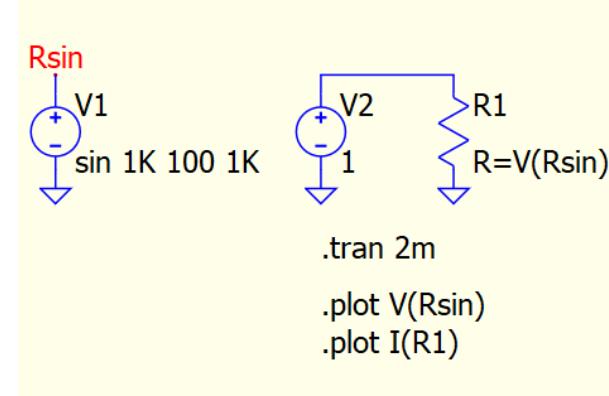
Behavioral Resistor

Behavioral Resistor (R)

Qspice : Behavioral R Demo 01.qsch ; Behavioral R Demo 02.qsch

- Behavioral Resistor

- To use formula or voltage/current node for resistance, type $R=...$ in <val> of resistor
- Also support to use Behavioral source (B) for behavioral resistor
 - Replace $V=$ expression with $R=$ expression



S. Voltage Controlled Switch

S. Voltage Controlled Switch Model Parameters

- S. Voltage Controlled Switch Model Parameters
 - It is common to define Switch Model for usage as multiple switches in a schematic
 - Syntax: Snnn N1 N2 NC+ NC- <model> [instance parameters]
 - .model <model> SW [model parameters]

Voltage Controlled Switch Model Parameters

Name	Description	Units	Default
ETA ¹	Sub-/over-Threshold conduction	V	0.0
ROFF	Off resistance	Ω	1e6
RON	On resistance	Ω	1.0
TTOL	Temporal tolerance	sec	1e308
VH	Hysteresis voltage	V	0.0
VOFF	Voltage when open	V	0.0
VON	Voltage when closed		
VT	Threshold voltage		

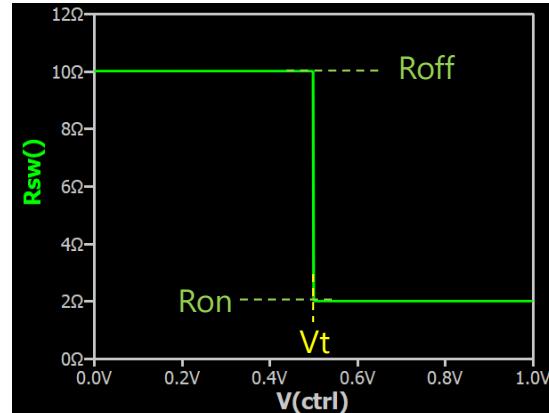
Input Control
Voltage

Switch Model Params : Ron, Roff, VT, Von and Voff

Qspice : Switch - Ron Roff VT.qsch

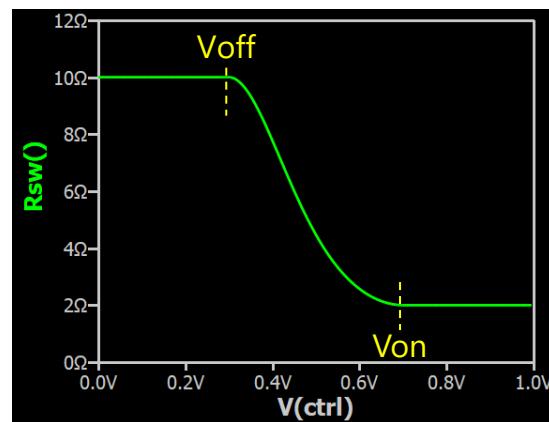
- RON, ROFF, VT
 - Ron : On resistance
 - Roff : Off resistance
 - VT : Threshold voltage

```
.model mSW SW Ron=2 Roff=10 Vt=0.5 VH=0
pulse 0 1 0 1 1 1 4
.tran 4
.func Rsw() V(sw)/I(I1)
.plot Rsw()
.plot V(ctrl)
```



- VON, VOFF
 - Von : Voltage when closed
 - Voff : Voltage when open
 - switch smoothly transitions between on and off
 - If VT and VH are specified, VON and VOFF are ignored

```
.model mSW SW Ron=2 Roff=10 Von=0.7 Voff=0.3
pulse 0 1 0 1 1 1 4
.tran 4
.func Rsw() V(sw)/I(I1)
.plot Rsw()
.plot V(ctrl)
```

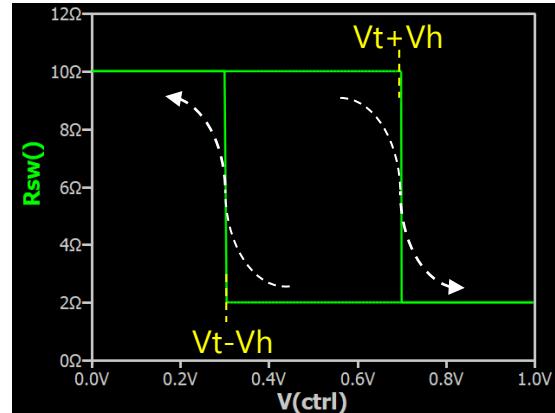


Switch Model Params : VH

Qspice : Switch - VH.qsch

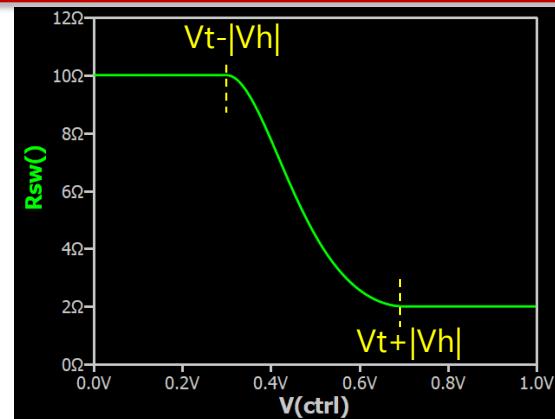
- VH
 - V_h : Hysteresis voltage

```
.model mSW SW Ron=2 Roff=10 Vt=0.5 Vh=0.2  
+ve Vh  
  
V1 --- S1 --- SW --- I1 --- 1  
|           |  
|           +-----+  
|           |       |  
ctrl      mSW    SW  
  
pulse 0 1 0 1 1 1 4  
.tran 4  
.func Rsw() V(sw)/I(I1)  
.plot Rsw()  
.plot V(ctrl)
```



- VH (-vegitive explains)
 - Negative V_h
 - If VH is negative the switch smoothly transitions between on and off

```
.model mSW SW Ron=2 Roff=10 Vt=0.5 Vh=-0.2  
-ve Vh  
  
V1 --- S1 --- SW --- I1 --- 1  
|           |  
|           +-----+  
|           |       |  
ctrl      mSW    SW  
  
pulse 0 1 0 1 1 1 4  
.tran 4  
.func Rsw() V(sw)/I(I1)  
.plot Rsw()  
.plot V(ctrl)
```

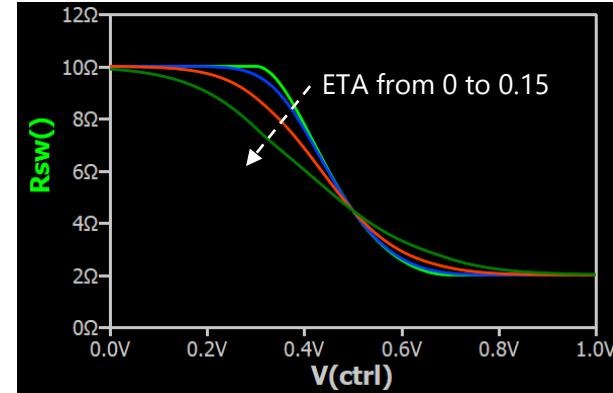


Switch Model Params : ETA

Qspice : Switch - ETA.qsch

- ETA
 - ETA : Sub-/over- Threshold conduction
 - Prevents the control voltage Jacobian from vanishing
 - Only effective in smoothly transitions cases
 - V_t is negative
 - V_{on} / V_{off} are used without V_t and V_h

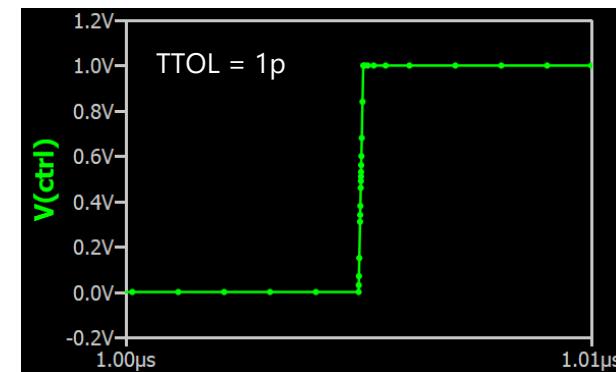
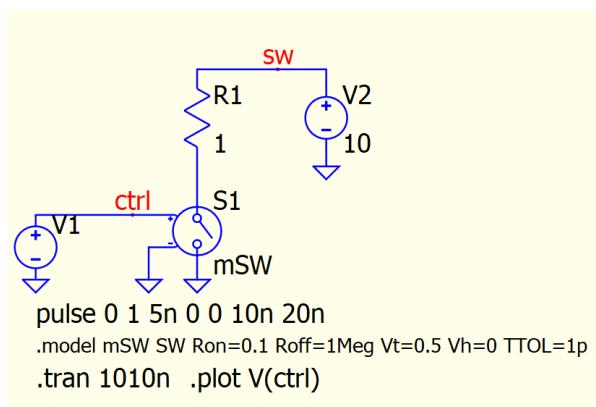
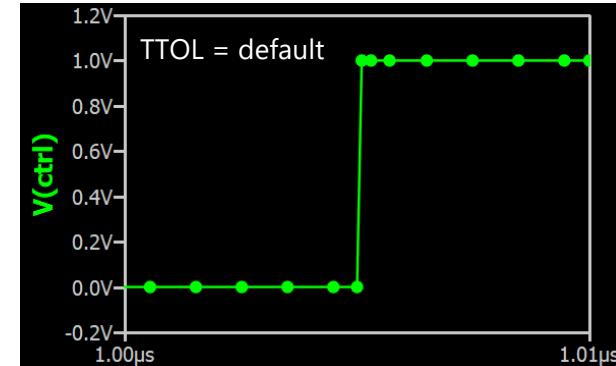
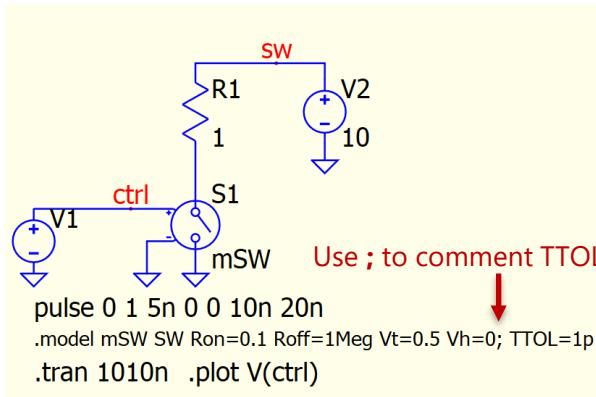
```
.model mSW SW Ron=2 Roff=10 Vt=0.5 Vh=-0.2 ETA=ETA
          S1
          SW
          I1
V1      ctrl
          S1
          mSW
          I1
          1
pulse 0 1 0 1 1 1 4
.step param ETA list 0 0.05 0.1 0.15
.tran 4
.func Rsw() V(sw)/I(I1)
.plot Rsw()
.plot V(ctrl)
```



Switch Model Params : TTOL

Qspice : Switch - TTOL.qsch

- TTOL
 - Ttol : Temporal tolerance
 - **Default TTOL=1e308s**
- Usage
 - TTOL allows one to determine how accurately the switch time should be found
 - It only affect timestep at switch time, which maintain simulation speed but improve accuracy at switching or logic action



T. Lossless Transmission Line

T. Lossless Transmission Line Instance Parameters

- T. Lossless Transmission Line
 - Syntax: Tnnn L+ L- R+ R- Zo=<value> Td=<value>

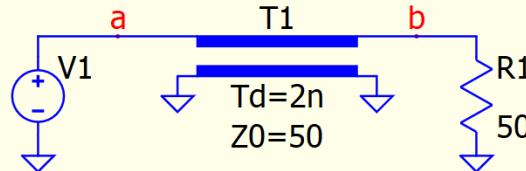
Lossless Transmission Line Instance Parameters

Name	Description	Units	Default
F ¹	Frequency	Hertz	1GHz
NL ¹	Normalized length at frequency given	wavelengths	1/4
TD	Transmission delay	sec	
Z0	Characteristic impedance(aka ZO)	Ω	50 Ω

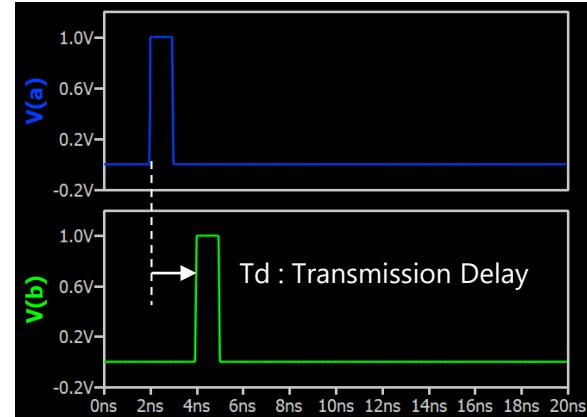
T. Instance Params : TD, F and NL

Qspice : Tline - Td.qsch ; Tline - F NL.qsch

- TD
 - Td : Transmission delay
 - This simulation terminate transmission line with characteristic impedance Z_0 , no reflection of signal
 - If TD is given, F and NL are ignored

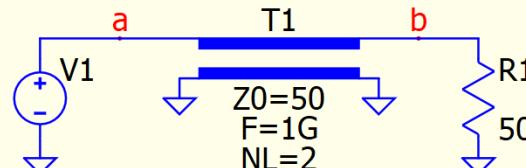


```
pulse 0 1 2n 0 0 1n 1 1  
.options MAXSTEP=1p  
.tran 20n  
.plot V(b)  
.plot V(a)
```

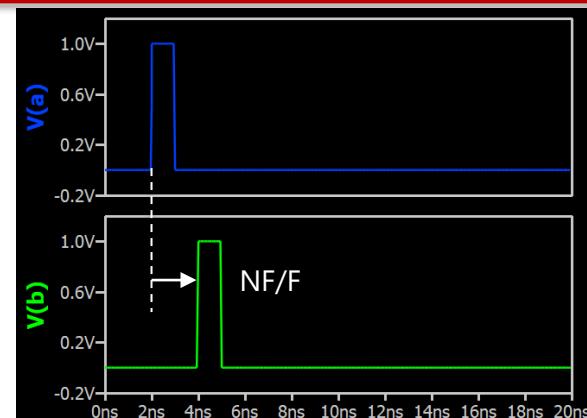


- F and NL
 - F : Frequency
 - NL : Normalized length at frequency given
 - Equation

$$\begin{aligned} NL &= \frac{\text{Length}}{\text{Wavelength}} = \frac{\text{Length}}{\lambda} \\ \text{Period per } \lambda &: T = \frac{1}{F} \\ \text{Delay } T_d &= T \times \frac{\text{Length}}{\lambda} = \frac{NL}{F} \end{aligned}$$



```
pulse 0 1 2n 0 0 1n 1 1  
.options MAXSTEP=1p  
.tran 20n  
.plot V(b)  
.plot V(a)
```



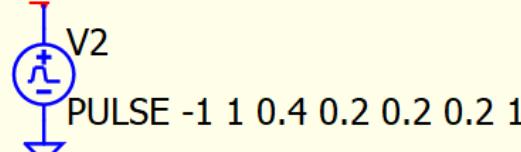
V. Voltage Source

V. Voltage Source : PULSE (Pulse)

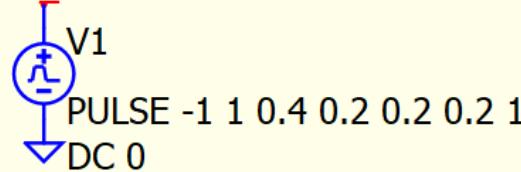
Qspice : Vsource PULSE.qsch

Syntax : PULSE V1 V2 Td Trise Tfall Ton Tperiod

pulse_woDC

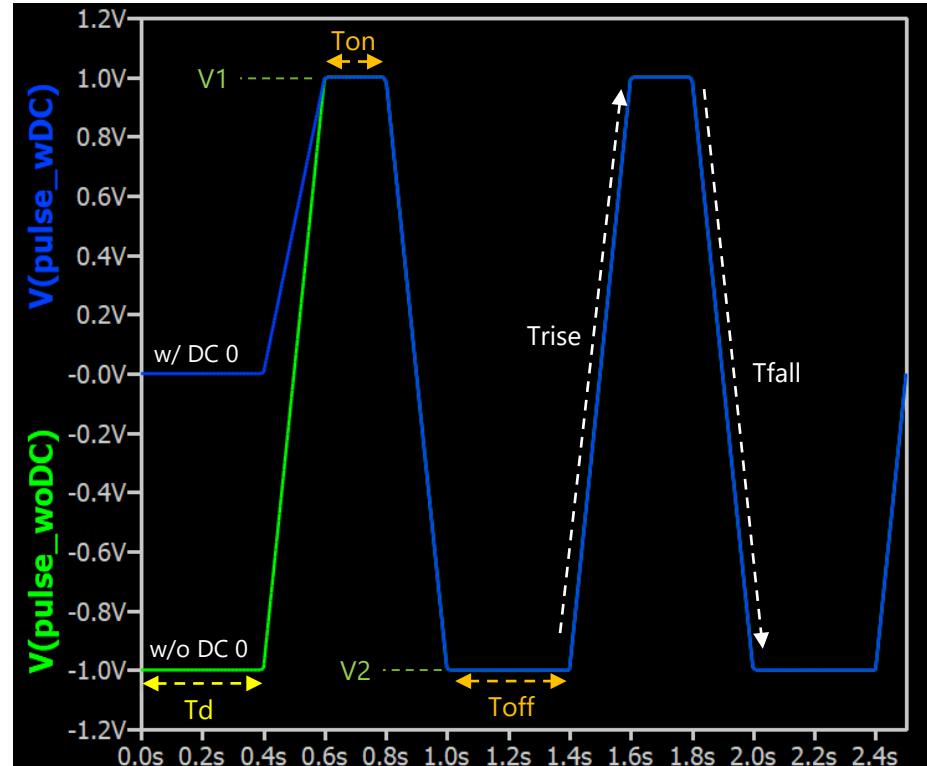


pulse_wDC



.tran 2.5

.plot V(pulse_woDC) V(pulse_wDC)

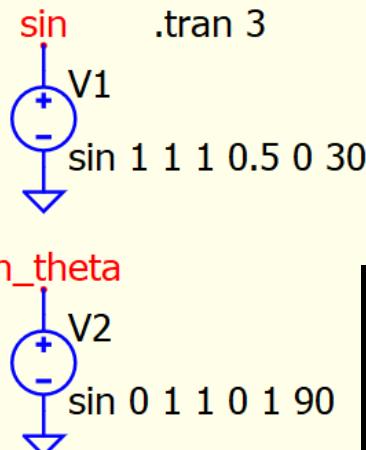


V. Voltage Source : SIN (Sine Wave)

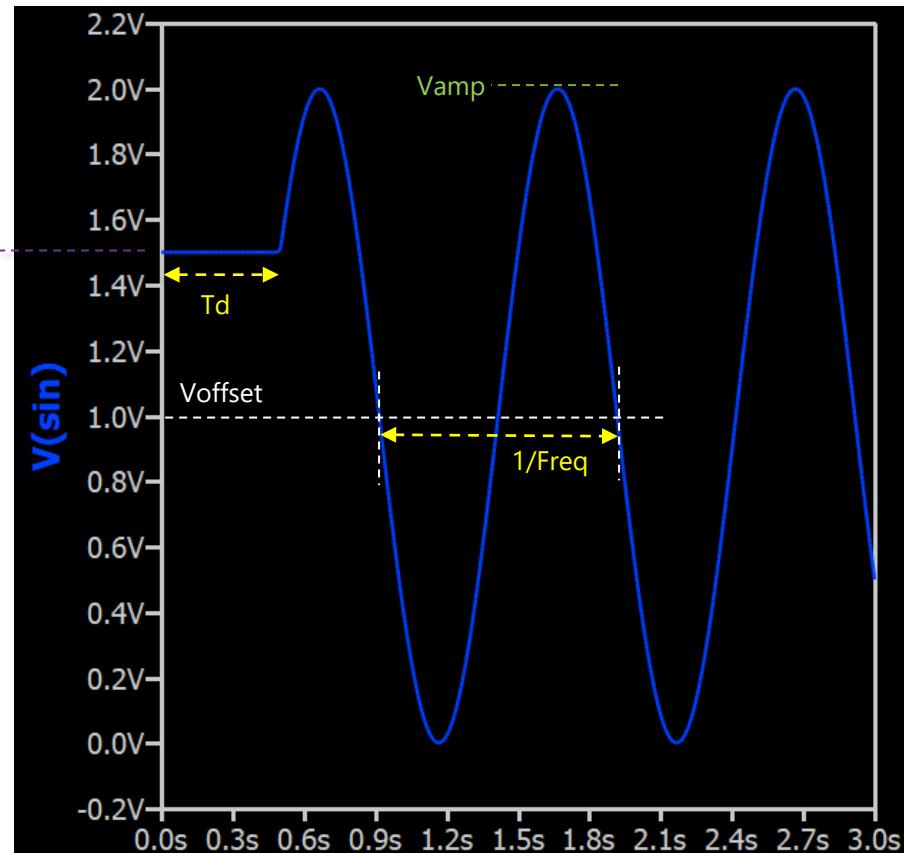
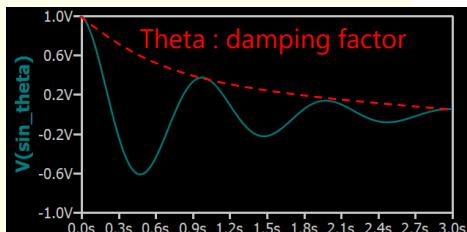
Qspice : Vsource SIN.qsch

Phi : level = $V_{offset} + \sin(\Phi)$
e.g.: $=1+\sin(30^\circ) = 1.5$

Syntax : SIN Voffset Vamp Freq Td Theta Phi



Amplitude drops by $e^{-1} \sim 0.378$ in $1/\Theta$ seconds



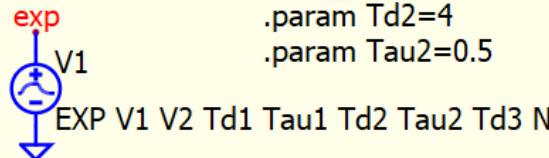
V. Voltage Source : EXP (Exponential)

Qspice : Vsource EXP.qsch

```
.plot V(expTperiod) V(exp)
```

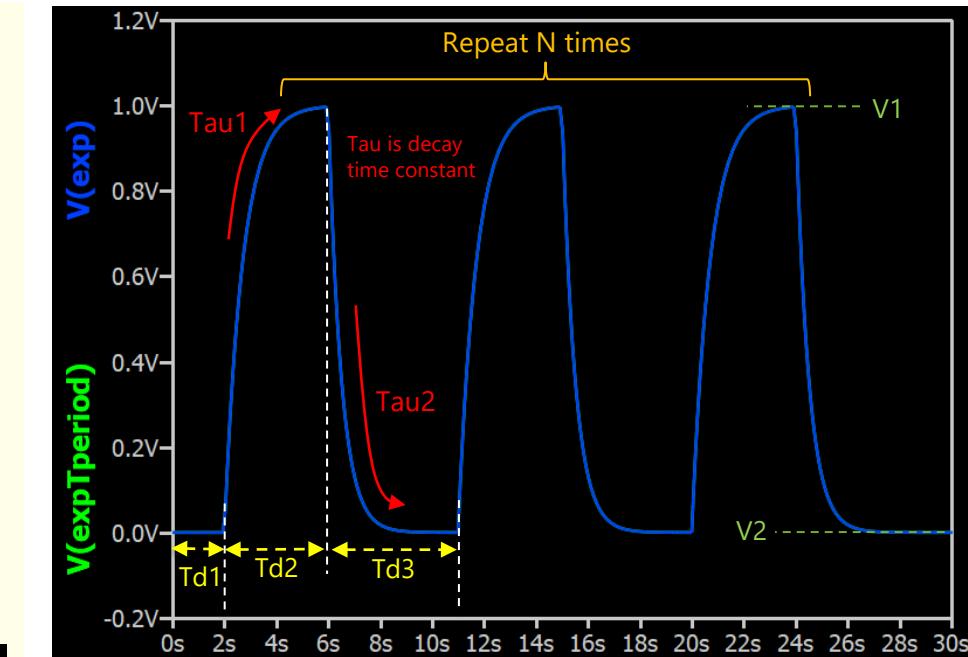
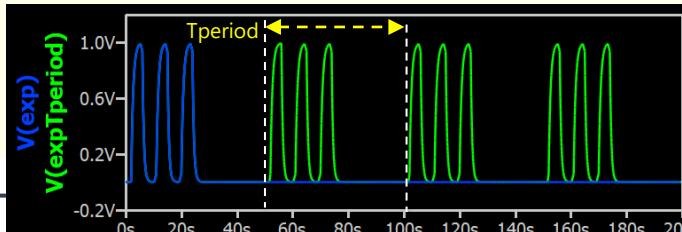
Syntax : EXP V1 V2 Td1 Tau1 Td2 Tau2 Td3 N Tperiod

```
.tran 200          .param V1=0      .param Td3=9  
                   .param V2=1      .param N=3  
                   .param Td1=2      .param Tperiod=50  
                   .param Tau1=0.7  
                   .param Td2=4  
                   .param Tau2=0.5
```



expTperiod

```
EXP V1 V2 Td1 Tau1 Td2 Tau2 Td3 N Tperiod
```



V. Voltage Source : SFFM (Single Frequency FM)

Qspice Vsource SFFM.qsch

- SFFM
 - Single Frequency FM
 - It is hard to observe FM signal in time domain waveform
 - FFT is used to explain its nature

Syntax : SFFM Voff Vamp Fcar MDI Fsig

SFFM



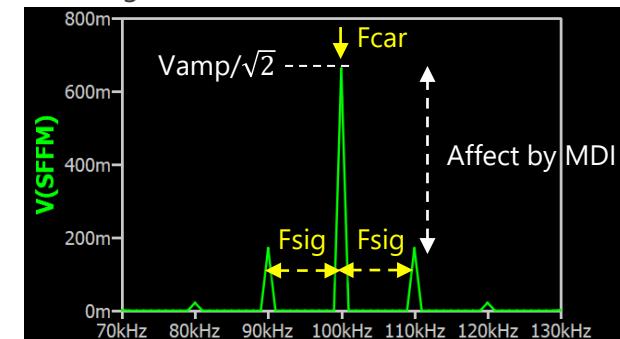
V1

SFFM 0 1 100K 0.5 10K

.tran 10/10K

.plot V(SFFM)

FFT magnitude is RMS

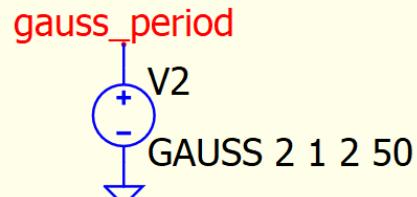
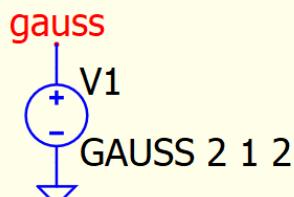


- Transient formula
 - $V_{off} + V_{amp} \cdot \sin((2\pi \cdot F_{car} \cdot time) + MDI \cdot \sin(2\pi \cdot F_{sig} \cdot time))$

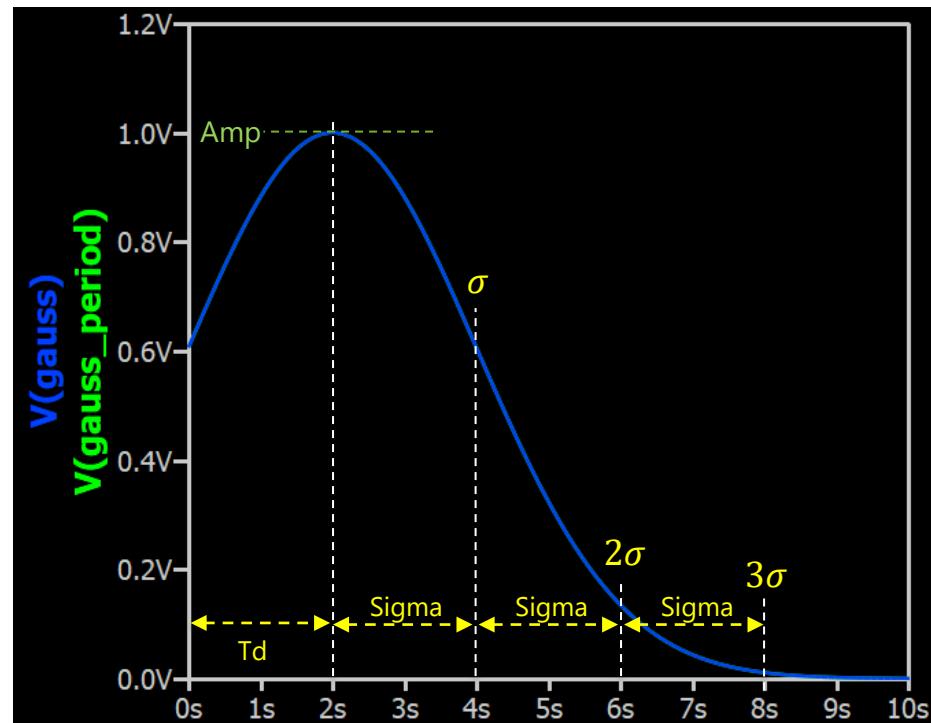
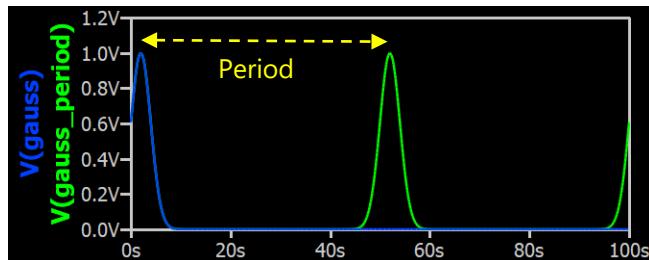
V. Voltage Source : GAUSS (Gaussian Pulse)

Qspice Vsource GAUSS.qsch

Syntax : GAUSS Td Amp Sigma [Period]



```
.plot V(gauss_period) V(gauss)
.tran 100
```

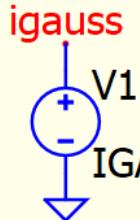


V. Voltage Source : IGAUSS (Imaginary Gaussian Pulse)

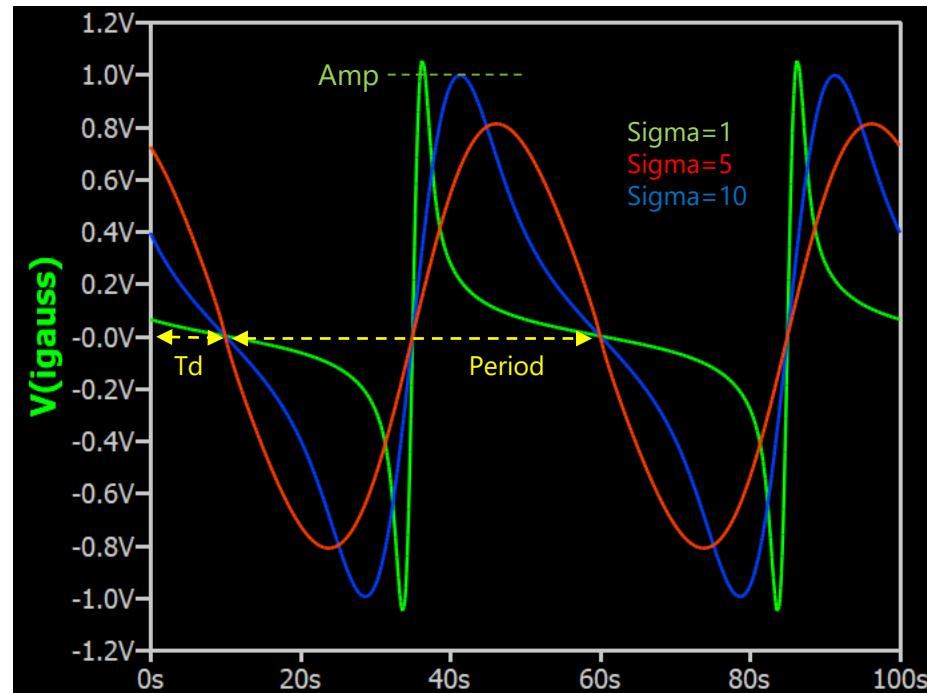
Qspice Vsource IGAUSS.qsch

Syntax : IGAUSS Td Period Sigma Amp

.step param Sigma list 1 5 10



.plot V(igauss)
.tran 100

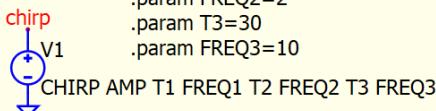


V. Voltage Source : CHIRP (Piece-wise Linear Chirp)

Qspice Vsource Chirp.qsch

Syntax : CHIRP(AMP T1 FREQ1 T2 FREQ2 [...]) [LOG] [XTRAP]

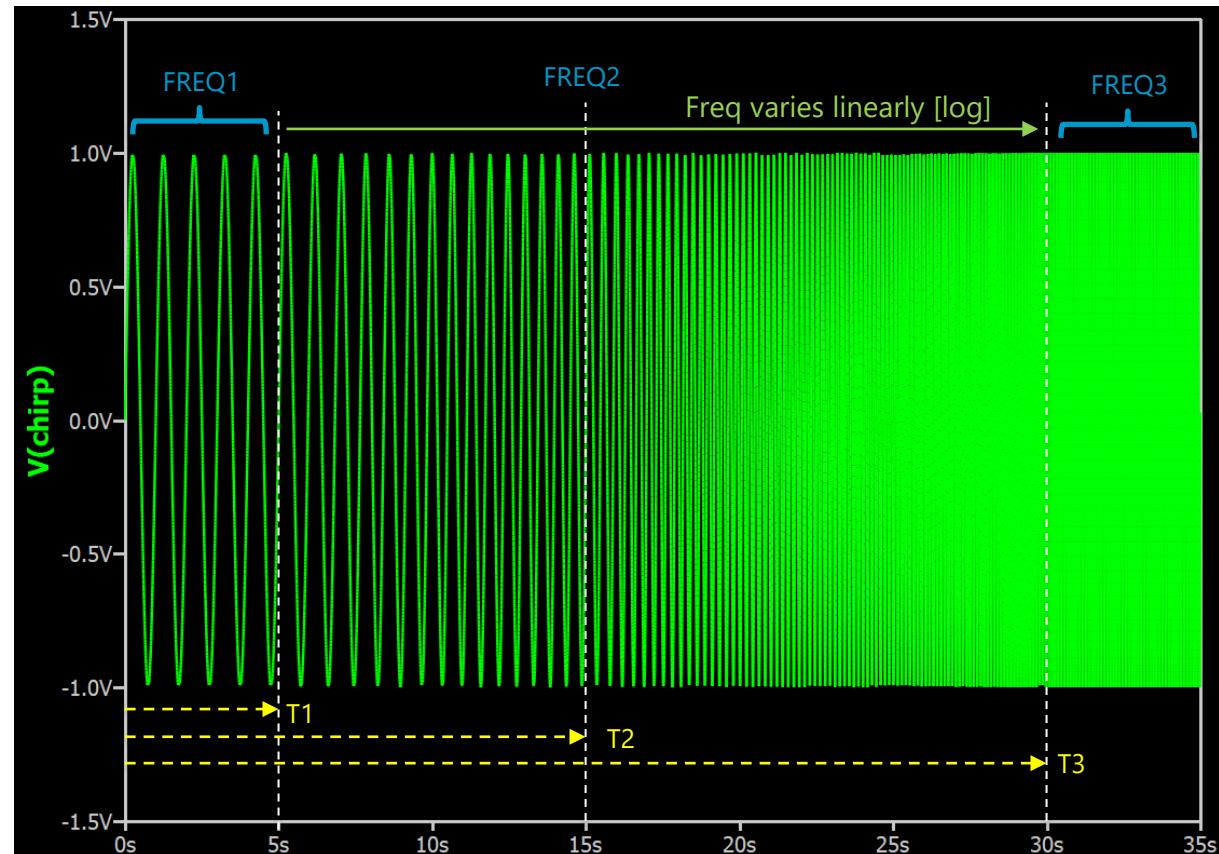
```
.param AMP=1  
.param T1=5  
.param FREQ1=1  
.param T2=15  
.param FREQ2=2  
.param T3=30  
.param FREQ3=10
```



```
.plot V(chirp)  
.tran 35
```

```
.options MAXSTEP=1/1000
```

XTRAP : extrapolate beyond PWL and CHIRP points

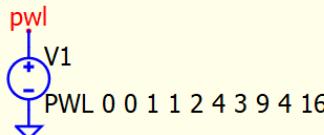


V. Voltage Source : PWL (Piece-wise Linear)

Qspice Vsource PWL.qsch ; Vsource PWL-Log.qsch ; Vsource PWL file.qsch

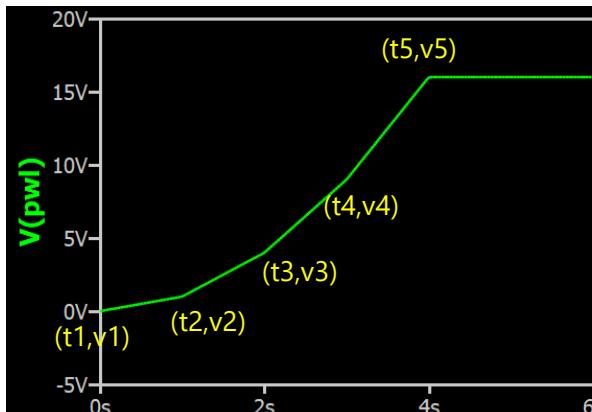
XTRAP : extrapolate beyond PWL and CHIRP points

Syntax : PWL(t1 v1 t2 v2 t3 v3...) [LOG] [XTRAP]

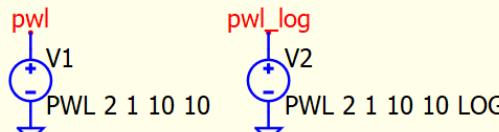


.tran 6
.plot V(pwl)

Vsource PWL.qsch

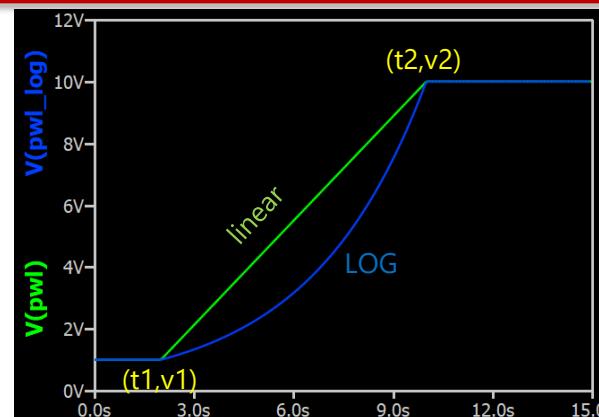


Syntax : PWL(t1 v1 t2 v2 t3 v3...) [LOG] [XTRAP]



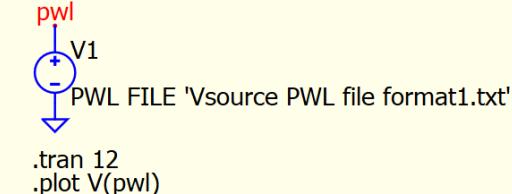
.tran 15
.plot V(pwl) V(pwl_log)

Vsource PWL-Log.qsch



Support load time/value from file.txt

Syntax : PWL FILE file.txt [LOG] [XTRAP]



.tran 12
.plot V(pwl)

Vsource PWL file format1.txt

1	1	1
2	2	4
3	3	9
4	4	16
5	5	25
6	6	36
7	7	49
8	8	64
9	9	81
10	10	100

Vsource PWL file format2.txt

1	1, 1
2	2, 4
3	3, 9
4	4, 16
5	5, 25
6	6, 36
7	7, 49
8	8, 64
9	9, 81
10	10, 100

\tilde{A} -Device

Ã-Device

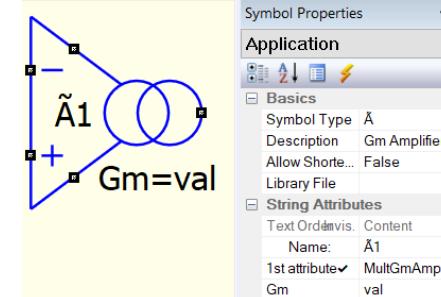
- Ä-Device
 - Syntax

~nnn VDD VSS OUT IN- IN+ MULT+ MULT- IN-- IN++ EN ##### <TYPE> [INSTANCE PARAMETERS]

- \tilde{A} -device models a highly configurable Gm block than can mimic the behavior of a complementary MOSFET output, there are two types MULTGMAMP and RROPAMP

A-Device Types	
Type	Behavior
MULTGMAMP	Multiplying Gm Amplifier
RROPAMP	Rail-to-Rail Output OpAmp

- In Symbol Properties > 1st attribute
- View > Netlist : from device syntax



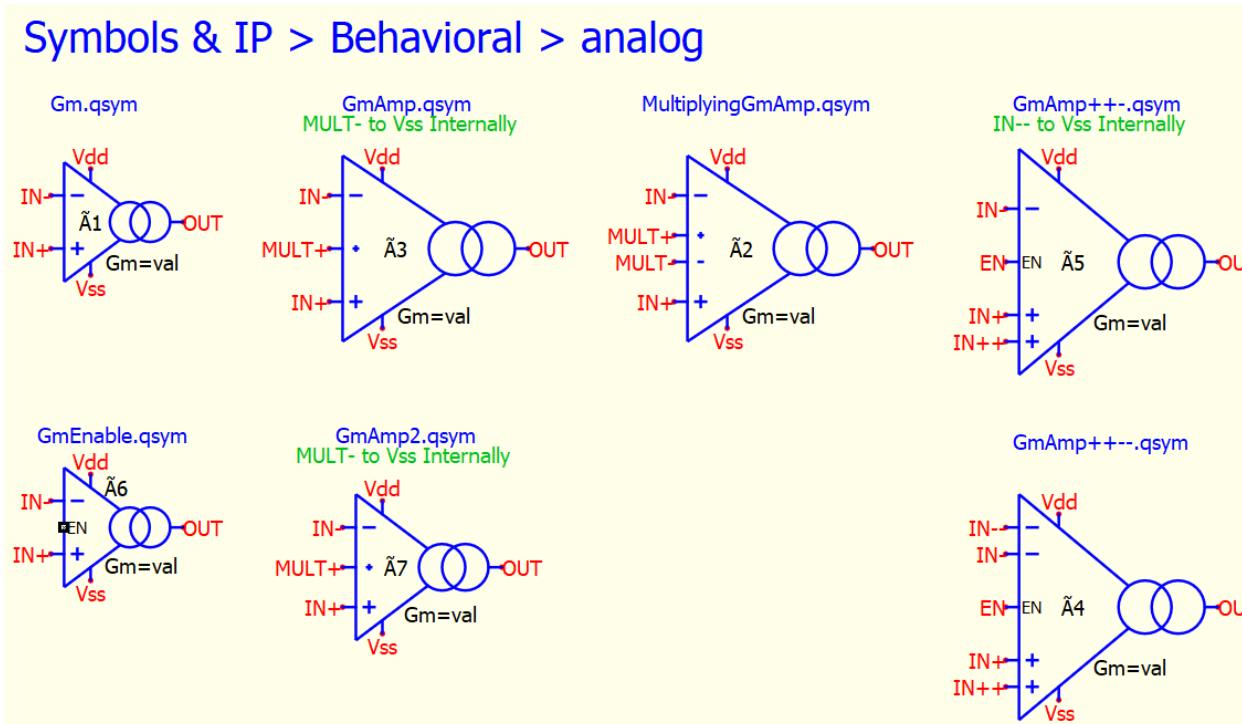
```
* C:\Users\kelvinleung\Documents\QSPICE\Untitled.qsch
A1 Y0 Y1 Y2 Y3 Y4 Y Y Y Y Y Y Y Y MultGmAmp Gm=val
.end
```

\tilde{A} -Device [MULTGMAMP]

- \tilde{A} -Device

- Syntax: **$\tilde{A}nnn\ VDD\ VSS\ OUT\ IN-\ IN+\ MULT+\ MULT-\ IN--\ IN++\ EN\ \#\#\#\#\#\#<TYPE>\ [INSTANCE\ PARAMETERS]$**
- Formula in Linear Region : $i_{out} = GM * V(MULT+, MULT-) * V(\min(IN+, IN++), \max(IN-, IN--))$

Symbols & IP > Behavioral > analog



À-Device Instance Parameters in MULTGMAMP

À-Device Instance Parameters

Name	Description
CAPINCM	Common eigenmode input capacitance
CAPINNM	Normal eigenmode input capacitance
CAPVDD	Capacitance from output to Vdd
CAPVSS	Capacitance from output to Vss
EN	Equivalent input voltage noise density
ENK	EN corner frequency
FT	3dB bandwidth of transconductance with no voltages slewing
GM	Ideal transconductance
IC	Initial condition of $V_{in} \times V_{mult}$
IN	Equivalent input current noise density
INF	Common mode input current noise density proportional to frequency
INK	IN corner frequency
IOUT	Maximum sourcing current
ISNK	Maximum sinking current
ISNKKNEE	Sharpness of Maximum sinking current limit
ISRC	Maximum sourcing current
ISRCKNEE	Sharpness of max sourcing current limit
M	Number of parallel devices

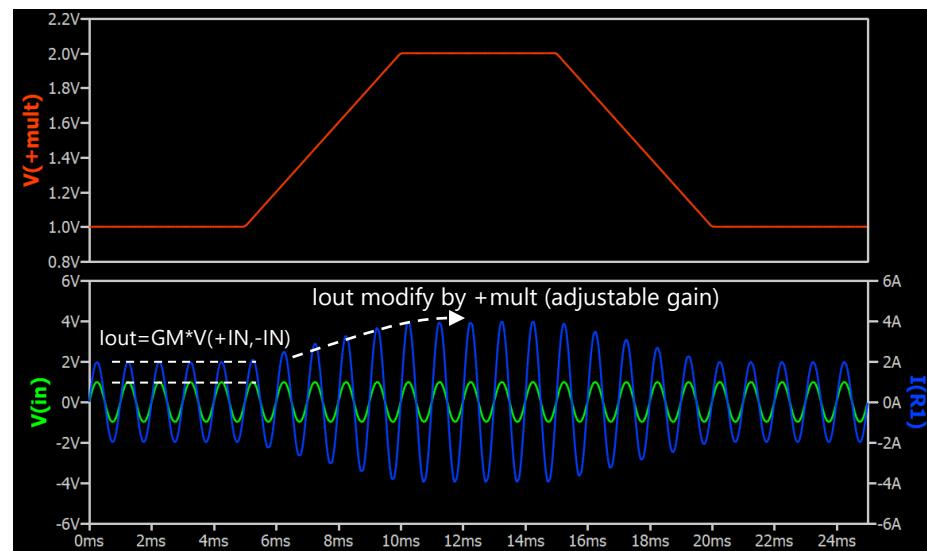
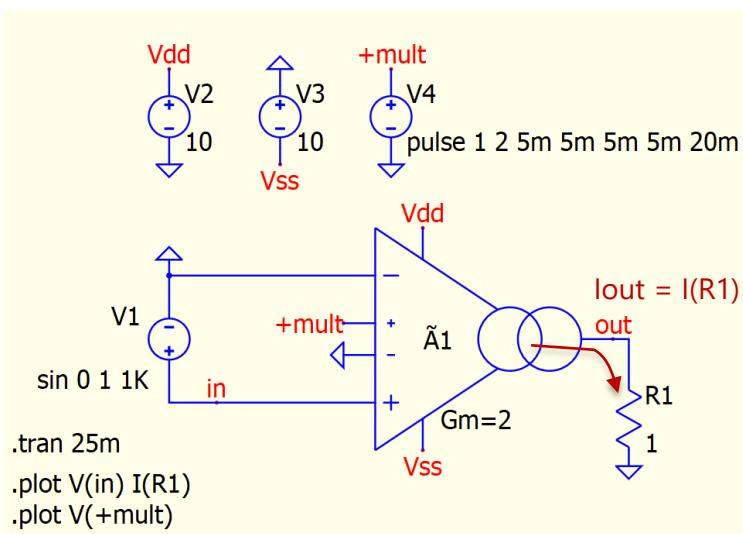
REF	Logic threshold for enable(from Vss)
ROUT	Additional impedance added to output(2*R to Vdd, 2*R to Vss)
TEMP	Instance temperature
TTOL	Temporal tolerance for enable & UVLO
UVLO	Minimum supply voltage
VCROSS	Cross conduction voltage range
VDSAT	Voltage where gm starts to switch over to a resistance
VDSAT1	Voltage where gm starts to switch over to a resistance(top FET)
VDSAT2	Voltage where gm starts to switch over to a resistance(bottom FET)
VINHIGH	Output range measured from positive rail
VINHIGHKNEE	Sharpness of positive input range limit
VINLOW	Input range measured from negative rail
VINLOWKNEE	Sharpness of negative input range limit
VOS1	Offset voltage for input
VOS2	Offset voltage for multiplying input
VOUTMAX	Maximum output voltage measured from negative rail
VOUTMIN	Minimum output voltage measured from negative rail

MULTGMAMP : Ideal transconductance (GM)

Qspice : Multgmamp - Gm.qsch

- Gm : Ideal transconductance

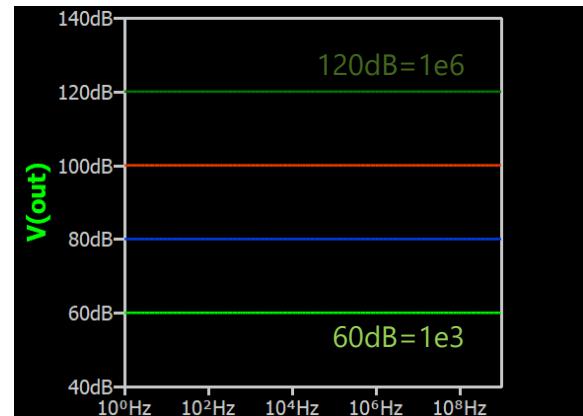
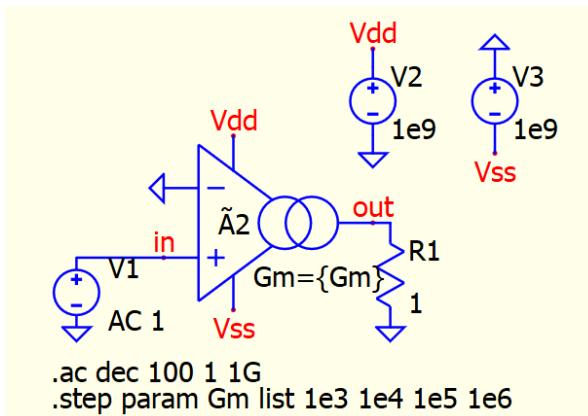
- Without IN++ and IN--, formula becomes $I_{out} = \mathbf{GM} * V(\text{MULT+}, \text{MULT-}) * V(\text{IN+}, \text{IN-})$
- For ideal operation amplifier, GM is infinity
- In Qspice, Gm cannot be set to 0



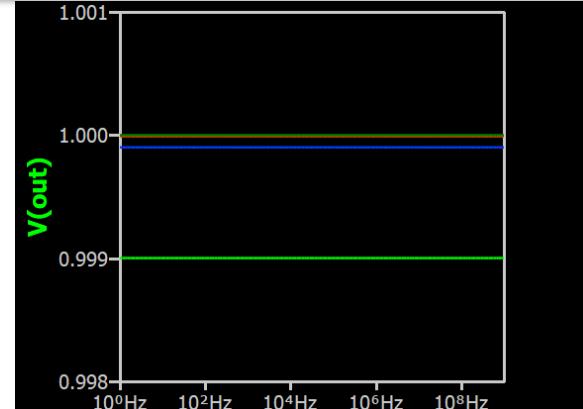
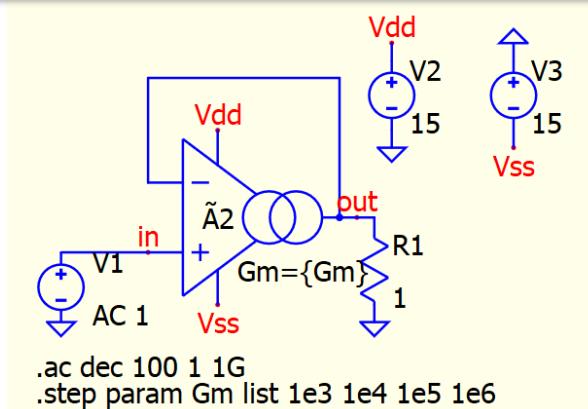
MULTGMAMP : Ideal transconductance (GM)

Qspice : Multgmamp - Gm freq response.qsch ; Multgmamp - Buffer.qsch

- Gm : Ideal transconductance
 - MULTGMAMP has ideal frequency response if without instance parameters
 - No default value of Gm, must define by user



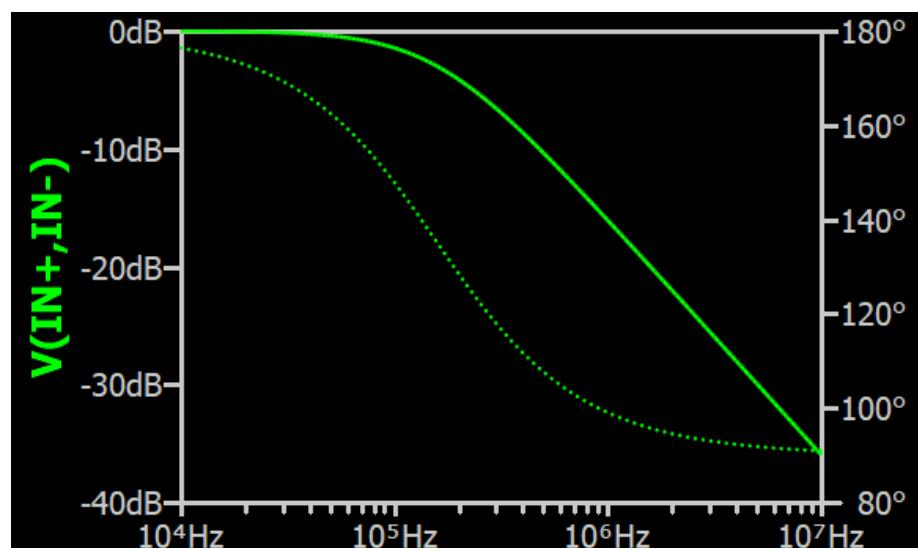
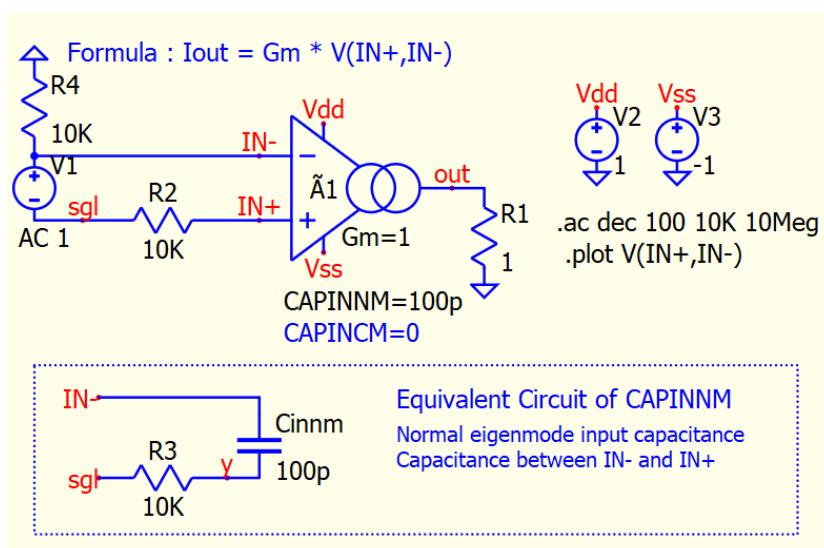
- Demo : Buffer Circuit
 - Demonstrate op-amp close loop ideal characteristic with different Gm value



MULTGMAMP : Normal eigenmode input capacitance (CAPINNM)

Qspice : Multgmamp - Capinnm.qsch

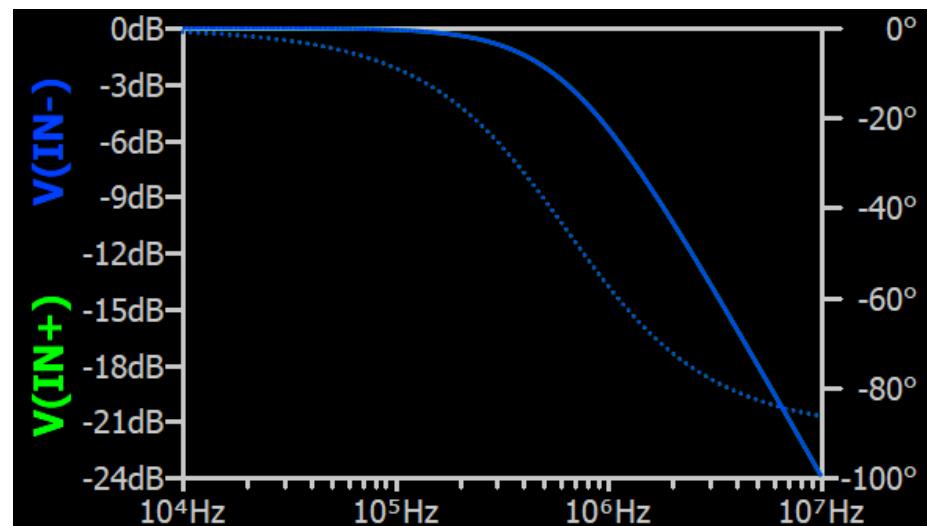
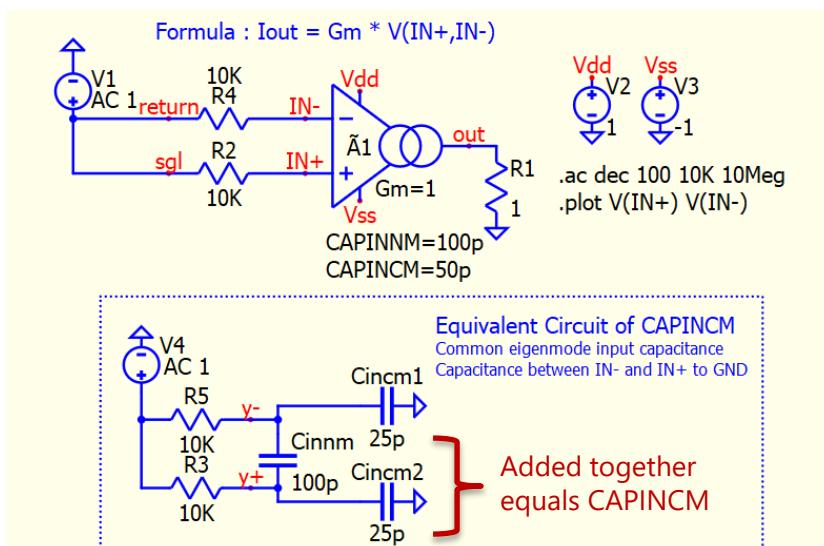
- CAPINNM : Normal eigenmode input capacitance
 - Default CAPINNM=0
 - This capacitance is equivalent between IN- and IN+



MULTGMAMP : Common eigenmode input capacitance (CAPINCM)

Qspice : Multgmamp - Capincm.qsch

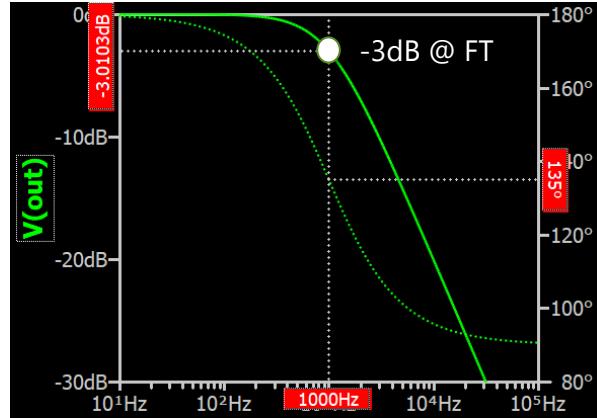
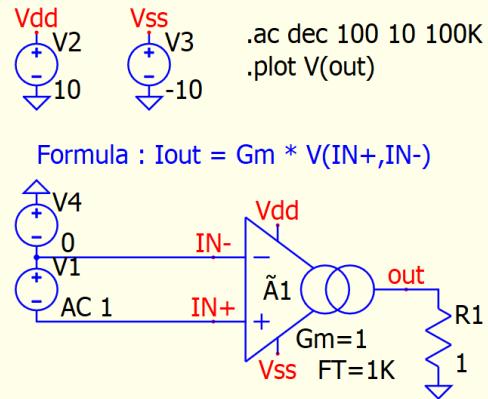
- CAPINCM : Common eigenmode input capacitance
 - Default CAPINCM=0
 - This capacitance is between IN- to GND and IN+ to GND



MULTGMAMP : FT 3dB Bandwidth

Qspice : Multgmamp - FT.qsch

- FT (3dB Bandwidth)
 - FT : 3dB bandwidth of transconductance with no voltages slewing
 - **Default FT=0** (i.e. infinite)

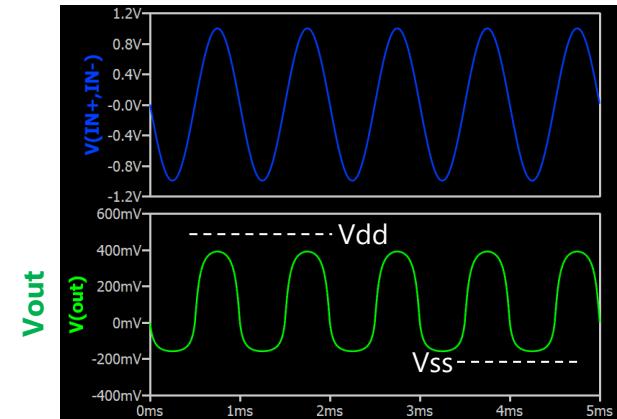
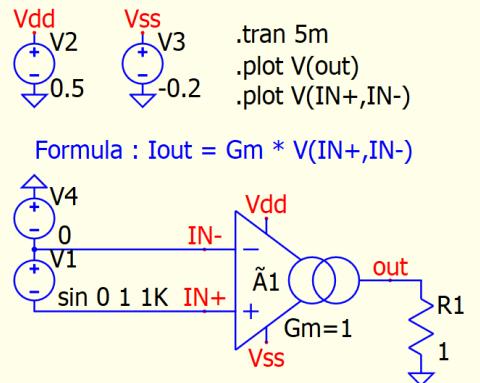


MULTGMAMP : Output Voltage Vdd, Vss and VDSAT

Qspice : Multgmamp - Vdd Vss.qsch ; Multgmamp - VDSAT.qsch

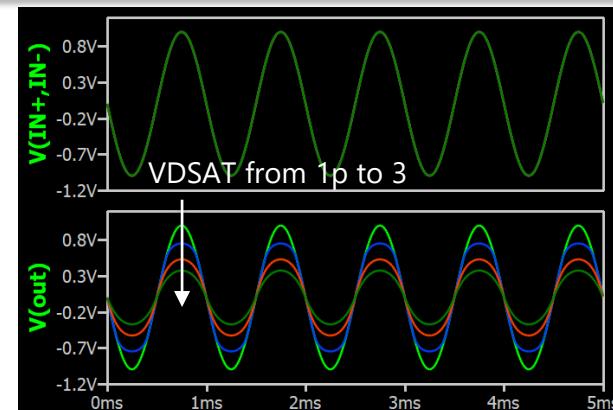
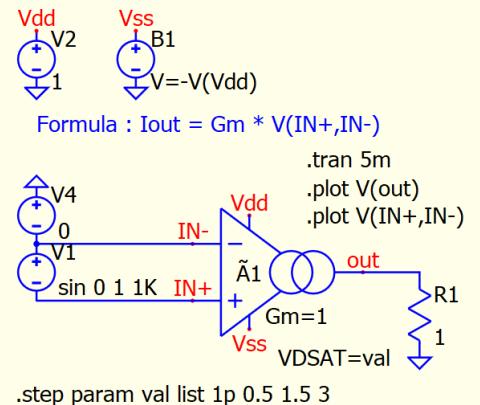
- Vdd and Vss Nets

- This is not parameters but Net 1 and Net 2 in \tilde{A} -Device
- Output voltage swing is limited by Vdd and Vss
- ** In this example, Vout cannot reach Vdd and Vss because a default VDSAT is set**



- VDSAT

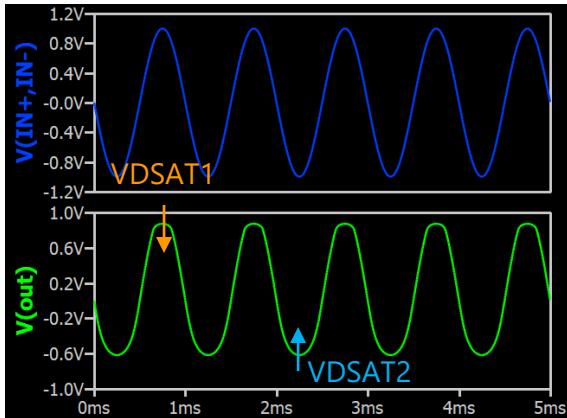
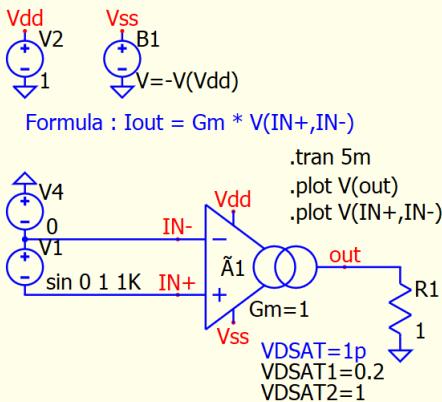
- V_{dsat} : Voltage where g_m starts to switch over to a resistance
- Default VDSAT = 0.5**
- VDSAT=0** forced its to default
- VDSAT=1p** for no saturation



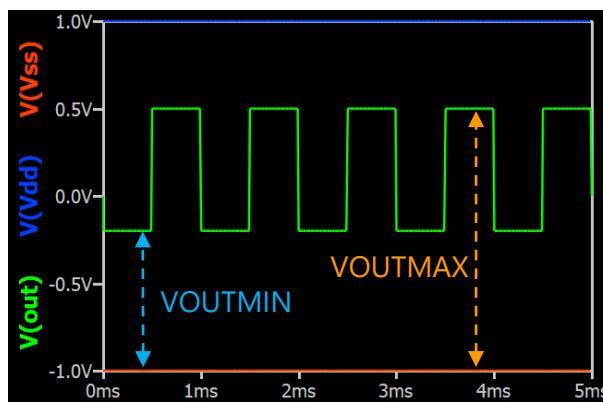
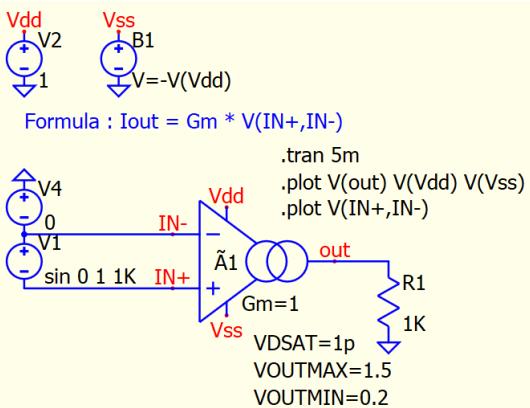
MULTGMAMP : Output Voltage VDSAT1, VDSAT2, VOUTMIN, VOUTMAX

Qspice : Multgmamp - VDSAT1 VDSAT2.qsch ; Multgmamp - VOUTMAX VOUTMIN.qsch

- VDSAT1 and VDSAT2
 - VDSAT1 : Voltage where gm starts to switch over to a resistance (top FET)
 - VDSAT2 : Voltage where gm starts to switch over to a resistance (bottom FET)
 - **Default VDSAT1=VDSAT**
 - **Default VDSAT2=VDSAT1**



- VOUTMIN and VOUTMAX
 - V_{outmin} : Minimum output voltage measured from negative rail
 - V_{outmax} : Maximum output voltage measured from negative rail

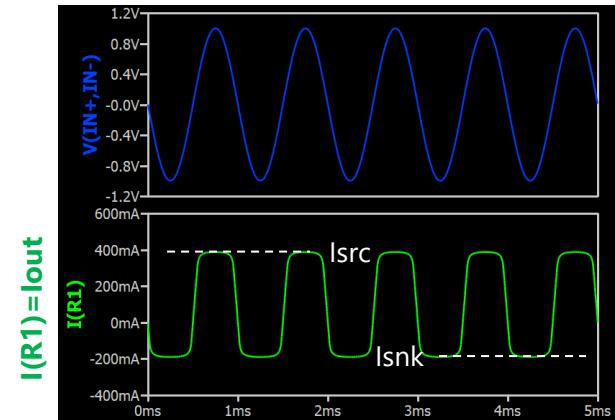
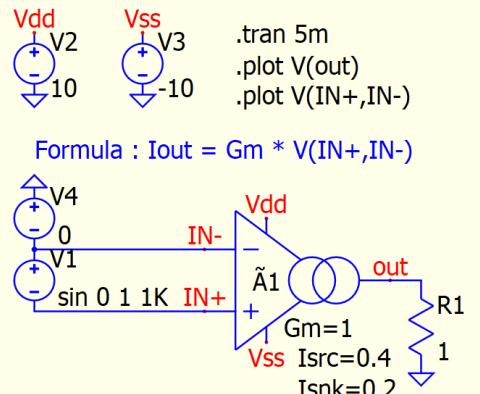


MULTGMAMP : Sink and Src Current (Iout / Isrc, Isnk)

Qspice : Multgmamp - ISRC ISNK.qsch ; Multgmamp - ISRCKNEE ISNKKNEE.qsch

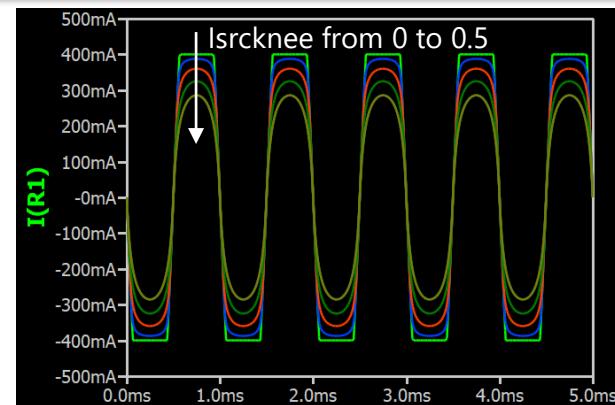
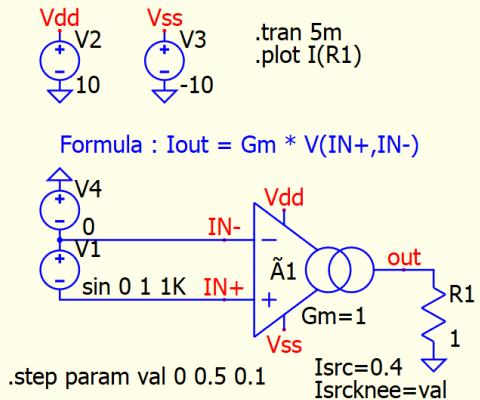
- IOUT/ISRC and ISNK

- Iout/Isrc : Maximum sourcing current (toward load)
- Isnk : Maximum sinking current (toward device)
- **Default ISRC = Infinite**
- **Default ISNK = IOUT or ISRC**
 - i.e. if ISNK not specified, ISNK equals IOUT or ISRC



- ISRCKNEE and ISNKKNEE

- Isrcknee : Sharpness of max sourcing current limit
- Isnkknee : Sharpness of Maximum sinking current limit
- **Default Isrckness = 0.1**
- **Default Isnkkness = Isrcknee**



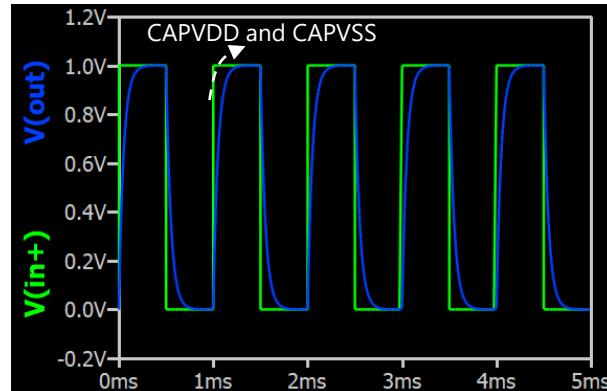
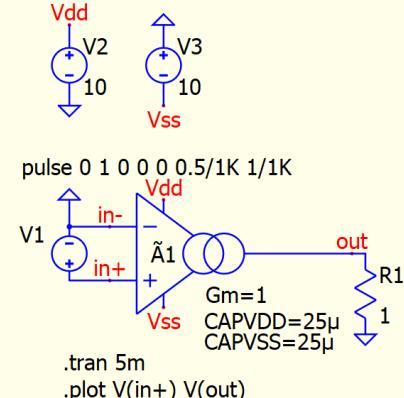
- Important Note

- To have effect, must defines ISRC or ISNK

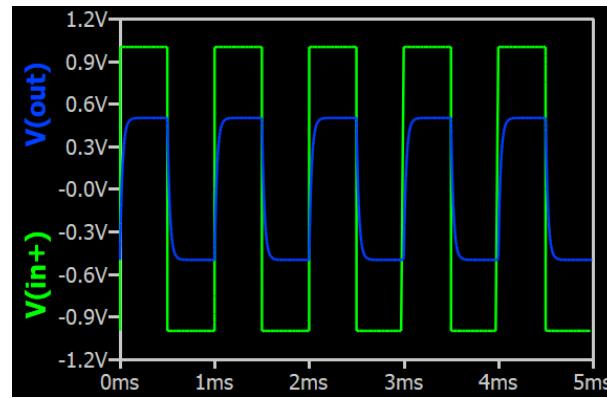
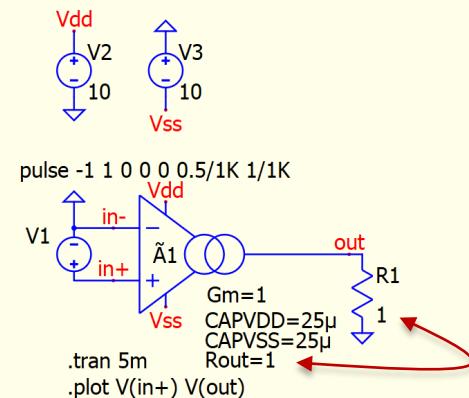
MULTGMAMP : Output Capacitance (CAPVDD, CAPVSS) and Resistance (Rout)

Qspice : Multgmamp - Capvdd Capvss.qsch ; Multgmamp - Rout.qsch

- CAPVDD and CAPVSS
 - CAPVDD : Capacitance from output to Vdd
 - Capvss : Capacitance from output to Vss



- **ROUT**
 - Rout : Additional impedance added to output(2*R to Vdd, 2*R to Vss)
 - In this example, Rout equal to amplifier loading, V(out) reduced by halve

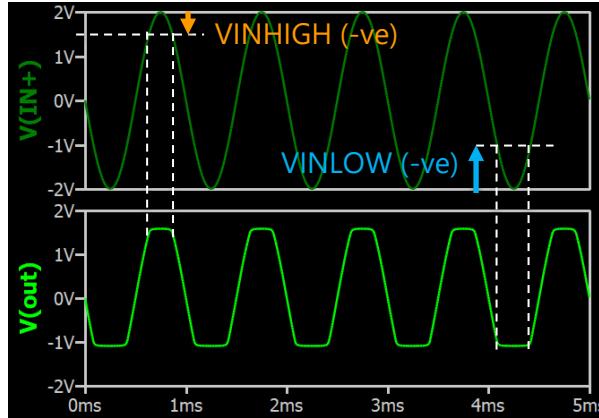
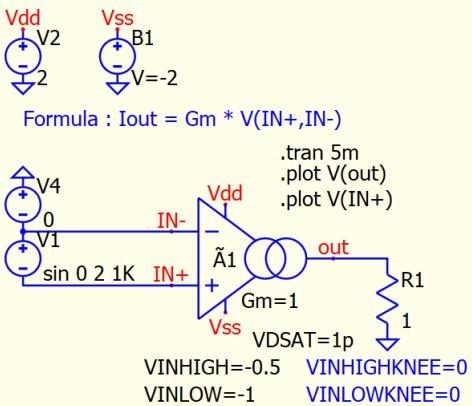


MULTGMAMP : Input Range VINLOW, VINHIGH, VINHIGHKNEE, VINLOWKNEE

Qspice : Multgmamp - VINHIGH VINLOW.qsch ; Multgmamp - VINHIGHKNEE VINLOWKNEE.qsch

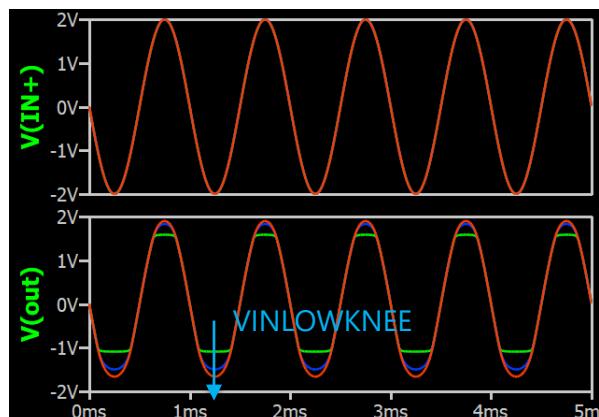
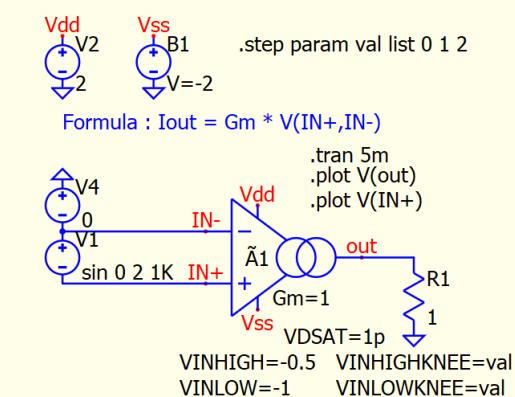
- VINLOW and VINHIGH**

- VINLOW : Input range measured from negative rail
- VINHIGH : Input range measured from positive rail
- Default VINLOW=0**
- Default VINHIGH=0**
- Value is negative**, which limit input range. For example, VINHIGH=-0.5, Input HIGH is limited to $Vdd + VINHIGH = 2 - 0.5 = 1.5$ in this example



- VINLOWKNEE**
VINHIGHKNEE

- Vinlowknee : Sharpness of negative input range limit
- Vinhightknee : Sharpness of positive input range limit
- Default VINHIGHKNEE=0**
- Default VINLOWKNEE=0**
- Increase KNEE soften the sharpness of input range, more output signal to come

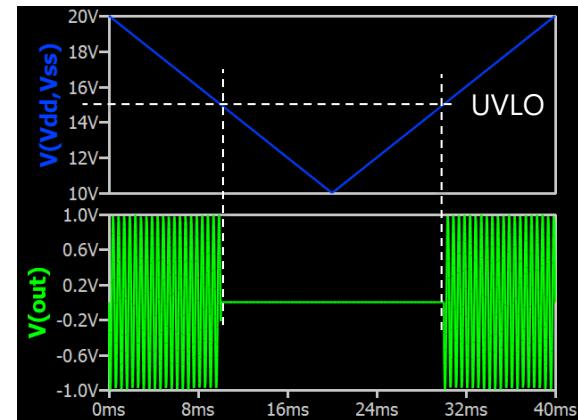
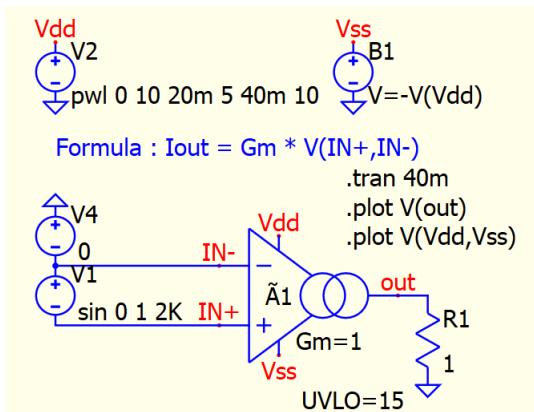


MULTGMAMP : UVLO and VOS1

Qspice : Multgmamp - UVLO.qsch ; Multgmamp - VOS1.qsch

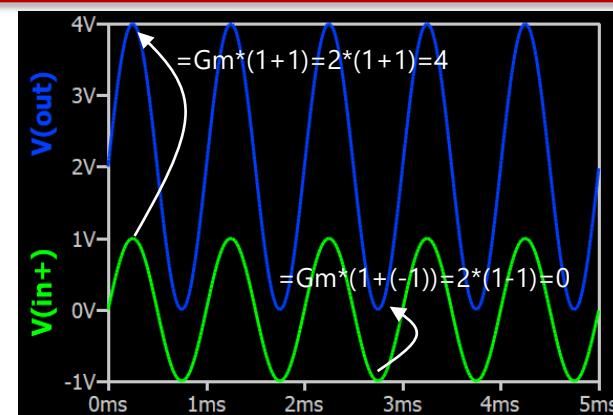
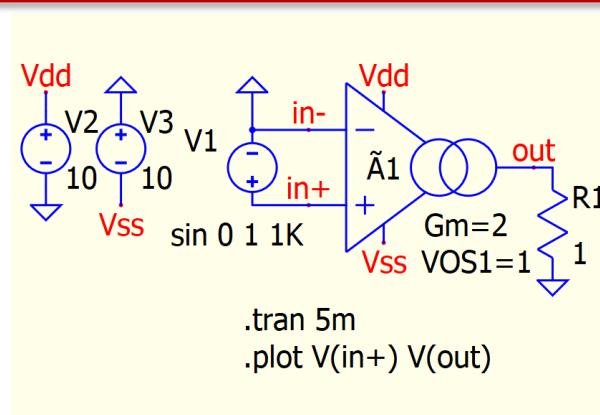
- UVLO

- UVLO : Under Voltage Lock Out - Minimum supply voltage
- Default UVLO is Infinite
- UVLO is compare to supply voltage = $V_{dd} - V_{ss}$



- VOS1

- VOS1 : Offset voltage for input
- $I_{out} = G_m * (VOS1 + V(IN+,IN-))$
 - This parameter is not in HELP formula, but it actually implemented
- Default VOS1 = 0



¥-Device

¥-Device

- ¥-Device
 - Syntax:

`¥nnn N1 N2 N3 N4 N5 N6 N7 N8 N9 N10 N11 N12 N13 N14 N15 N16 <TYPE> [INSTANCE PARAMETERS]`

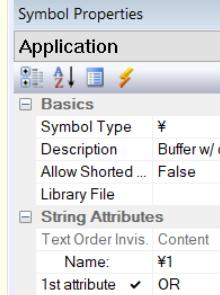
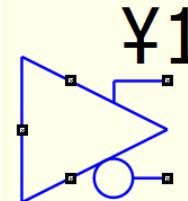
- The ¥-device supplies gate, flop, and a few other types of functional behaviors. The device expects exactly 16 pins, but not all are used. Unused pins must be specified connected to "¥".

¥-Device Types

TYPE	Behavior
AND	AND gate
CLOCKSYNC	Selects between a Sync and Clock inputs
D-FLOP	D-type flip-flop
EXTOSC	Oscillator programmed with an external resistor
HMITT	Schmitt trigger
JK-FLOP	JK-type flip-flop
MONOSTABLE	Retriggerable monostable
OR	OR gate
PS-FLOP	SMPS flip-flop
RS-FLOP	RS-type flip-flop
T-FLOP	Toggle flip-flop
XOR	XOR gate
Φ-DET	Phase/Frequency detector

To Identify what <TYPE> a symbol is

- In Symbol Properties > 1st attribute
- View > Netlist : from device syntax

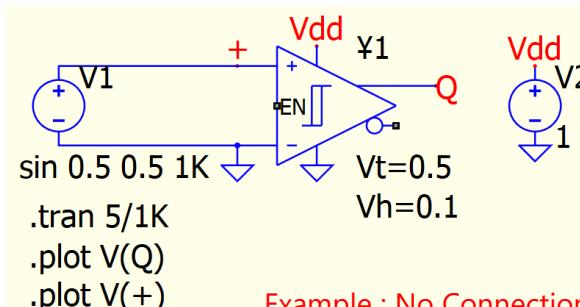


```
* C:\Users\kelvinleung\Documents\QSPICE\Unt
¥1 ¥0 ¥1 ¥2 ¥3 ¥4 ¥ ¥ ¥ ¥ ¥ ¥ ¥ ¥ ¥ ¥ ¥ ¥ OR
.end
```

¥-Device : How EN pin works

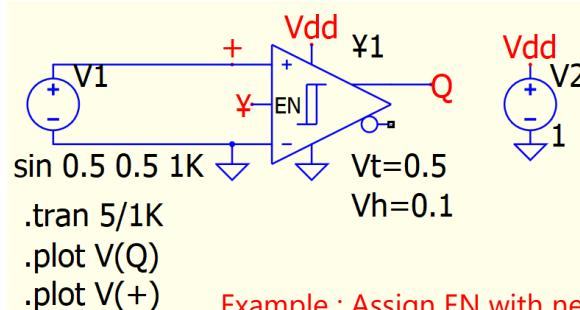
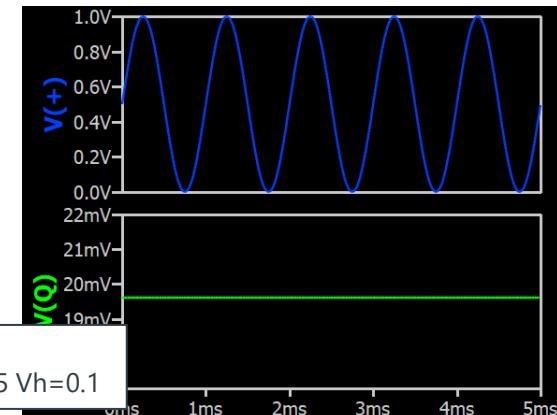
Qspice - Logic - EN.qsch

- How EN works
 - If EN is preset in symbol, normally, a signal is used to control its status. Here discuss two situations
 - #1 No connect to EN pin
 - Netlist assign ¥n as net name. EN pin is active to monitor EN signal. In this case, no output will generate
 - #2 Assign EN pin with net ¥
 - ¥ net name is equivalent to unassigned in ¥-device
 - Unassigned EN pin will be considered as Default ENABLE
 - Therefore, a symbol can be created with pin assigned to ¥ for their default



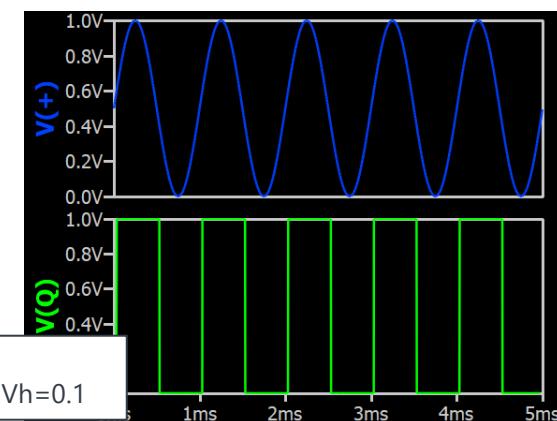
Example : No Connection

Netlist
¥1 Vdd 0 Q ¥0 + 0 ¥1 ¥ ¥ ¥ ¥ ¥ ¥ ¥ ¥ ¥ ¥ HMITT Vt=0.5 Vh=0.1



Example : Assign EN with net ¥

Netlist
¥1 Vdd 0 Q ¥0 + 0 ¥ ¥ ¥ ¥ ¥ ¥ ¥ ¥ ¥ ¥ ¥ HMITT Vt=0.5 Vh=0.1



¥-Device : HELP > Simulator > Device Reference > ¥-Device
 Common Instance Parameters (example from AND Gate Instance Param)

Name	Description	Units	Default
• CAPVDD	Capacitance from an output to Vdd	F	0.
• CAPVSS	Capacitance from an output to Vss	F	0.
IC	Initial condition(needed, e.g., for a ring osc)		
M	Number of parallel devices		1.
• REF	Logic reference voltage	V	$(Vdd + Vss) \div 2$
• RSINK	Resistance to Vss when output high	Ω	RSRC
• RSRC	Resistance to Vdd when output low(aka ROUT)	Ω	100.
• TD	Delay(aka TD1)	s	0.
• TD2	Asymmetrical delay	s	TD
TEMP	Instance temperature	$^{\circ}C$	27.
• TFALL	Fall time	s	0.
• TRISE	Rise time	s	0.
• TTOL	Temporal tolerance	s	$1\mu s$
• UVLO	Minimum Vdd-Vss voltage to operate	V	0.
ZMULT	Impedance multiplier when biased half way		1.

¥ Instance Params : REF Logic Reference Voltage

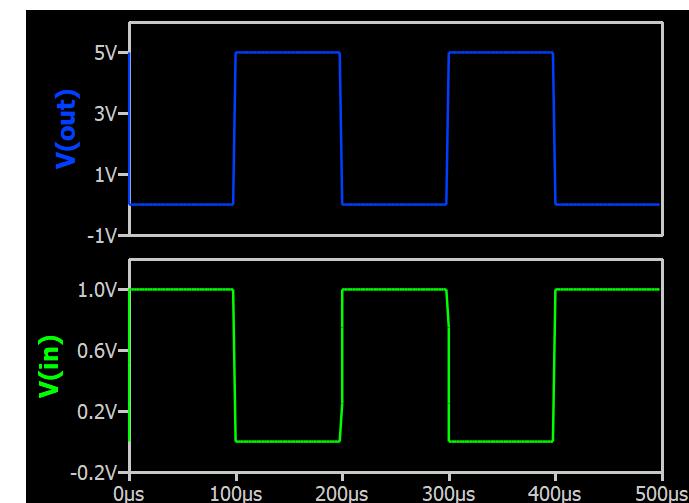
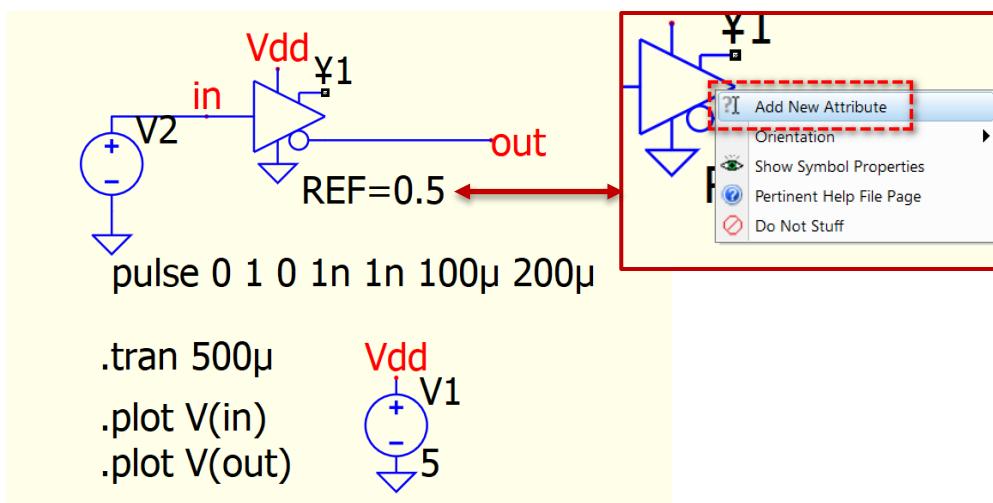
Qspice : Logic - REF.qsch

- REF : Logic reference voltage

- In default, ¥-Device logic threshold is $\frac{Vdd+Vss}{2}$

REF	Logic reference voltage	V	$(Vdd + Vss) \div 2$
-----	-------------------------	---	----------------------

- User can change logic threshold by [right click device] > [Add New Attribute] to add `REF=<value>`
- This example show logic output follows $Vdd/0$ with logic input threshold equal 0.5V to interface with 1V input logic

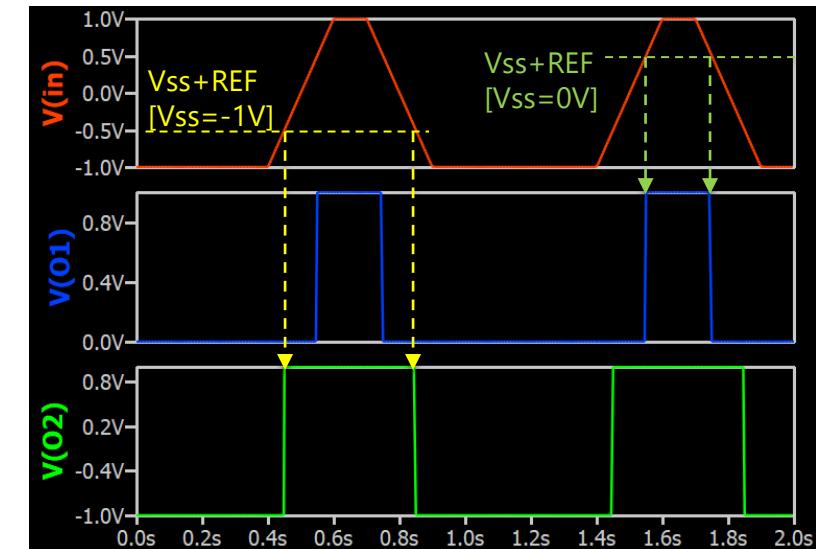
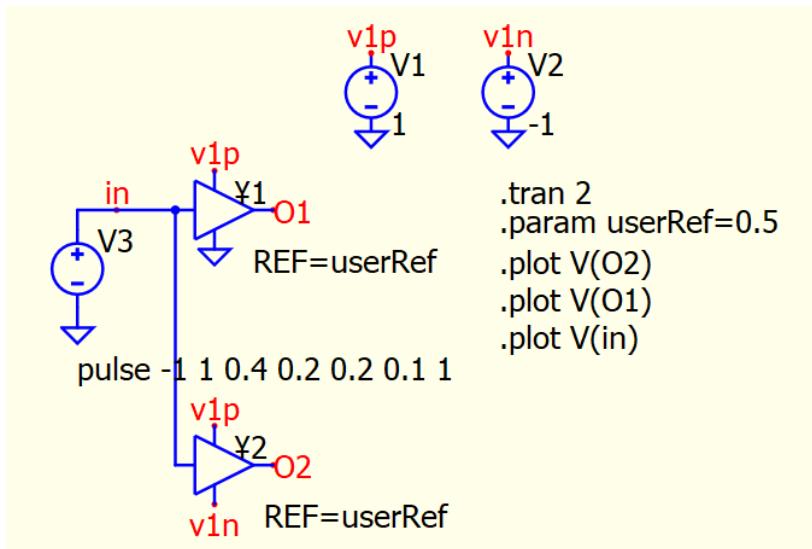


¥ Instance Params : REF Logic Reference Voltage

Qspice : Logic - REF (Dual Supply).qsch

- REF : Logic Reference Voltage

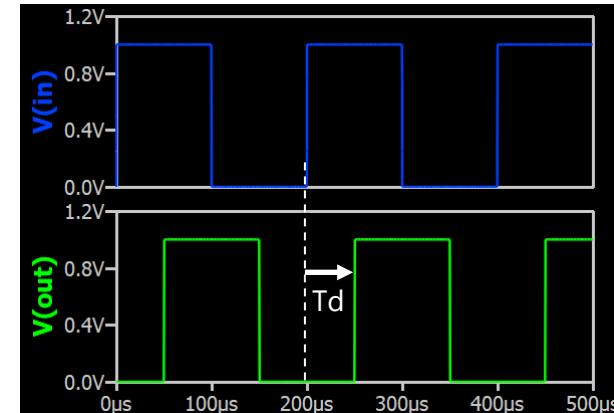
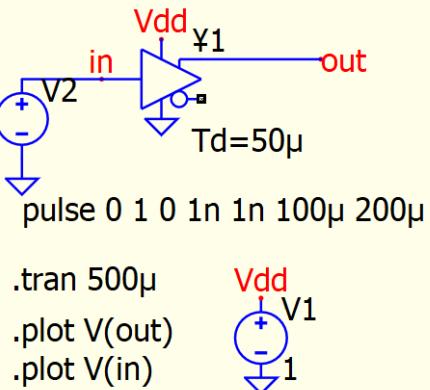
- REF is not absolute voltage to node 0, but reference to Vss node of ¥-Device
- In this example, ¥1 and ¥2 are with same REF value, but as ¥1 Vss=0V and ¥2 Vss=-1V, their logic reference is different reference to node 0 (GND). Therefore, even their input is same, their output can be different



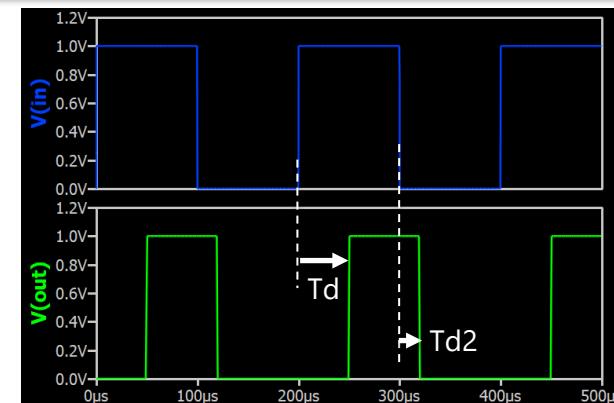
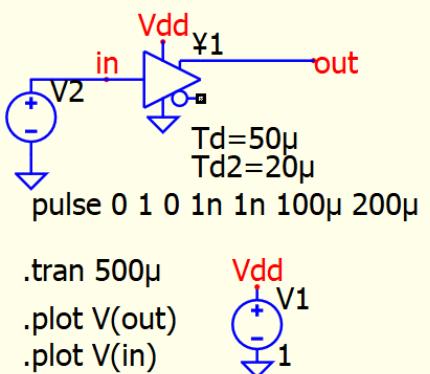
Instance Params : Delay (TD) and Asymmetrical Delay (TD2)

Qspice : Logic - Td.qsch ; Logic - Td Td2.qsch

- TD (Delay)
 - Default is 0s
 - ** If TD2 is not set, both rising and falling delay times are same
 - ** If TD > logic H duration or delay TD2 > logic L duration, output always LOW or HIGH



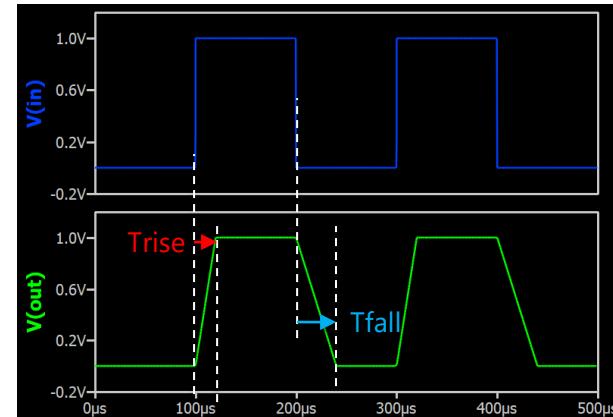
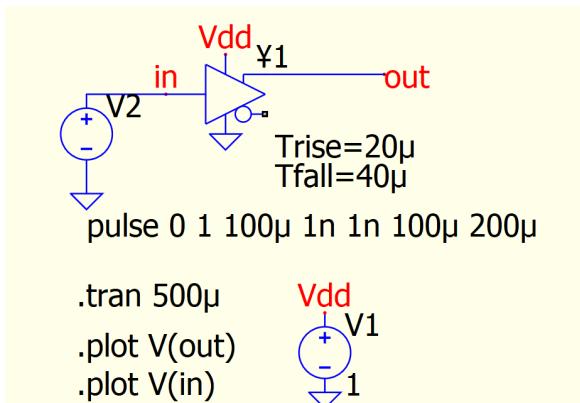
- TD2 (Asymmetrical delay)
 - Default set equal to TD
 - If different delay times for rising and falling edge, set TD2 for falling edge delay time
(i.e. TD only control rising edge delay time)



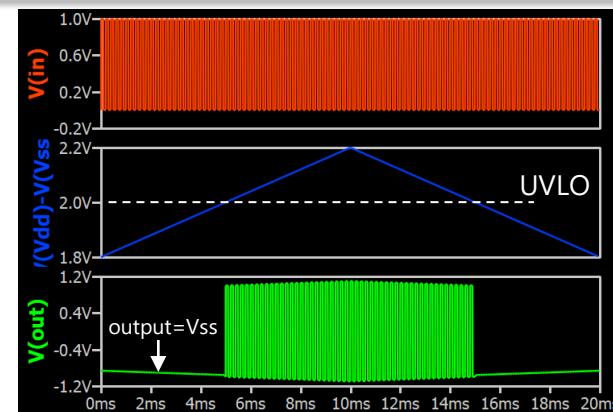
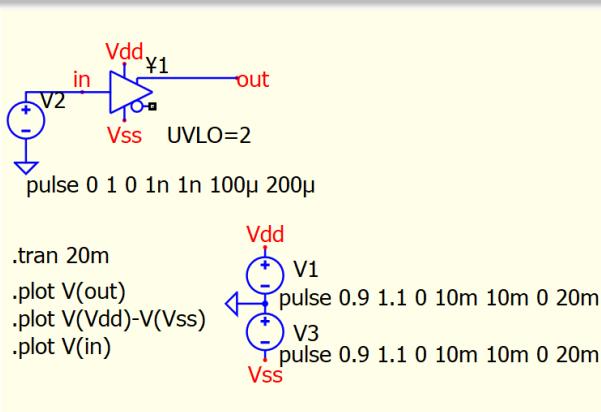
Instance Params : Rise time (Trise), Fall time (Tfall) and UVLO

Qspice : Logic - Trise Tfall.qsch

- TRISE and TFALL
 - Trise : Rise time
 - Tfall : Fall time



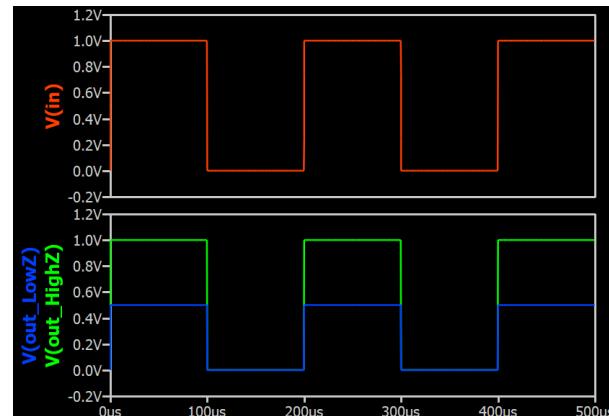
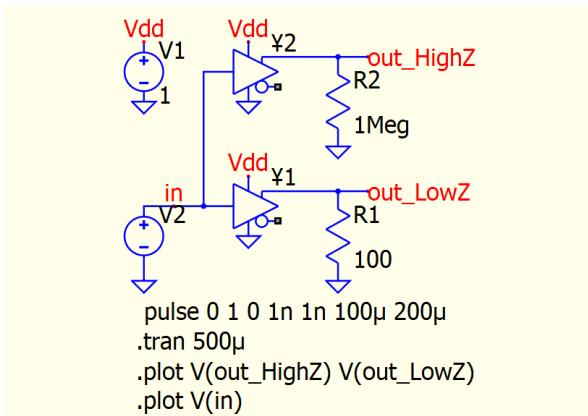
- UVLO
 - Under Voltage Lock Out UVLO
 - UVLO : Minimum $V_{dd}-V_{ss}$ voltage to operate
 - Output only enabled when $V_{dd}-V_{ss} > \text{UVLO}$
 - Output equals V_{ss} when gate disable



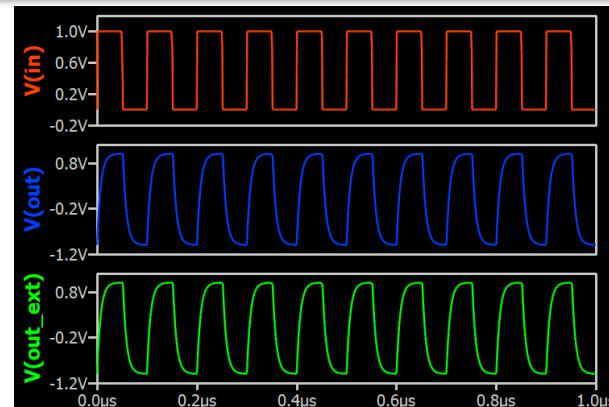
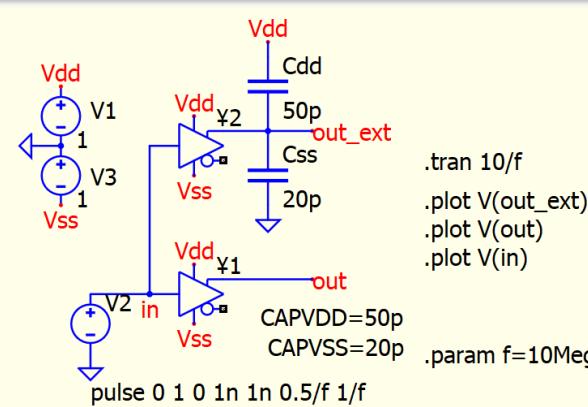
Instance Params : Output R and C (Rsink, Rsrc, Capvdd, CapVss)

Qspice : Logic - RSINK RSRC.qsch ; Logic - Capvdd Capvss.qsch

- RSINK and RSRC
 - RSINK : Res to Vss when o/p high
 - RSRC : Res to Vdd when o/p low
 - Default both are 100 ohms
- Example
 - This simulation shows loading effect when output to a 100 ohms, where o/p level is reduced to half of Vdd



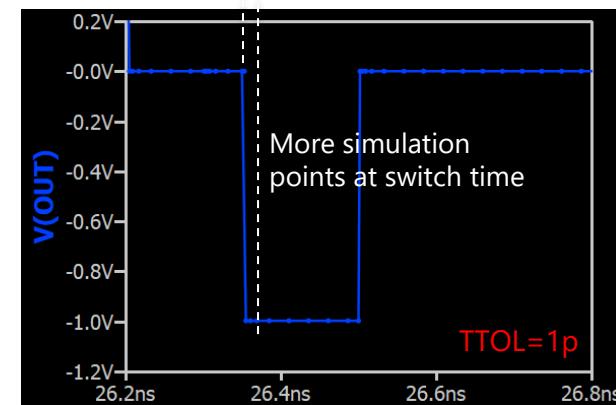
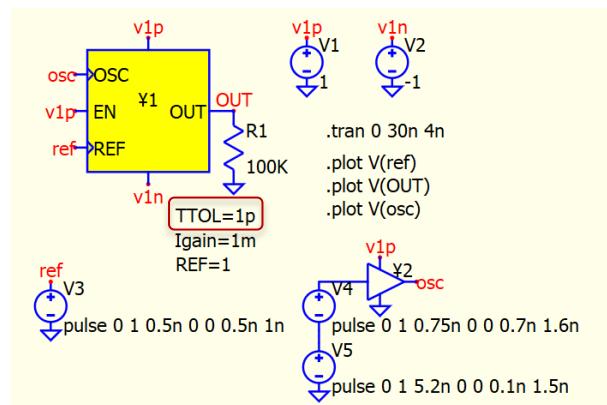
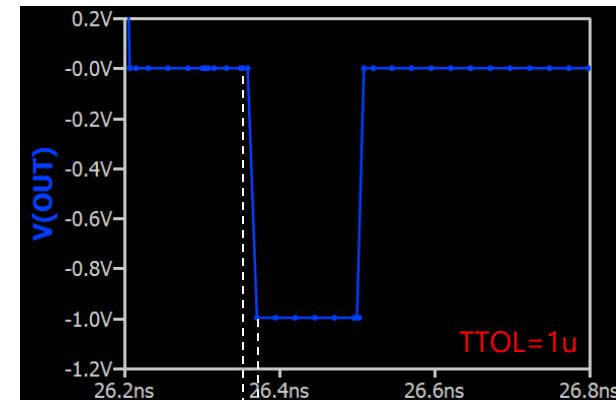
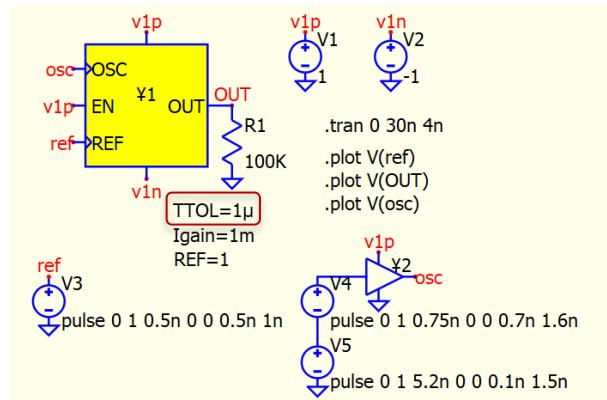
- CAPVDD, CAPVSS
 - Capvdd : Capacitance from an output to Vdd
 - Capvss : Capacitance from an output to Vss
- Explanation
 - Capacitance Capvdd/Capvss equivalent Cdd/Css this example
 - This demo can have frequency response because Rsink=Rsrc=100 internally



Instance Params : TTOL Temporal Tolerance

Qspice : Logic - TTOL.qsch

- TTOL
 - Ttol : Temporal tolerance
 - Default TTOL=1u**
 - TTOL allows one to determine how accurately the switch time should be found

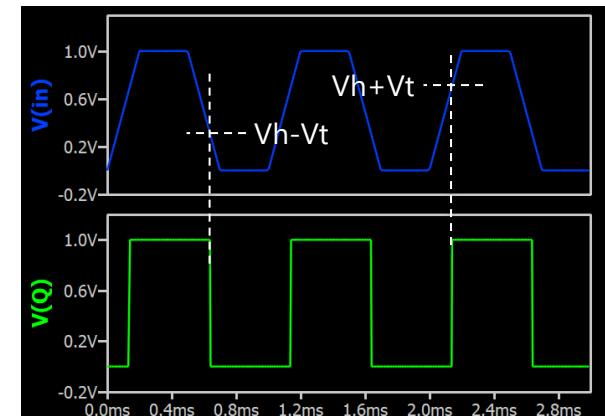
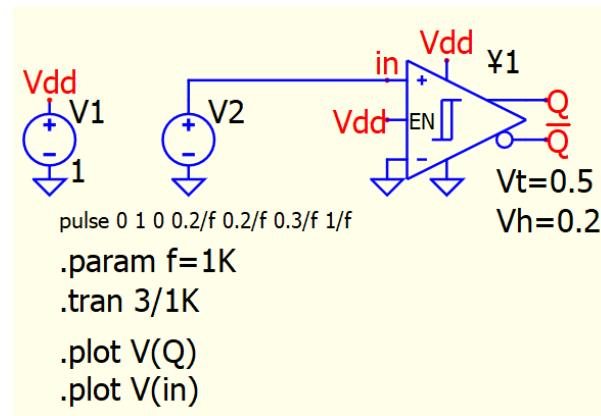


⌘ [HMITT] Instance Params : Threshold (VT) and Half Hysteresis (VH)

Qspice : HMITT - Vt VH.qsch

- VT and VH

- Vt : Threshold voltage
- VH : Half hysteresis voltage
- HMITT is schmitt trigger logic input
- low trip point is $Vt-VH$ and the high trippoint is $Vt+VH$



¥ Truth Table : AND, OR, XOR

Qspice : Truth Table of AND OR XOR.qsch

- AND

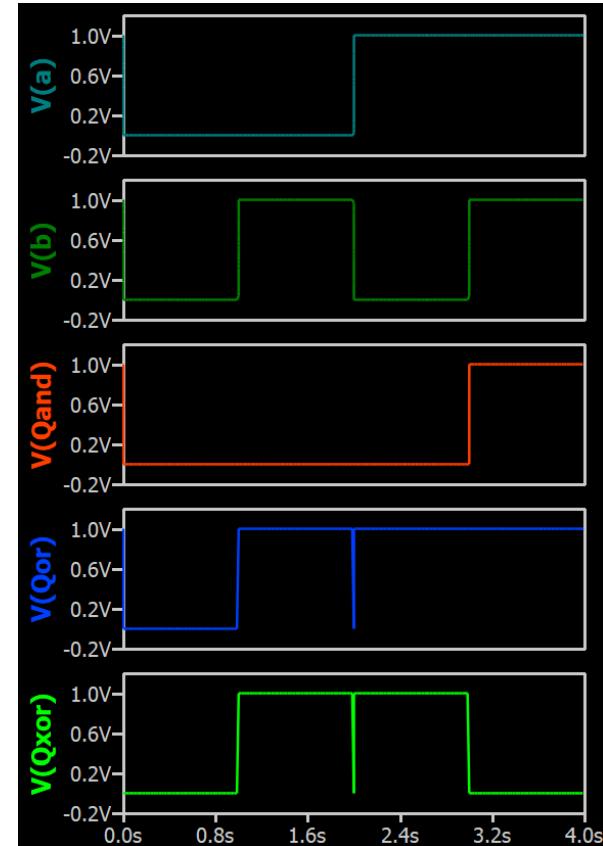
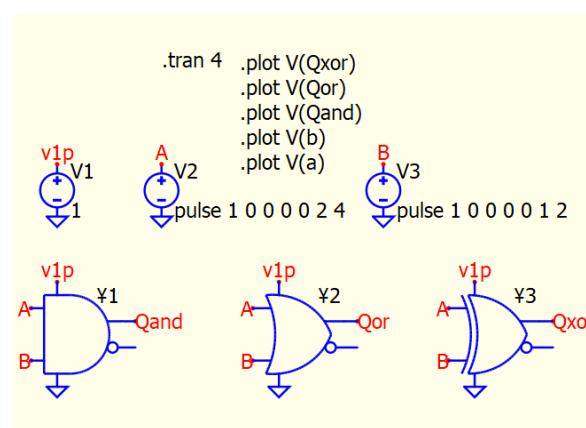
¥-Device AND			
A	B	Q	_Q
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

- OR

¥-Device OR			
A	B	Q	_Q
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

- XOR

¥-Device XOR			
A	B	Q	_Q
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1



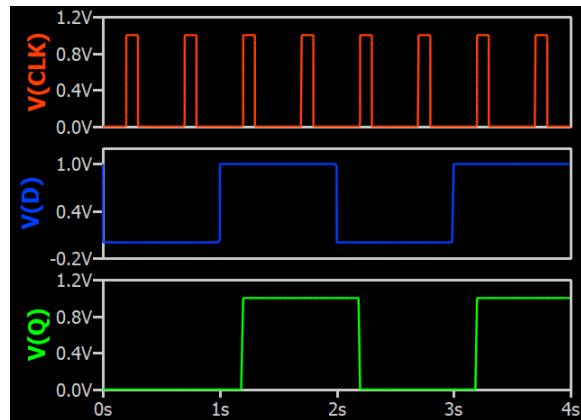
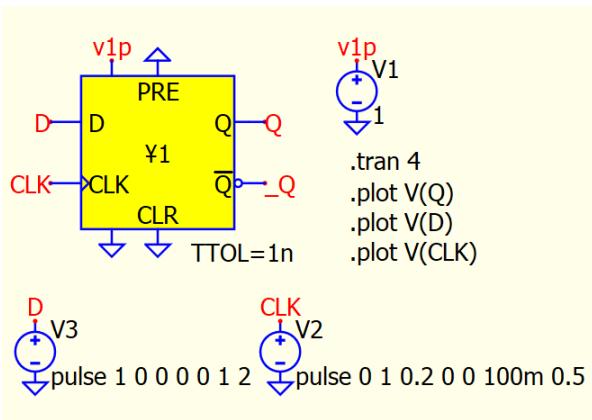
¥ Truth Table : D-FLOP and T-FLOP

Qspice : Truth Table of D-FLOP.qsch ; Truth Table of T-FLOP.qsch

- D-FLOP

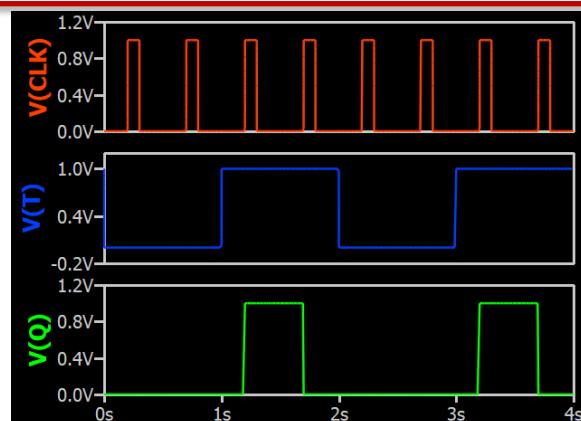
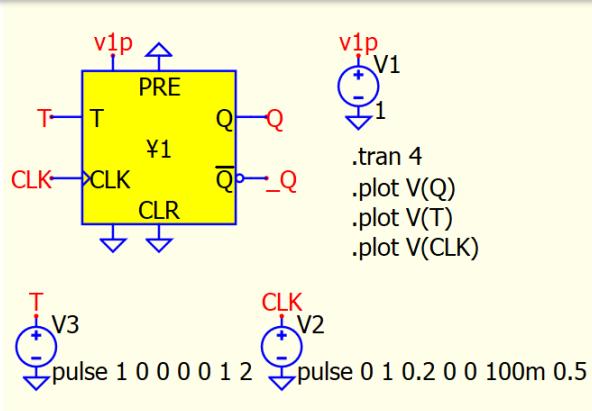
- PRE : Active High (=SET)
- CLR : Active High (=RESET)

¥-Device D-flop					
CLK	D	PRE	CLR	Q	\bar{Q}
↑	0	0	0	0	1
↑	1	0	0	1	0
x	x	0	0	Q	\bar{Q}
x	x	1	0	1	0
x	x	x	1	0	1



- T-FLOP

¥-Device T-flop				
CLK	T	PRE	CLR	Q_{n+1}
↑	0	0	0	0
↑	1	0	0	\bar{Q}_n
x	x	0	0	Q
x	x	1	0	1
x	x	x	1	0

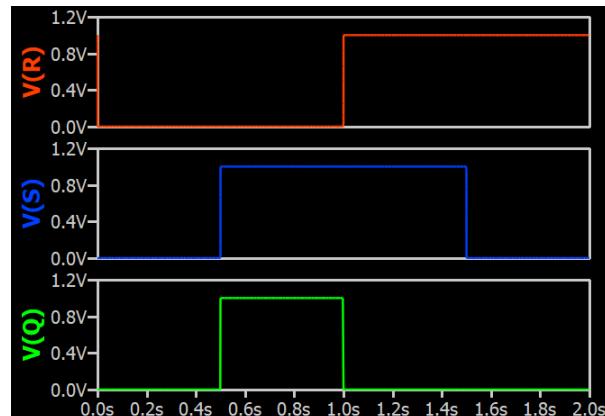
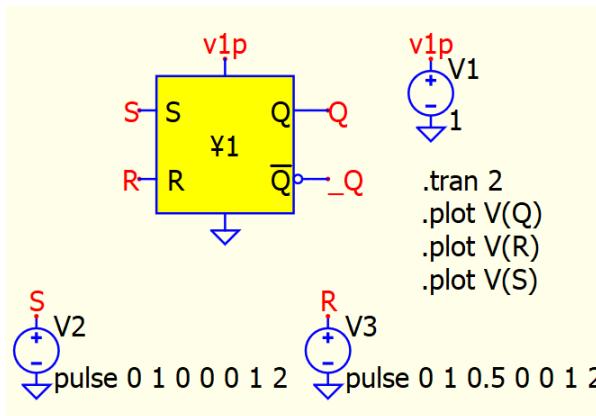


¥ Truth Table : SR-FLOP and JK-FLOP

Qspice : Truth Table of SR-FLOP.qsch ; Truth Table of JK-FLOP.qsch

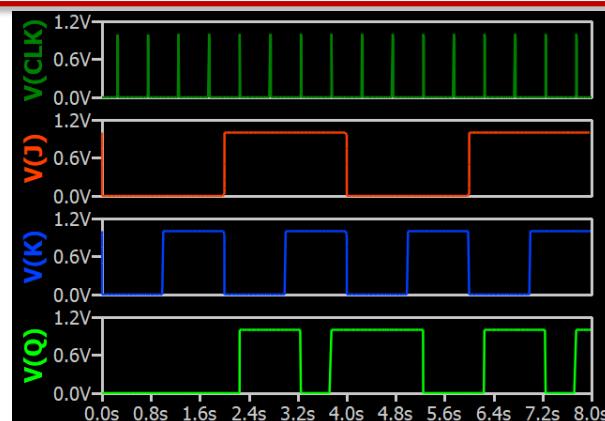
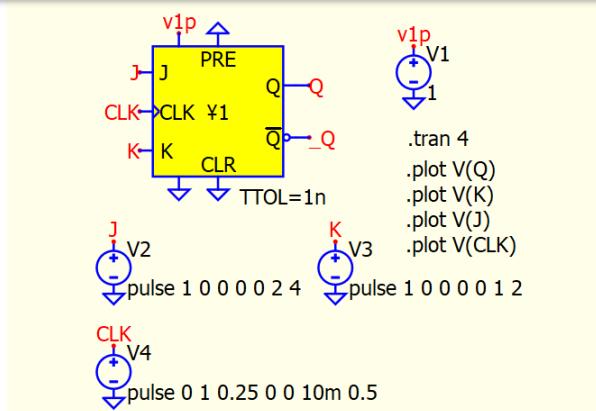
- SR-FLOP

R	S	Q	\bar{Q}
0	0	0	1
0	1	1	0
1	x	0	1



- JK-FLOP

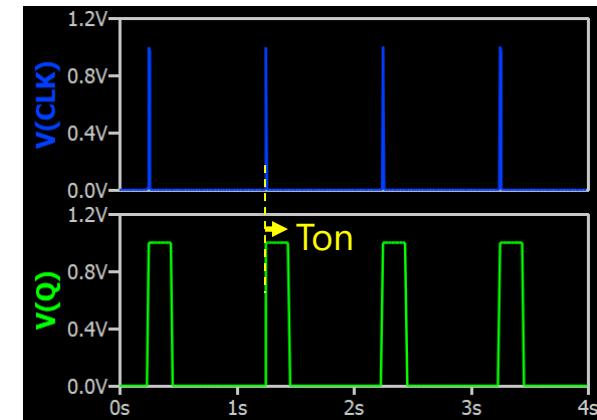
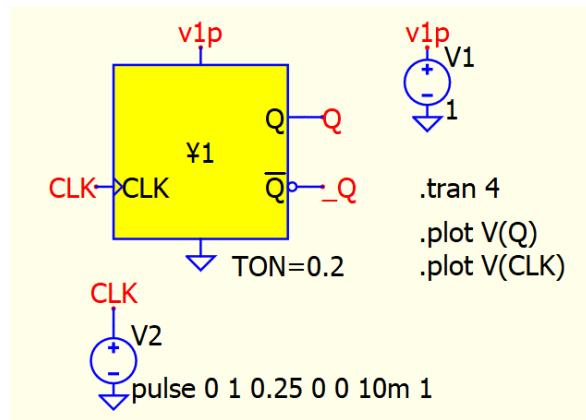
CLK	J	K	PRE	CLR	Q_{n+1}
↑	0	0	0	0	Q_n
↑	0	1	0	0	0
↑	1	0	0	0	1
↑	1	1	0	0	\bar{Q}_n
x	x	x	0	0	Q
x	x	x	1	0	1
x	x	x	x	1	0



¥-Device Monostable

Qspice : Usage - Monostable.qsch

- Monostable
 - TON must be specified to use Monostable
 - CLK trigger a minimum on-time pulse



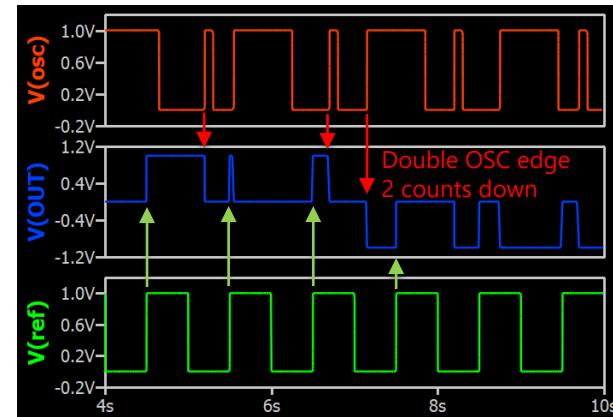
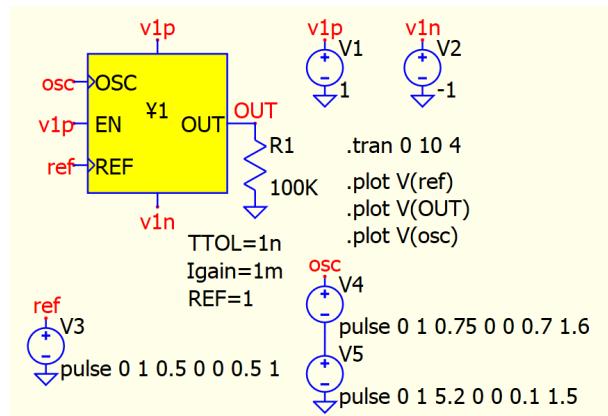
¥ Truth Table : Φ -DET (Phi-Det) [Symbol : PhaseDetector in analog]

Qspice : Truth Table of Phi-Det.qsch

- Φ -DET (Phi-Det)
 - Phase/Frequency Detector

¥-Device Phi-Det		
REF	OSC	OUT
↑	x	Up
x	↑	Down
↑	↑	Unchange

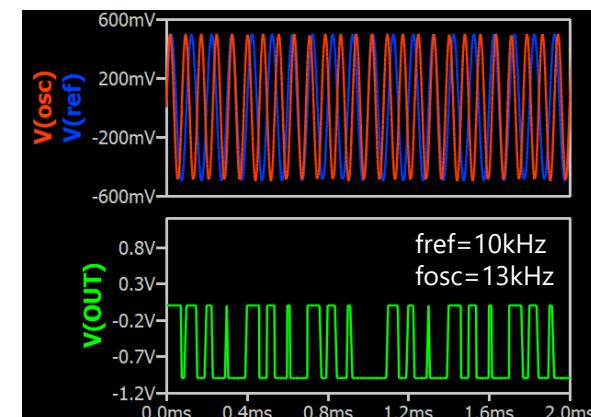
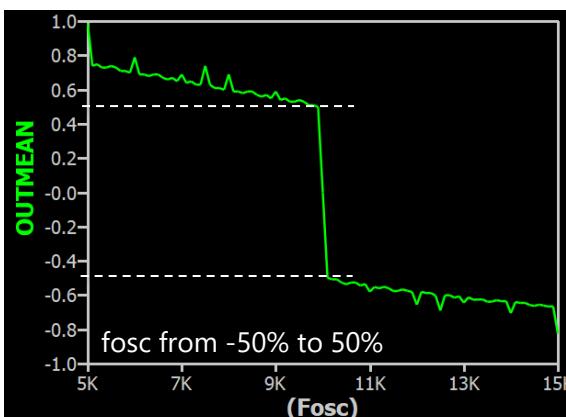
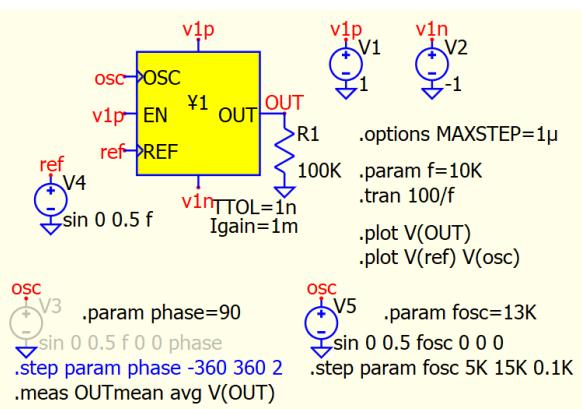
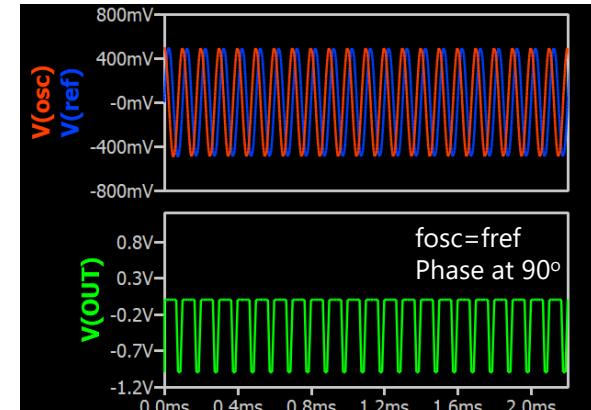
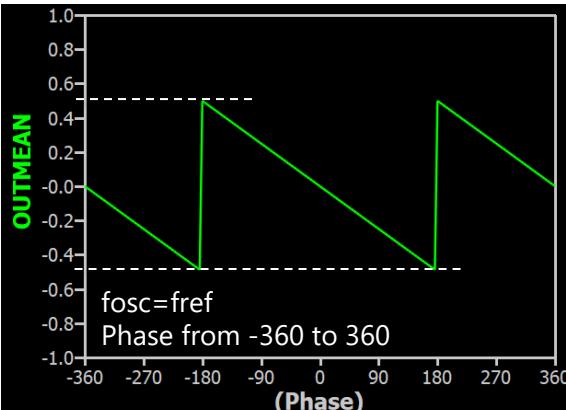
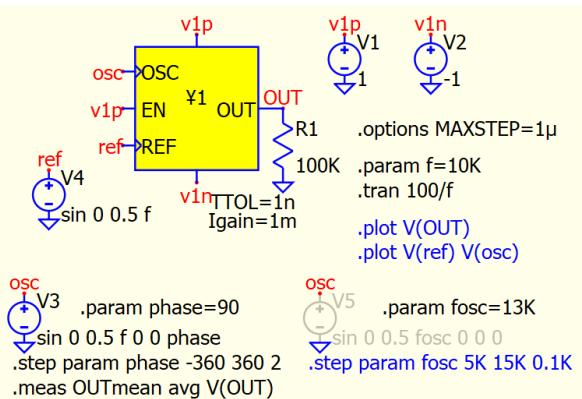
- Important
 - Output is current, not voltage
 - Suggest to set a higher Igain for OUT can reach Vdd/Vss with load (Default Igain only 10µA)
 - This device is a [Vdd, 0, Vss] 3-state counter, therefore, must operate with dual supply
 - REF edge counts up
 - OSC edge counts down



- Phase/Frequency Detection
 - Next slide is simulation results in phase change and frequency change
 - Mean of PWM output pattern can differentiate it is OSC signal phase or frequency deviate from REF signal
 - This is a key component in Phase Lock Loop (PLL)

¥-Device Φ -DET (Phi-Det) : OSC and REF Relationship with OUT

Qspice : Usage - Phi-Det (Freq and Phase).qsch

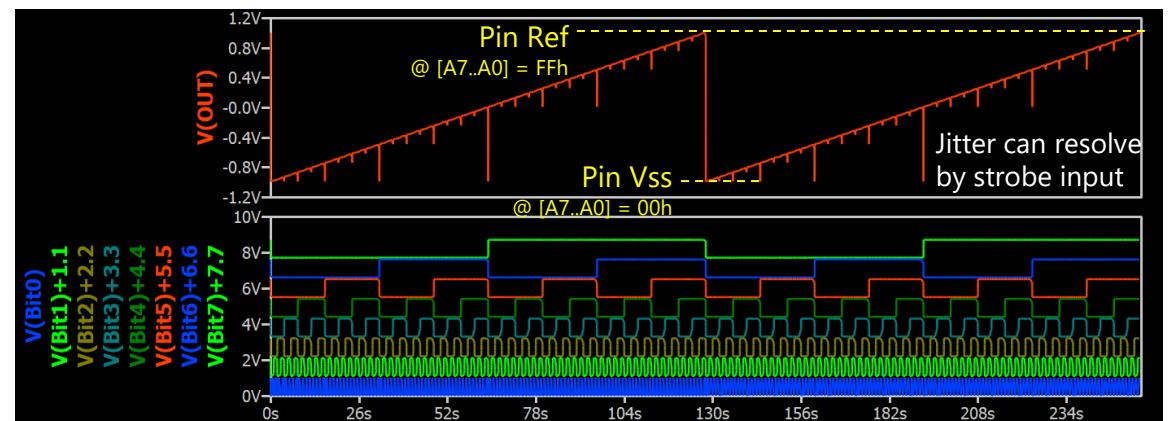
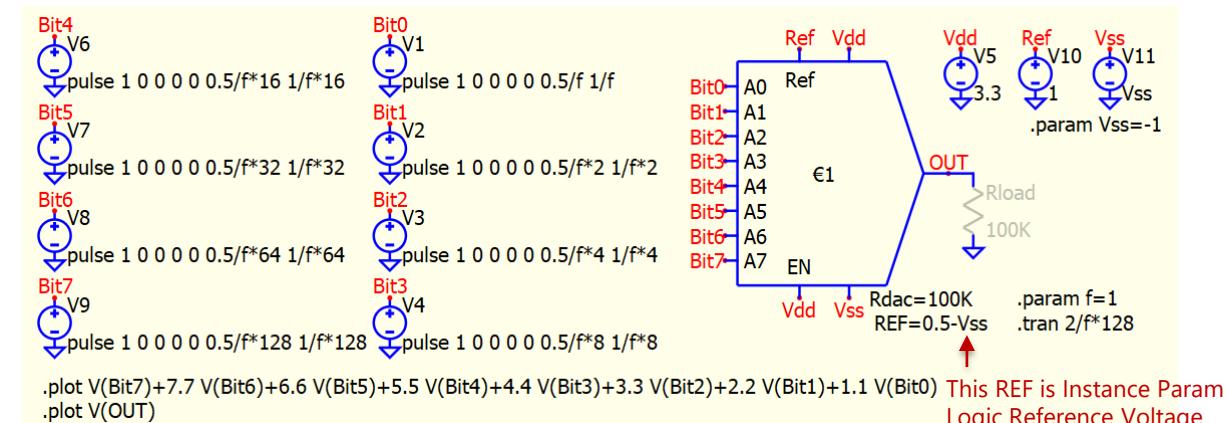


ϵ -Device

€-Device DAC : Build-in Symbol DAC8.qsym

Qspice : DAC - Basic.qsch

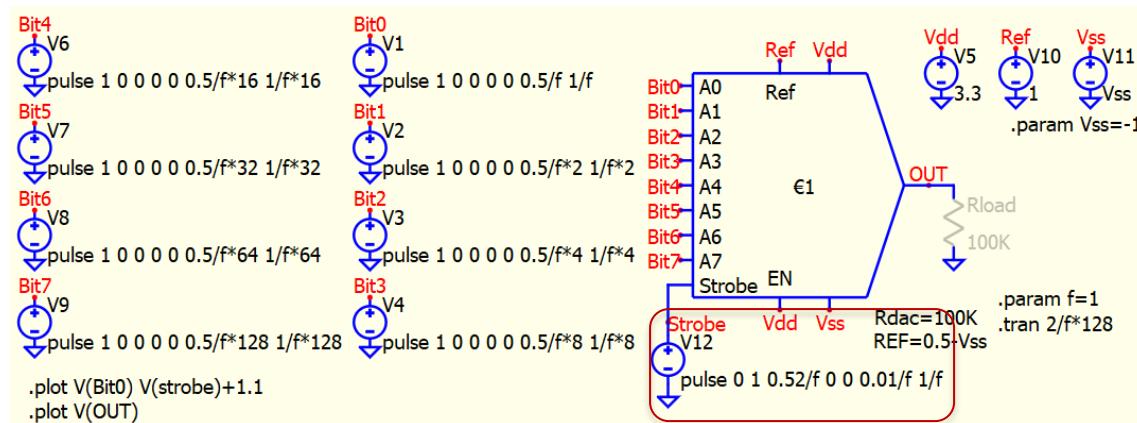
- DAC
 - DAC : Digital to Analog Converter
- Important Pins
 - Ref : the maximum voltage value that the DAC can reach
 - A7 : MSB of input word A
 - A0 : LSB of input word A
 - EN : Enable
- Instance Params
 - Common instance params can refer to €-Device section (e.g. REF)



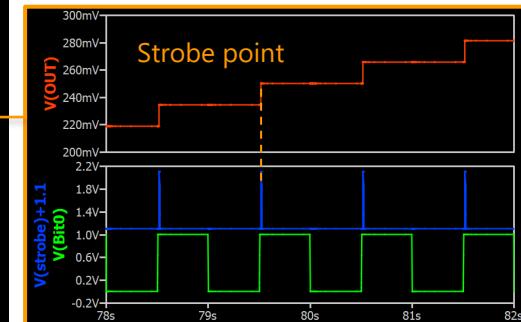
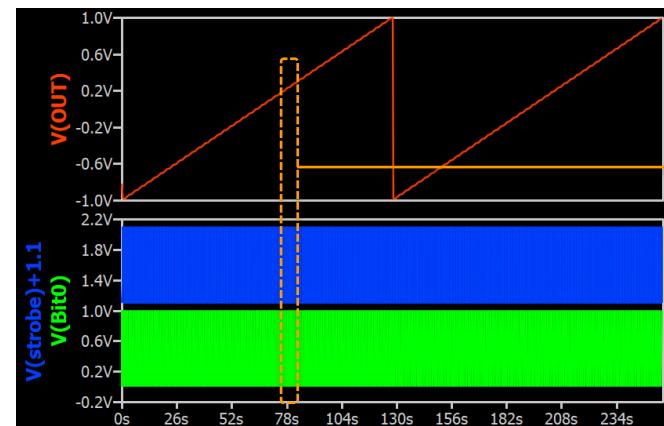
€-Device DAC : Build-in Symbol DAC8strobe.qsym

Qspice : DAC - Strobe.qsch

- Strobe
 - In practice, it named as load DAC strobe (LDAC)
 - This pin transfers all input register data to the DAC registers
 - It resolve jitter in V(out) in previous slide



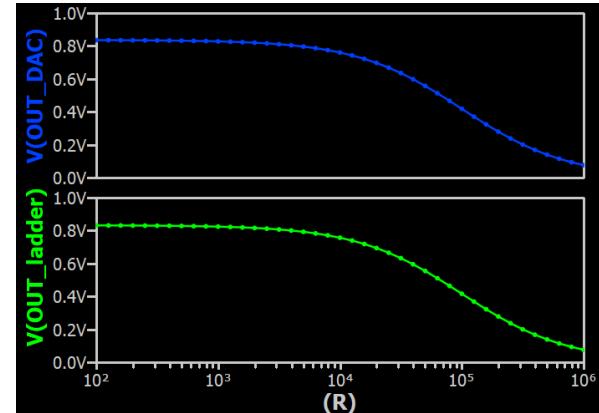
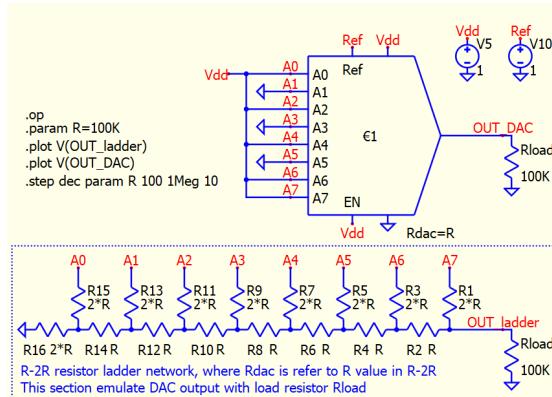
- Symbol
 - Build-in symbol with strobe is
 - DAC8strobe.qsym



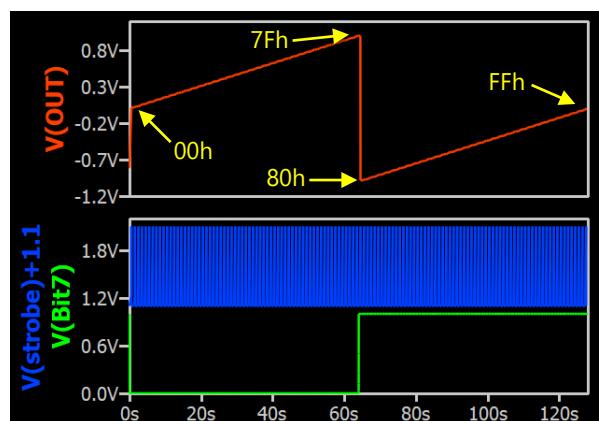
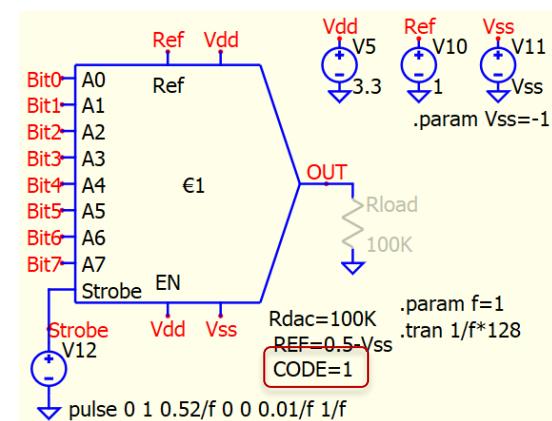
€-Device DAC Instance Params : RDAC

Qspice : DAC - RDAC.qsch ; DAC - CODE.qsch

- RDAC
 - Rdac : R of R-2R DAC
 - R-2R resistor ladder network is inexpensive solution for digital to analog conversion
 - Reference
 - https://en.wikipedia.org/wiki/Resist_ladder
 - Therefore, to prevent loading effect, a voltage buffer should be used in DAC output



- CODE
 - Code : Non-zero maps from -n to n-1 to 0 to 2n-1
 - Default CODE=0**
 - CODE=0 : Unsigned
 - CODE=1 : Signed - two's complement

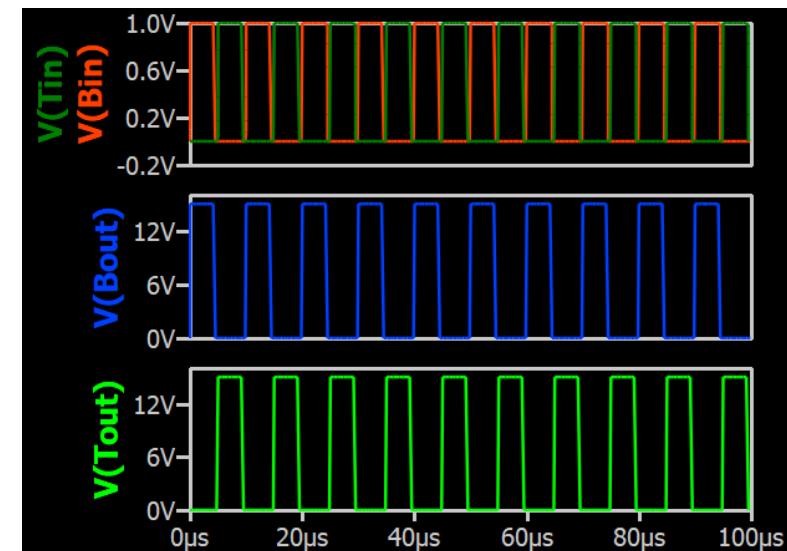
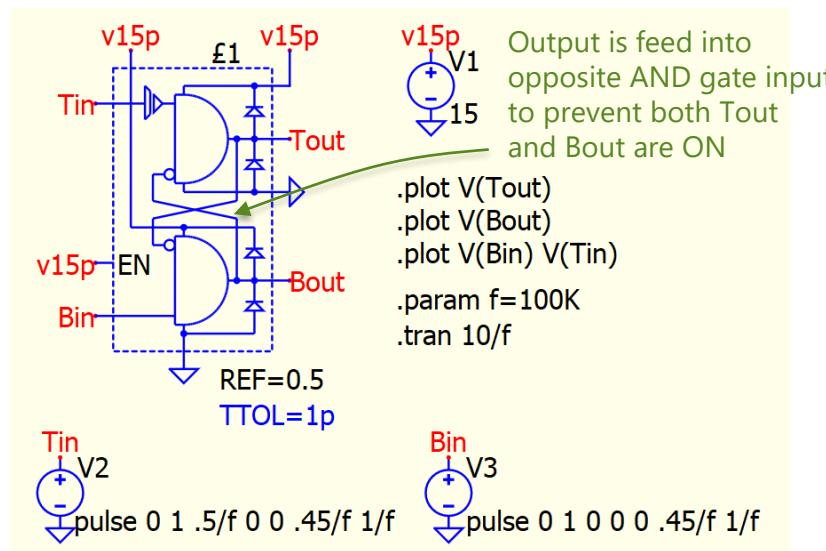


f -Device

f-Device : Dual Gate Driver

Qspice : Dual Gate Driver.qsch

- f-Device Dual Gate Driver
 - Syntax: fnnn Vdd Vss BOOST TOPGATE SW BOTGATE TCTRL BCTRL EN ¥ ¥ ¥ ... GATEDRIVER [INSTANCE PARAMETERS]
 - This behavioral device expects Top Input and Bottom Input has deadtime in between



£ [Dual Gate Driver] Instance Params

Gate Driver Instance Parameters

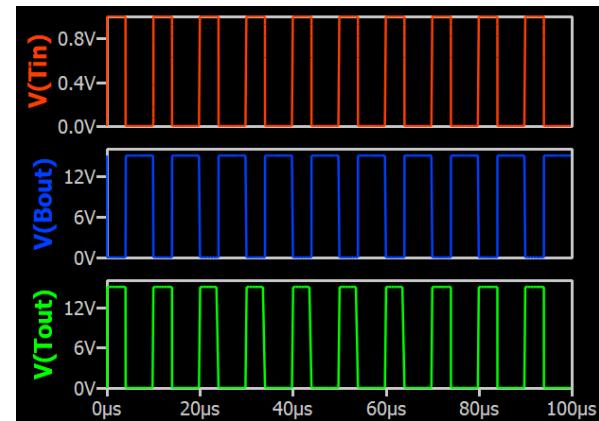
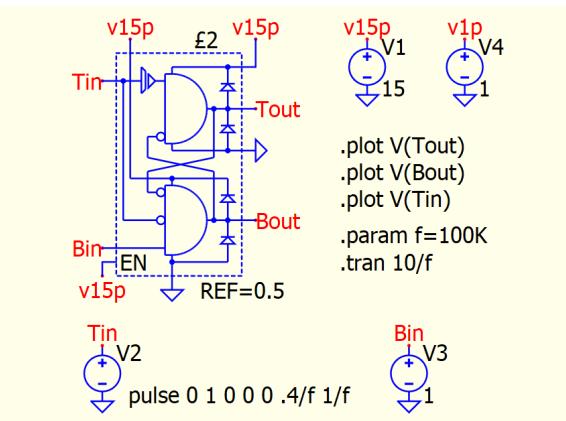
Name	Description	Units	Default
BOOST	Add logic such that the top FET is off if the bottom is controlled to be on		(not set)
BUCK	Add logic such that the bottom FET is off if the top is controlled to be on		(not set)
CAPVDD	Capacitance from a logic output to Vdd(or BOOST)	F	0.
CAPVSS	Capacitance from a logic output to Vss(or SW)	F	0.
M	Number of parallel devices		1.
REF	Logic reference for enable input	V	$(Vdd + Vss) \div 2$
ROFF1	Resistance used to pull bottom FET to VSS	Ω	RON1
RON1	Resistance used to pull bottom FET to VDD	Ω	1.
ROFF2	Resistance used to pull top FET to SW	Ω	ROFF
RON2	Resistance used to pull top FET to BOOST	Ω	RON1
RPASSIVE	Resistance used to pull both FETs' gates low when the driver is not enabled	Ω	1Meg
TEMP	Instance temperature	$^{\circ}C$	27.
TTOL	Temporal tolerance	s	
UVLO	Minimum Vdd-Vss voltage to operate	V	2.

£ [Dual Gate Driver] Instance Params - Buck and Boost

Qspice : Dual Gate Driver (Buck).qsch; Dual Gate Driver (Boost).qsch

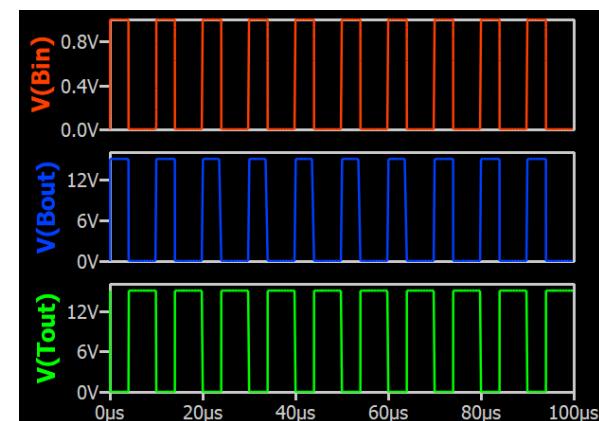
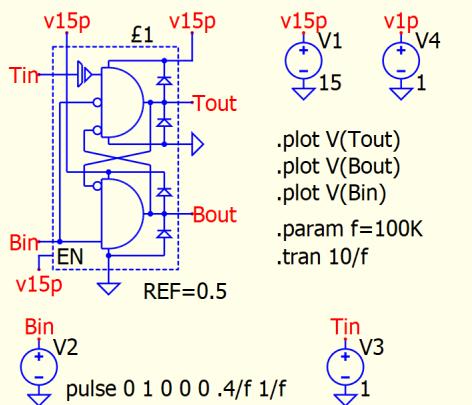
• BUCK

- Add logic such that the bottom FET is off if the top is controlled to on
- **Tin** is inverted to drive Bottom AND gate
 - Bin connects to LOW
- Switch of buck converter is generally at High Side



• BOOST

- Add logic such that the top FET is off if the bottom is controlled to be on
- **Bin** is inverted to drive Top AND gate
 - Tin connects to HIGH
- Switch of boost converter is generally at Low Side

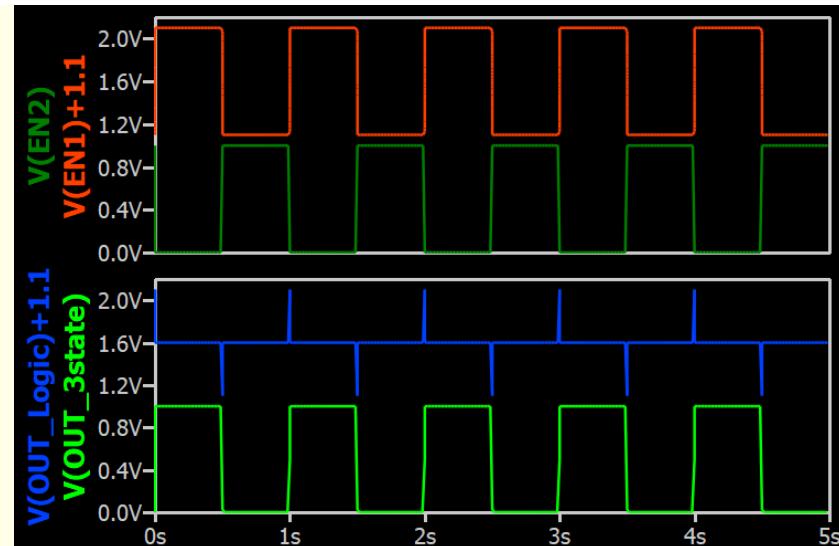
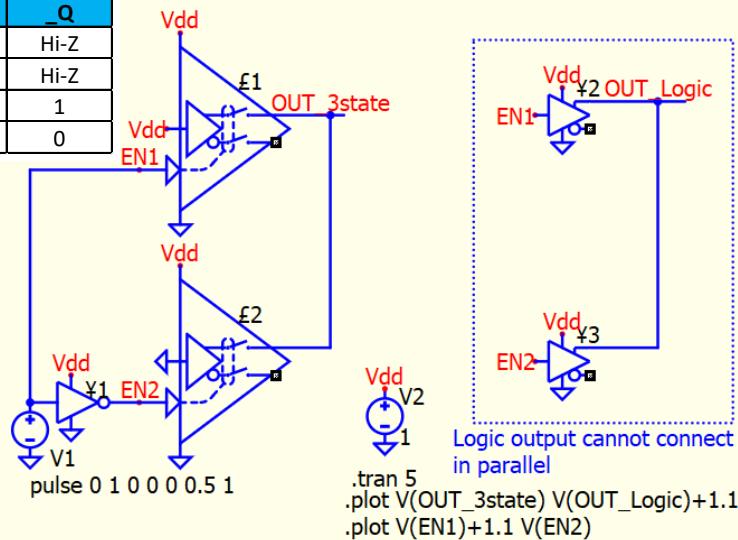


f-Device : Tri-state Buffer

- Tri-state Buffer

- Syntax: fnnn Vdd Vss Q Q̄ IN EN ¥ ¥ ¥ ... 3STATE [INSTANCE PARAMETERS]
- A tri-state output allows multiple circuits to share the same output line(s)
- Output into High-Z when disable

f-Device Tri-state Buffer			
EN	IN	Q	_Q
0	0	Hi-Z	Hi-Z
0	1	Hi-Z	Hi-Z
1	0	0	1
1	1	1	0

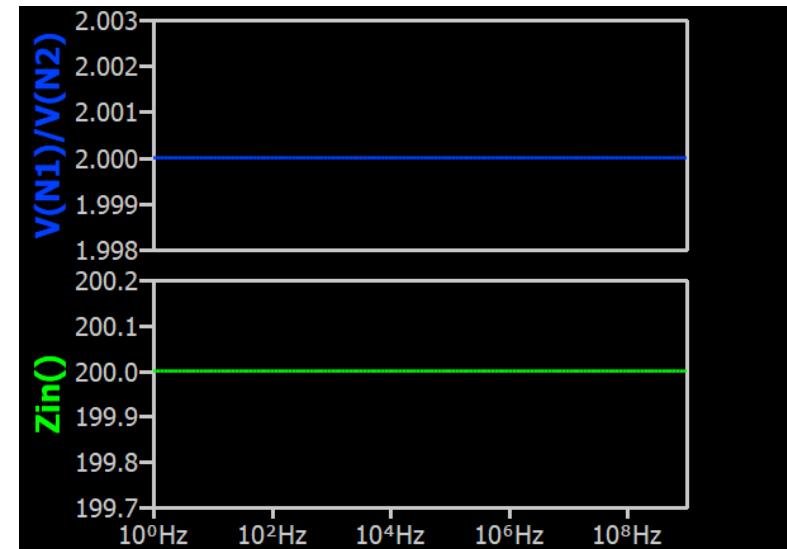
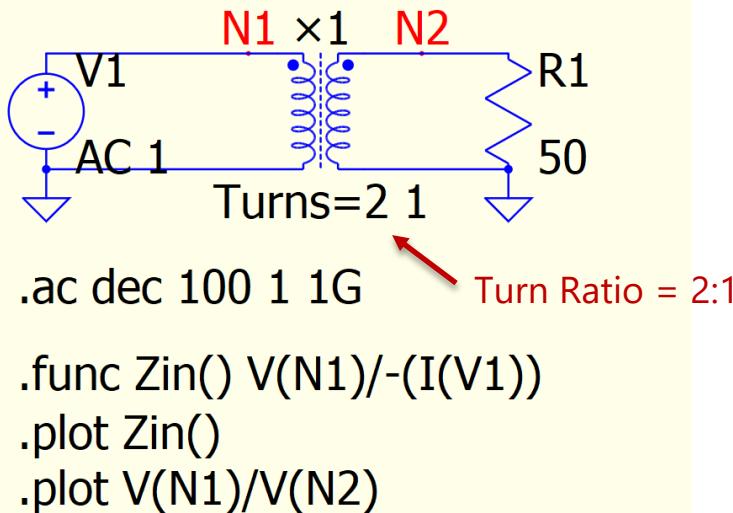


**x-Device
Transformer**

✗-Device: Transformer

Qspice : Transformer - Basic.qsch

- ✗-Device: Transformer
 - Syntax: $\times nnn \text{ «PRI+ PRI- SEC1+ SEC1- SEC2+ SEC2 [...]» } <\text{TURN}=N1 N2 N3 ...>$ [Additional Instance Parameters]
 - Ideal Transformer Equation (Inductance $\rightarrow \infty$)
 - $n = \frac{N_1}{N_2} = \frac{v_1}{v_2}$ and $Z_{N1} = n^2 Z_{N2}$



x-Device: Transformer Instance Params

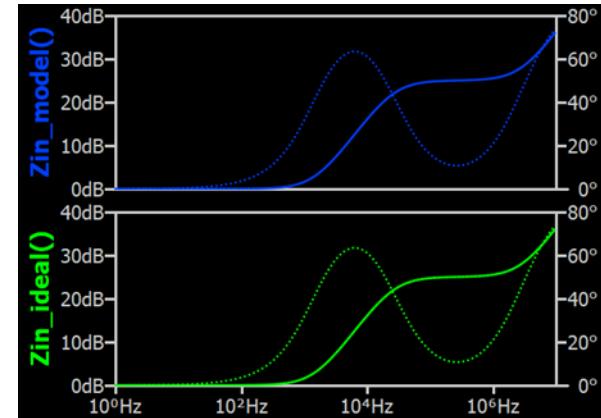
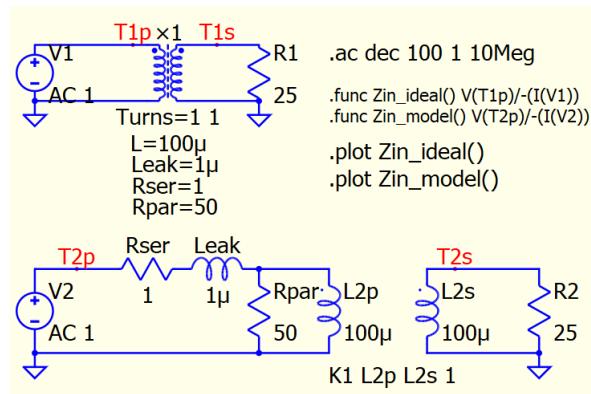
Transformer Instance Parameters

Name	Description	Units	Default
ISAT ¹	Current that drops inductance to SATFRAC of zero-current value	A	Infinite
K ¹	Alternate means of specifying LEAK		1
L	Primary zero-current inductance	H	Infinite
LEAK	Leakage inductance	H	0
LSAT ¹	Inductance asymptotically approached in saturation	H	10% of L
RPAR ¹	Primary parallel resistance	Ω	Infinite
RSER ¹	Primary series resistance	Ω	0.0
SATFRAC ¹	Fractional drop in L at ISAT		0.7
TURNS	List of relative number of turns		

Instance Params : L, Leak, Rser, Rpar, Isat, Lsat, Satfrac

Qspice : Transformer - L Leak Rser Rpar.qsch ; Transformer - Isat Lsat Satfrac.qsch

- L, Leak, Rser, Rpar
 - L : Primary Inductance
 - Leak : Leakage Inductance
 - Rser : Series Resistance
 - Rpar : Parallel Resistance
 - Equivalent model is shown in this simulation



- ISAT, LSAT, SATFRAC
 - Isat : Current that drops inductance to SATFRAC*L
 - Satfrac : Fractional drop in L at Isat
 - Lsat : Inductance asymptotically approached in saturation
 - These parameters are ignored unless L is given

