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# Qspice - Model Generators Guide by KSKelvin

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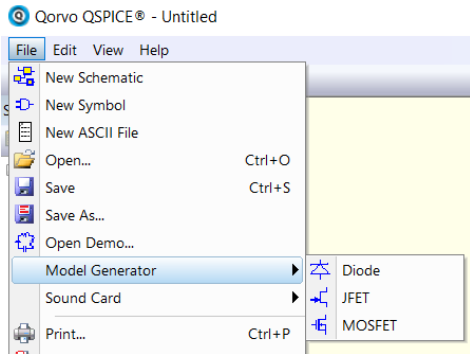
Last Update : 1-20-2025

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# Model Generator and Precaution in using this Guide

- Model Generator

- Model generators are in File > Model Generator > Diode/JFET/MOSFET
- Execute one of these model generators, within the subprogram, it has official HELP



- Precaution in using this Guide

- The model generator appears to still be subject to change. If you are unable to replicate the example provided in this guideline, it may be related to a change in the model generator
- I cannot guarantee the accuracy of this guideline as it heavily relies on parameter studies through these model generators. This guideline is still in its preliminary status

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# Technique in Digitizing Datasheet

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# Digitize with Crosshair Cursor and Arrow Slight Adjustment

## Step #2 : [Crosshair Cursor]

- Move cursor to this area, **hold** Left mouse button  
Now, the cursor become a crosshair

## TYPICAL PERFORMANCE CURVES

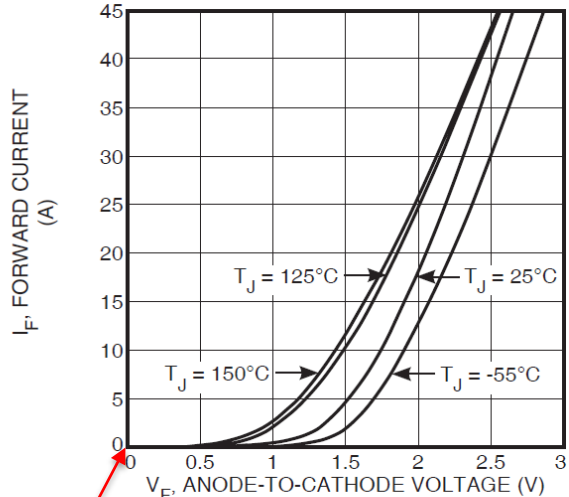
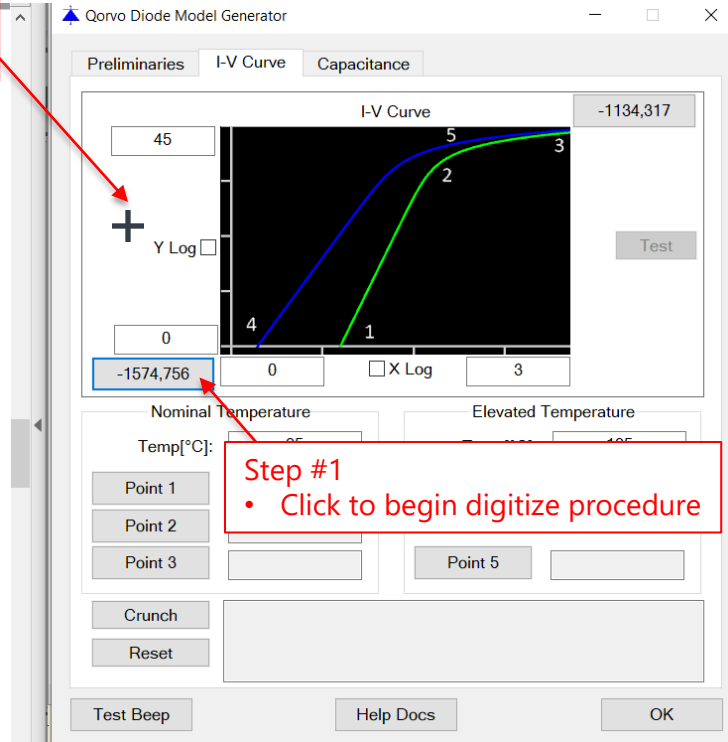


Figure 2. Forward Current vs. Forward Voltage

## Step #3 :

- Move crosshair cursor to pdf to digitize lower left corner  
(Can **use arrow key to adjust crosshair position precisely**)
- Release left mouse button and location is digitized
- [Repeat Step #2 and #3 until all points is digitized]

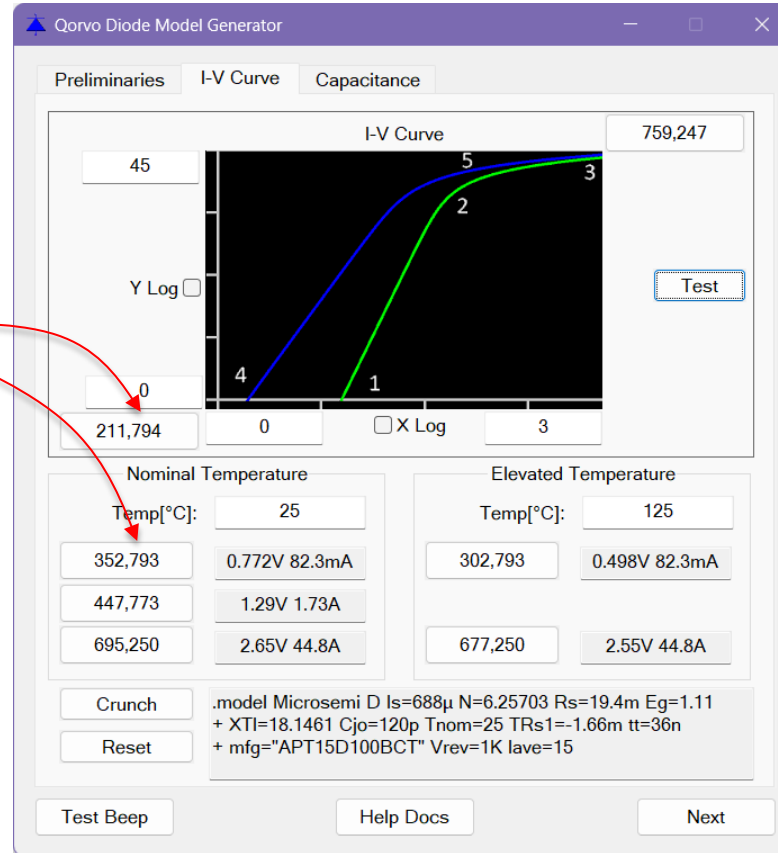


## Step #1

- Click to begin digitize procedure

# Useful Technique in using Digitize

To digitize a very small value on a linear scale, use the arrow keys to make fine adjustments to the cursor. Monitor the y-axis value to ensure it is one digit less than the y-axis value of the LowerLeft.



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# Diode Model Generator

DIODE.exe

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Diode Model  
Generator

Parameters  
Generation

# Diode Model Generator – Preliminaries Tab

Determine : mfg, lave, Vrev, Eg, tt, Cjo\*\*, BV, IBV, NBV

$$tt = \frac{\text{Rev Recovery Charge}}{I @ \text{Rev Recovery}}$$

Calculate **NBV** {  
(formula unknown)

Qorvo DIODE Model Generator

Preliminaries I-V Curve Capacitance

Model Name: 1N4933

MFG: Vishay **mfg** (display only)

Current Rating[A]: 1 **lave** (display only)

Voltage Rating[V]: 100 **Vrev** (display only)

Technology: Silicon

Rev. Recovery Charge[C]: 400n

I @ Rev. Recovery Q[A]: 1

Zero-biased Output Cap.[F]: 12p **Cjo \*\***

Zener Voltage[V]: Infinite **BV**

Zener Current[A]: 1m **IBV**

Zener Impedance[Ω]: 100

Help Docs OK

|                        |                  |
|------------------------|------------------|
| Silicon                | <b>Eg = 1.11</b> |
| Schottky Barrier Diode | <b>Eg = 0.69</b> |
| Germanium              | <b>Eg = 0.67</b> |
| Gallium Nitride(GaN)   | <b>Eg = 3.47</b> |
| Siconon Carbide(SiC)   | <b>Eg = 3.26</b> |
| Gallium Arsenide(GaAs) | <b>Eg = 1.42</b> |

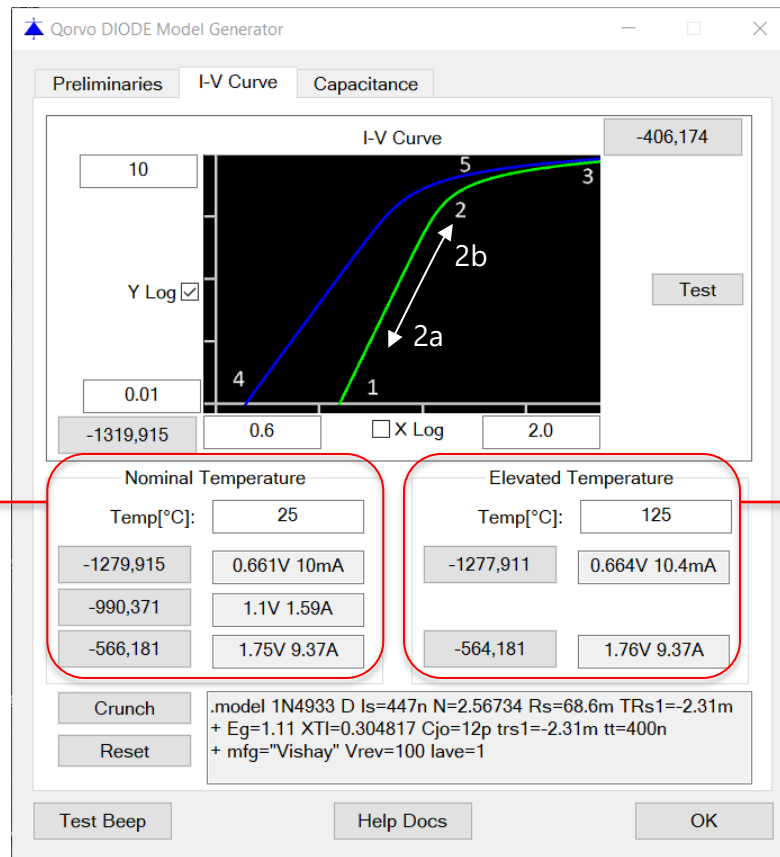
**BV, IBV, NBV** will be generated if this box is non-zero

**Cjo** : This only determine Cjo in I-V Curve digitized tab. If Capacitance digitized tab is used, this Cjo will be ignored



# Diode Model Generator – I-V Curve Tab

Determine :  $I_s$ ,  $N$ ,  $R_s$ ,  $TRs1$ ,  $XTI$



Determine  $I_s$ ,  $N$ ,  $R_s$

Determine  $TRs1$ ,  $XTI$

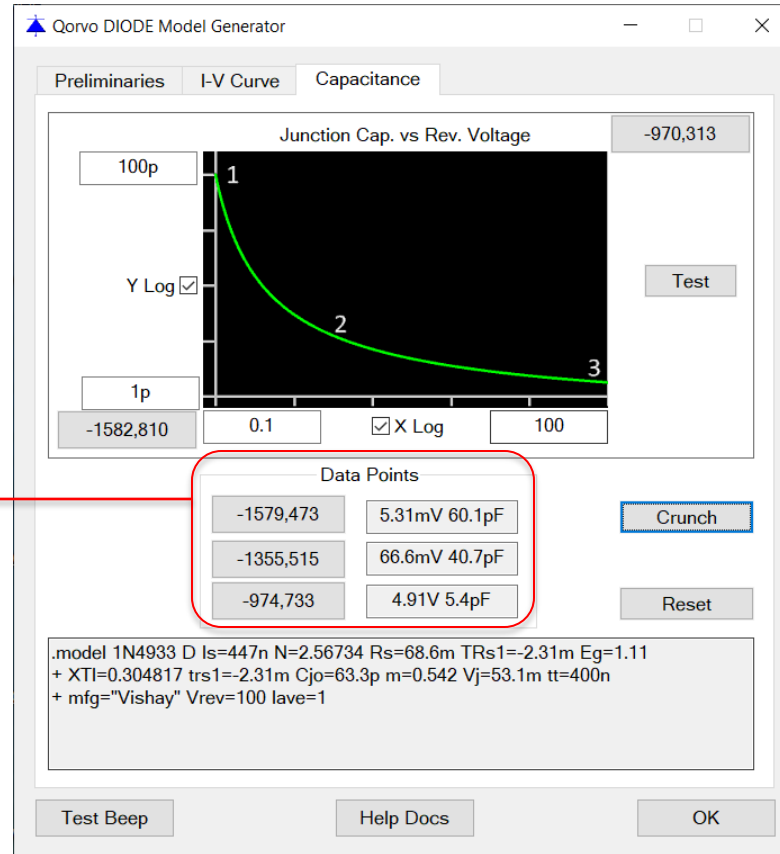
If Temp set to be identical nominal temperature, force  $TRs1=0$  and  $XTI=3$  (If  $XTI=3$ ,  $TRs1$  may not generated)

\*\* where to digitize point #2 can affect  $I_s$  and  $N$   
If point #1 and #2 are closer (e.g. at #2a),  $I_s$  tends to be calculated smaller

# Diode Model Generator – Capacitance Tab

Determine :  $C_{jo}$ ,  $m$ ,  $V_j$

Determine  $C_{jo}$ ,  $m$  and  $V_j$



## Diode Model Generator

Example – Datasheet  
of Onsemi MURS1200

# Example – Onsemi MURS120 Datasheet to Model Generator

| MAXIMUM RATINGS  |                                 |  |       |       |       |
|--|---------------------------------|--|-------|-------|-------|
| Rating   | Symbol                          | MURS/SURS/NRVUS  |       |       |       |
|  |                                 | 105T3  | 110T3 | 115T3 | 120T3 |
| Peak Repetitive Reverse Voltage<br>Working Peak Reverse Voltage<br>DC Blocking Voltage | $V_{RRM}$<br>$V_{RWM}$<br>$V_R$ | 50   | 100   | 150   | 200   |
| Continuous Forward Current   | $I_{F(DC)}$                     | 1.0 @ $T_L = 159^{\circ}\text{C}$<br>2.0 @ $T_L = 139^{\circ}\text{C}$ |       |       |       |

Qorvo DIODE Model Generator

Preliminaries I-V Curve Capacitance

Model Name: **MURS120**

MFG: OnSemi

Current Rating[A]: 1

Voltage Rating[V]: 200

Technology: Silicon

Rev. Recovery Charge[C]: 35n

I @ Rev. Recovery Q[A]: 1

Zero-biased Output Cap.[F]: 45p

Zener Voltage[V]: Infinite

Zener Current[A]: 1m

Zener Impedance[Ω]: 100

Help Docs OK

|   |          |          |
|---|----------|----------|
| Maximum Reverse Recovery Time<br>( $I_F = 1.0\text{ A}$ , $di/dt = 50\text{ A}/\mu\text{s}$ , $V_R = 30\text{ V}$ )<br>( $I_F = 0.5\text{ A}$ , $I_R = 1.0\text{ A}$ , $I_R$ to 0.25 A) | $t_{rr}$ | 35<br>25 |
|---|----------|----------|

- Reverse Recovery Time is given at  $I_F=1\text{A}$
- I @ Rev. Recovery = 1A
  - Rev. Recovery Charge =  $t_{rr} * I_F = 35\text{n}$

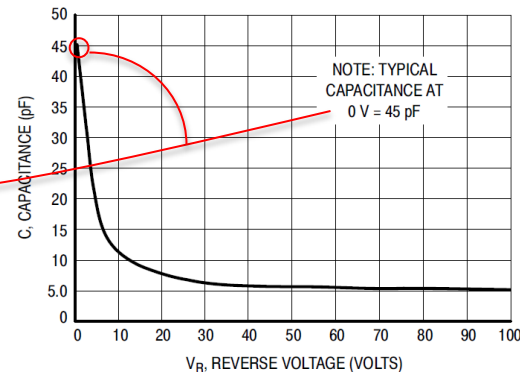


Figure 3. Typical Capacitance

# Example – Onsemi MURS120 Datasheet to Model Generator

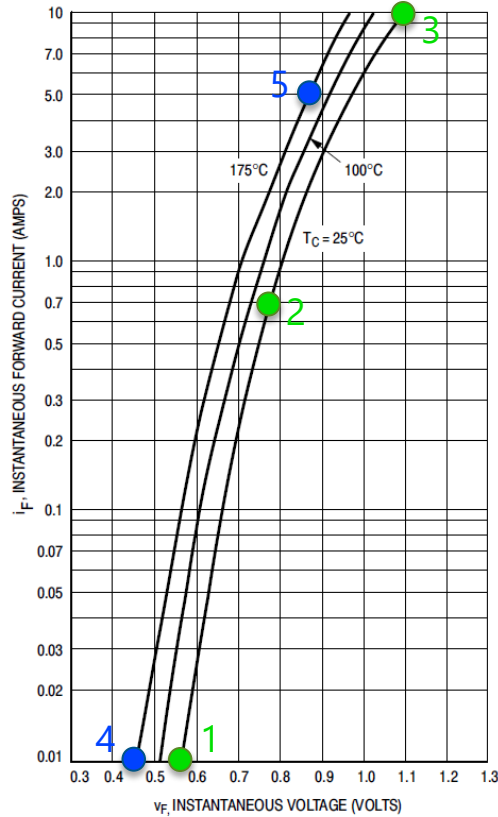
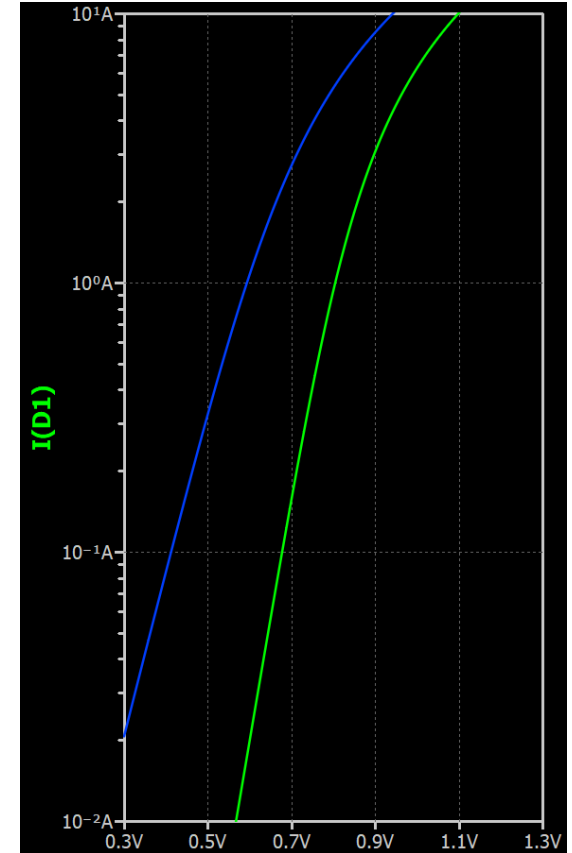
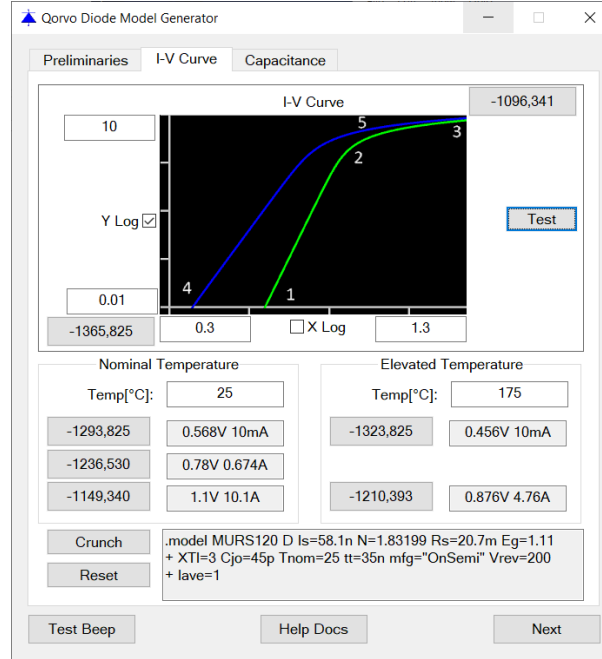


Figure 1. Typical Forward Voltage



# Example – Onsemi MURS120 Datasheet to Model Generator

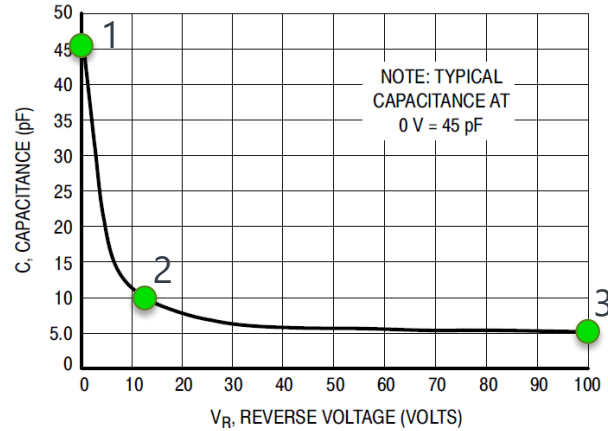
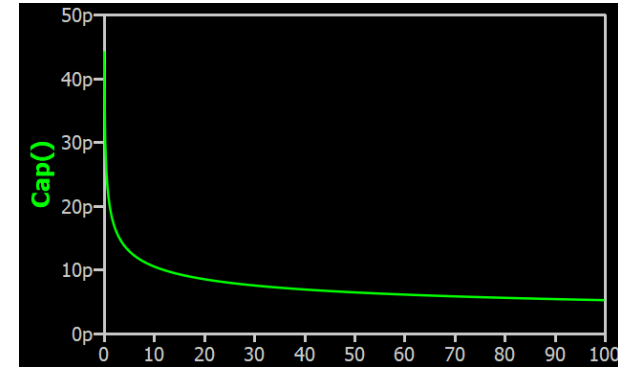
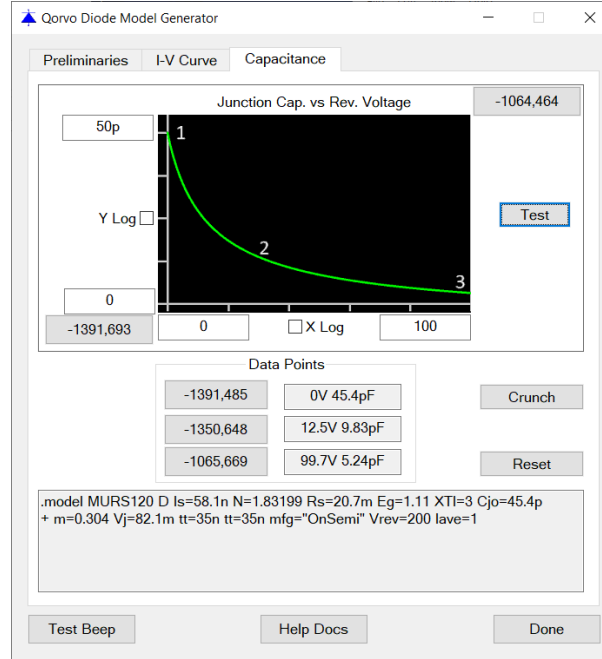


Figure 3. Typical Capacitance



## Diode Model Generator

Example – Datasheet  
of Microchip  
APT15D100BCT

# Example – Microchip APT15D100BCT Datasheet to Model Generator

| MAXIMUM RATINGS  |                                 |  |       |       |       |
|--|---------------------------------|--|-------|-------|-------|
| Rating   | Symbol                          | MURS/SURS/NRVUS  |       |       |       |
|  |                                 | 105T3  | 110T3 | 115T3 | 120T3 |
| Peak Repetitive Reverse Voltage<br>Working Peak Reverse Voltage<br>DC Blocking Voltage | $V_{RRM}$<br>$V_{RWM}$<br>$V_R$ | 50   | 100   | 150   | 200   |
| Continuous Forward Current   | $I_{F(DC)}$                     | 1.0 @ $T_L = 159^\circ\text{C}$<br>2.0 @ $T_L = 139^\circ\text{C}$ |       |       |       |

|           |                                  |   |   |     |   |      |
|-----------|----------------------------------|---|---|-----|---|------|
| $t_{rr}$  | Reverse Recovery Time            | $I_F = 15\text{A}$ , $di_F/dt = -200\text{A}/\mu\text{s}$<br>$V_R = 667\text{V}$ , $T_C = 25^\circ\text{C}$ | - | 260 | - | ns   |
| $Q_{rr}$  | Reverse Recovery Charge          |   | - | 540 | - | nC   |
| $I_{RRM}$ | Maximum Reverse Recovery Current |   | - | 4   | - | Amps |

Qorvo Diode Model Generator

Preliminaries I-V Curve Capacitance

Model Name: Microsemi  
MFG: APT15D100BCT  
Current Rating[A]: 15  
Voltage Rating[V]: 1000  
Technology: Silicon  
Rev. Recovery Charge[C]: 540n  
I @ Rev. Recovery Q[A]: 15  
Zero-biased Output Cap.[F]: 120p  
Zener Voltage[V]: Infinite  
Zener Current[A]: 1m  
Zener Impedance[Ω]: 100

Help Docs
Next

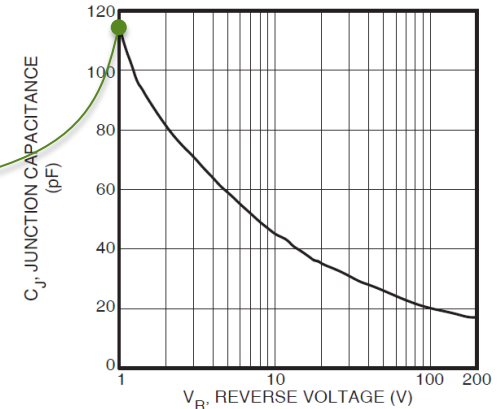


Figure 8. Junction Capacitance vs. Reverse Voltage



# Example – Microchip APT15D100BCT Datasheet to Model Generator

Qspice reference is log plot (y-axis log, x-axis linear),  
marker 1-5 is different if linear plot is used

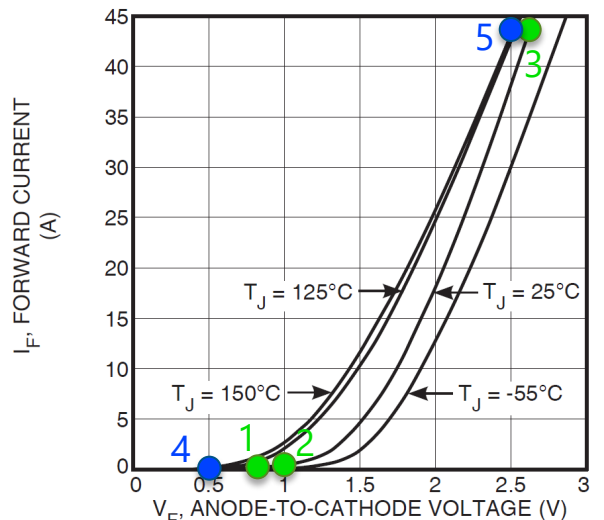
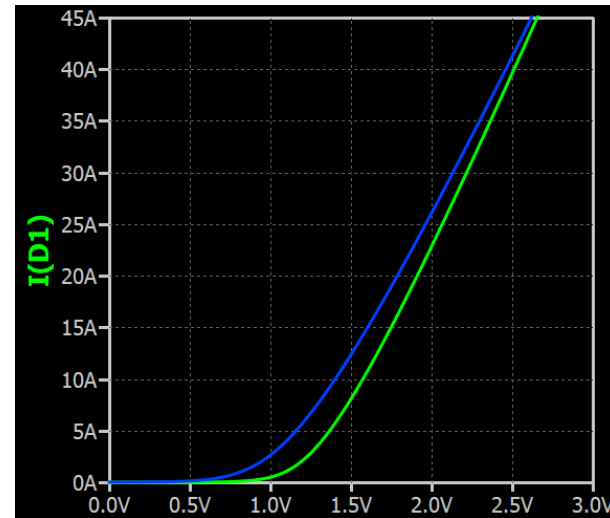
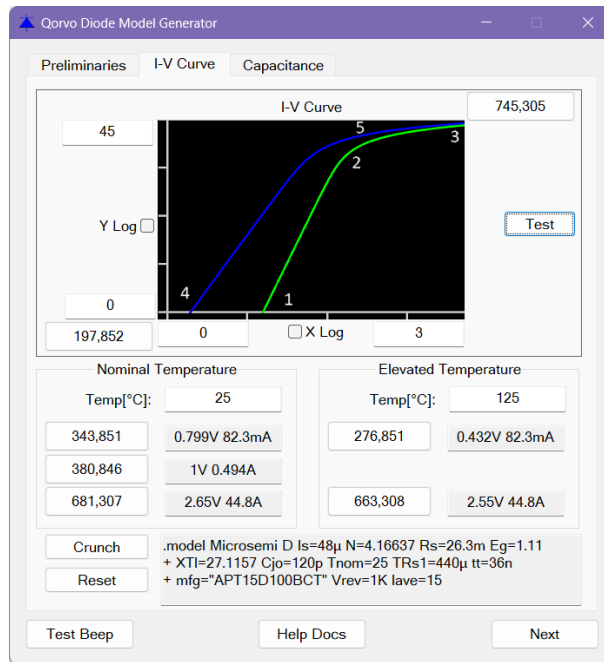


Figure 2. Forward Current vs. Forward Voltage

Marker 1 to 5 if linear plot is used  
(y-axis and x-axis are both linear)



# Example – Microchip APT15D100BCT Datasheet to Model Generator

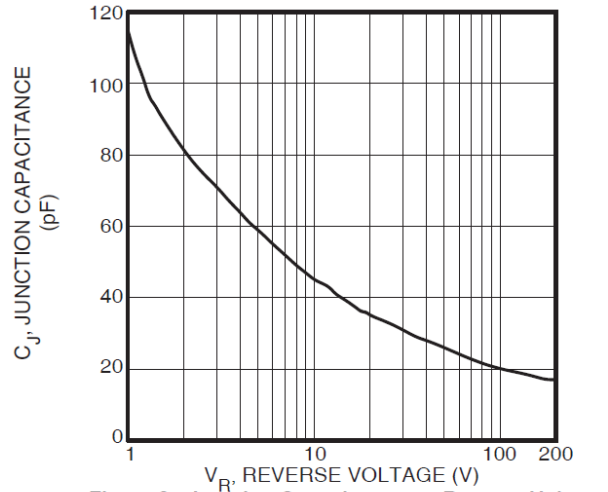
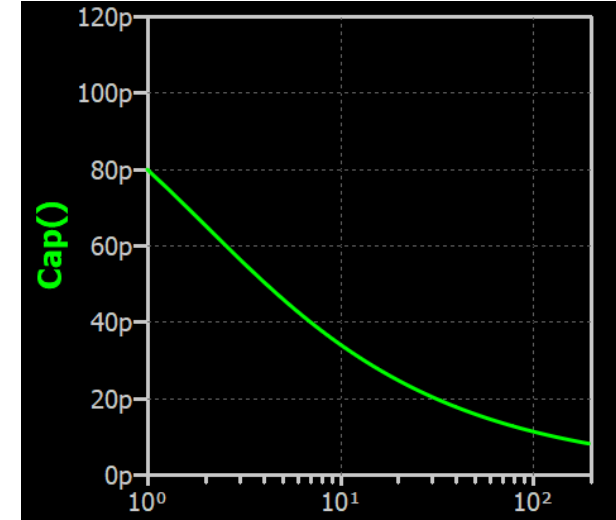
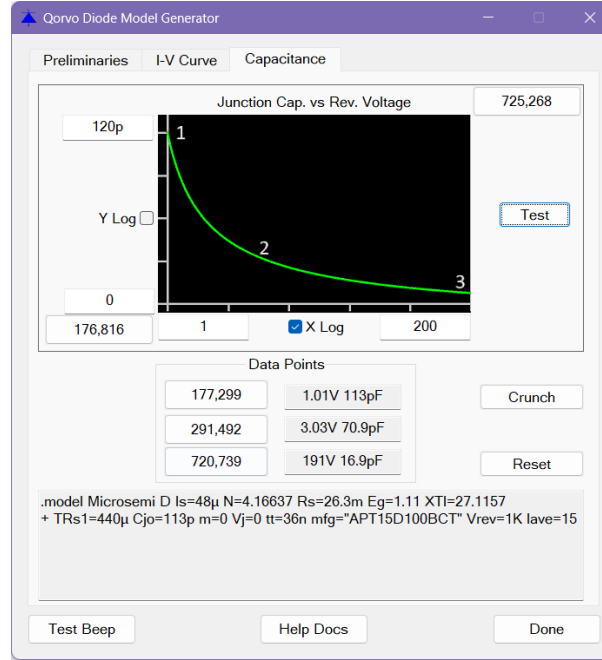


Figure 8. Junction Capacitance vs. Reverse Voltage



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# MOSFET Model Generator

MOSFET.exe

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# MOSFET Model Generator

Parameters  
Generation

# MOSFET Model Generator – Preliminaries Tab

Determine : mfg, Ids, Vds, Qg, Rg, Rds, Rd, Rs, Eg, tt

$$R_d + R_s = R_{ds(on)} \times (R_{ext} \div (R_{ext} + R_{channel}))$$

- $R_{ext} = R_d + R_s$  (e.g. bond wire, contact)
- $R_{channel}$  is  $R_{ds}$  of MOSFET channel

Not provide by datasheet, from Mike Engelhardt experience, in ~75% of resistance is contributed by  $R_{ext}$

$$R_d = R_{ds(on)} \times (R_{ext} \div (R_{ext} + R_{channel})) \times (R_d \div (R_d + R_s))$$

$$R_s = R_{ds(on)} \times (R_{ext} \div (R_{ext} + R_{channel})) - R_d$$

Not provided by datasheet, from Mike experience, Ratio of  $R_d$  and  $R_s$  from  $R_{ext}$ , approximate by 50%

Representation:

$$\frac{x}{x+y} \rightarrow 1 : x \gg y$$

$$\frac{x}{x+y} \rightarrow 0 : y \gg x$$

| Field                       | Value   | Notes   |
|-----------------------------|---------|---|
| Model Name:                 | IRF630  |   |
| MFG:                        | Vishay  | mfg (display only)  |
| Ids Rating[A]:              | 9       | Ids (display only)  |
| Vds Rating[V]:              | 200     | Vds (display only)  |
| Total Gate Charge[C]:       | 43      | Qg (display only)   |
| Rg[Ω]:                      | 2       | Rg  |
| Rds(on)[Ω]:                 | 0.2     | Ron (display), but also use to calculate Rd and Rs  |
| Vgs @ Rds(on)[V]:           | 10      | Contribute to Calculation of RonX (formula unknown)   |
| I @ Rds(on)[A]:             | 5.4     |   |
| Rext ÷ (Rext + Rchannel)    | 0.75    |   |
| Rd ÷ (Rd + Rs)              | 0.5     |   |
| Technology:                 | Silicon | Eg  |
| Rev. Recovery Charge[C]:    | 1.1n    | tt = Rev Recovery Charge / I @ Rev Recovery   |
| I @ Rev. Recovery Q[A]:     | 5.9     |   |
| Zero-biased Output Cap.[F]: | 1.5n    | Contribute to Calculation of Cjo<br>Cjo + Cgdmax = Zero-biased Output Cap Capacitance @ 0Vds! |

# Preliminaries Tab and its Affected Section

Qorvo MOSFET Model Generator

Preliminaries Output Characteristics Body Diode Gate Charge

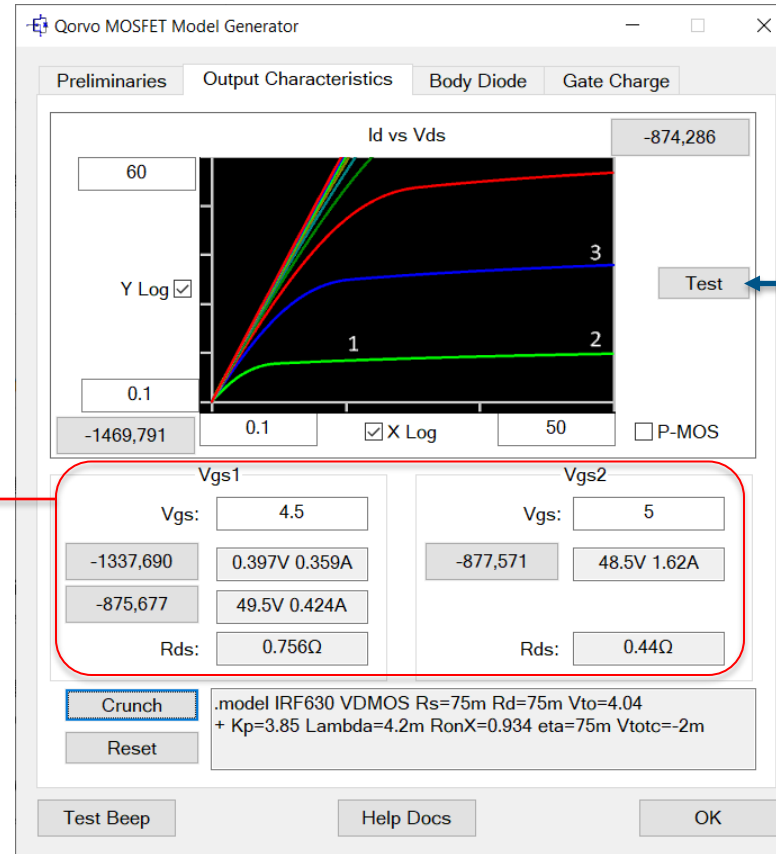
|                             |         |                                       |
|-----------------------------|---------|---------------------------------------|
| Model Name:                 | IRF630  | No effect                             |
| MFG:                        | Vishay  | No effect (mfg= <str> display only)   |
| Ids Rating[A]:              | 9       | No effect (Ids= <value> display only) |
| Vds Rating[V]:              | 200     | No effect (Vds= <value> display only) |
| Total Gate Charge[C]:       | 43      | No effect (Qg= <value> display only)  |
| Rg[Ω]:                      | 2       | Gate Charge : Rg= <value>             |
| Rds(on)[Ω]:                 | 0.2     | Output Characteristics                |
| Vgs @ Rds(on)[V]:           | 10      | Output Characteristics                |
| I @ Rds(on)[A]:             | 5.4     | Output Characteristics                |
| Rext ÷ (Rext + Rchannel):   | 0.75    | Output Characteristics                |
| Rd ÷ (Rd + Rs):             | 0.5     | Output Characteristics                |
| Technology:                 | Silicon | Body Diode                            |
| Rev. Recovery Charge[C]:    | 1.1n    | Output Characteristics : tt= <value>  |
| I @ Rev. Recovery Q[A]:     | 5.9     | Output Characteristics : tt= <value>  |
| Zero-biased Output Cap.[F]: | 1.5n    | Gate Charge                           |

Help Docs OK

# MOSFET Model Generator – Output Characteristics

Determine :  $V_{to}$ ,  $K_p$ ,  $\Lambda$ ,  $R_{onX}$ ,  $\eta$ ,  $V_{totc}$

Determine  $V_{to}$ ,  $K_p$ ,  $\Lambda$ ,  $R_{onX}$



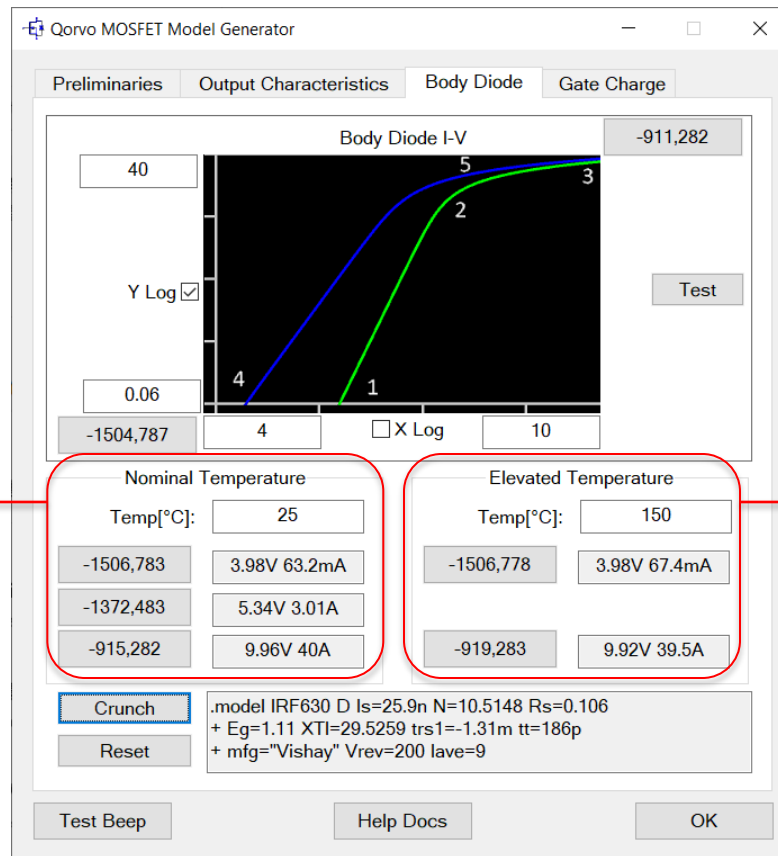
\*\*  $R_{ds,on}$  in preliminaries tab can be used to fine tuning Id vs Vds curve at lower Vds region

\*\*  $\eta$  and  $V_{totc}$  seems to be fixed  
 $\eta=75m$   
 $V_{totc}=-2m$

# MOSFET Model Generator – Body Diode

Determine :  $I_s$ ,  $N$ ,  $R_s$  ( $R_b$  in MOS),  $TRs1$ ,  $XTI$

Determine  $I_s$ ,  $N$ ,  $R_s$



Determine  $TRs1$ ,  $XTI$

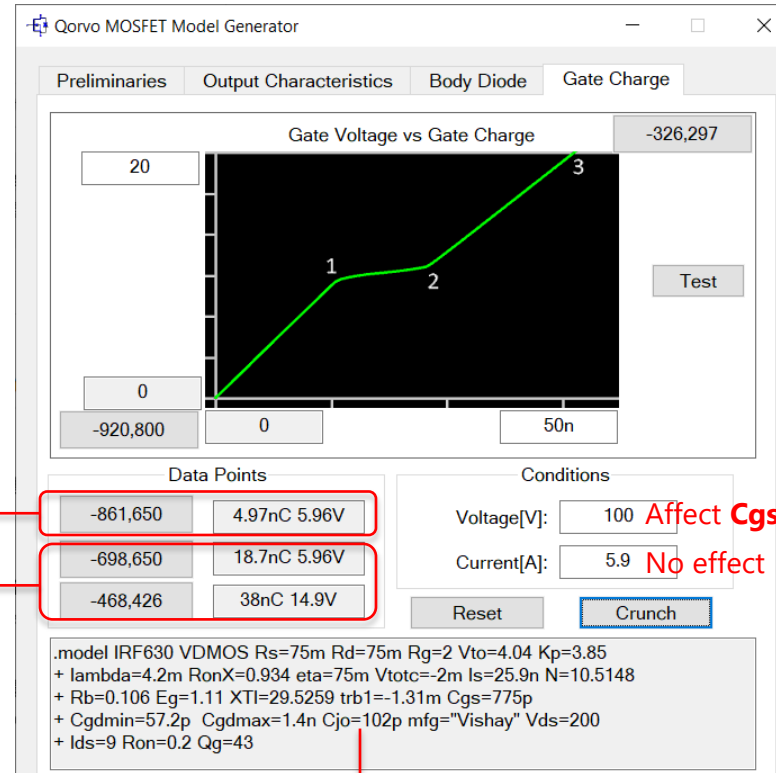
If Temp set to be identical nominal temperature, force  $TRs1=0$  and  $XTI=3$

\*\*  $tt$  and  $E_g$  is from Preliminary tab  
\*\*  $R_s$  is series resistor in diode model, this will rename to  $R_b$  in VDMOS model in Gate Charge tab ( $R_s \rightarrow$  rename to  $R_b$ )



# MOSFET Model Generator – Gate Charge

Determine :  $C_{gs}$ ,  $C_{gdmin}$ ,  $C_{gdmax}$ ,  $C_{jo}$



mainly determine :  $C_{gs}$

mainly determine :  $C_{gdmin}$ ,  $C_{gdmax}$

Affect  $C_{gs}$ ,  $C_{gdmin}$ ,  $C_{gdmax}$ ,  $C_{jo}$

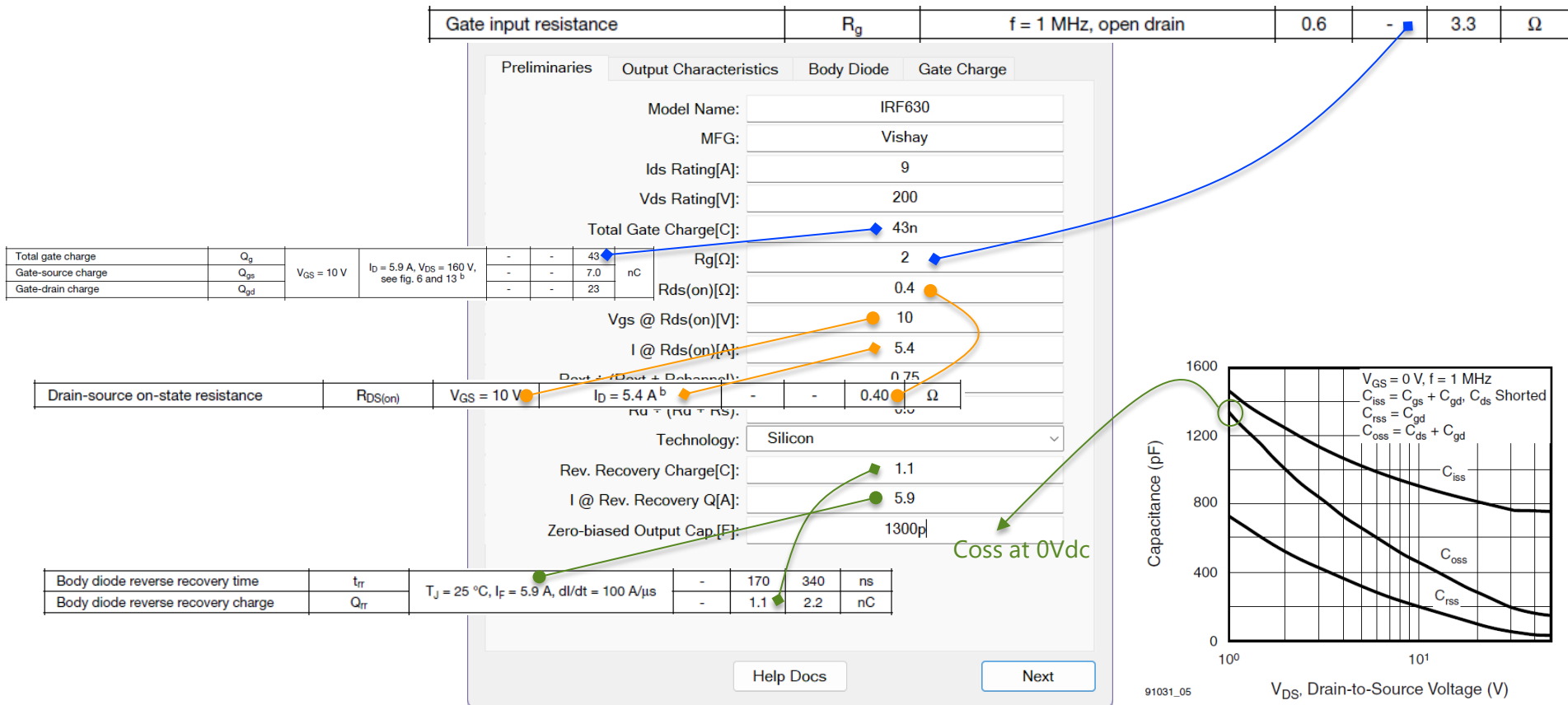
No effect

$C_{jo}$  = Zero-biased Output Cap (Preliminaries) –  $C_{gdmax}$  (min. value as 0)  
[ $C_{jo}$  is body diode zero-bias capacitance]

# MOSFET Model Generator

Example – Datasheet  
of Vishay IRF630

# Example – Vishay IRF630 Datasheet to Model Generator



# Example – Vishay IRF630 Datasheet to Model Generator

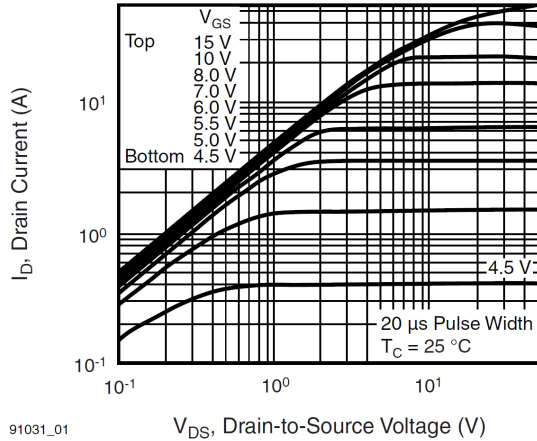
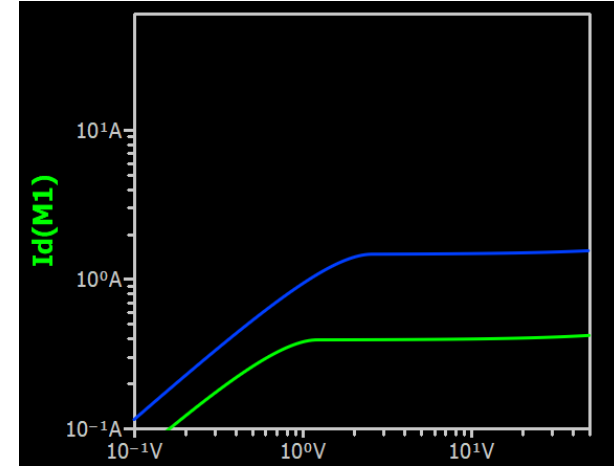


Fig. 1 - Typical Output Characteristics,  $T_C = 25^\circ\text{C}$



# Example – Vishay IRF630 Datasheet to Model Generator

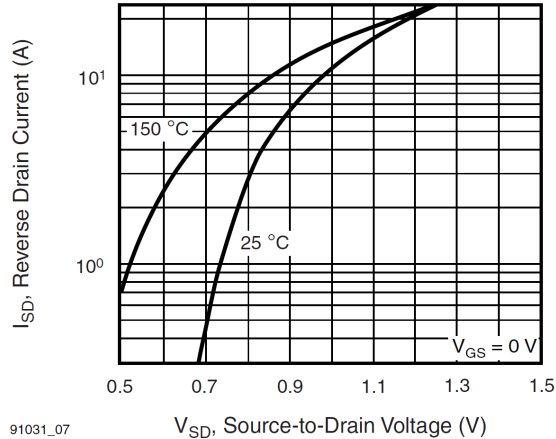
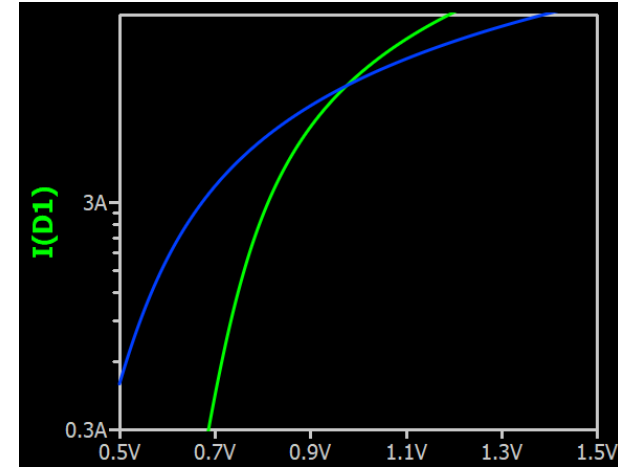
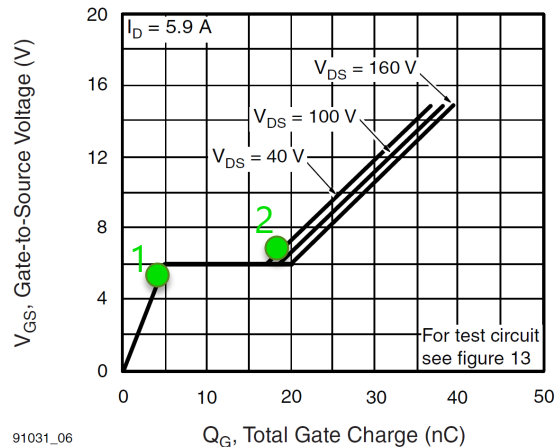


Fig. 7 - Typical Source-Drain Diode Forward Voltage



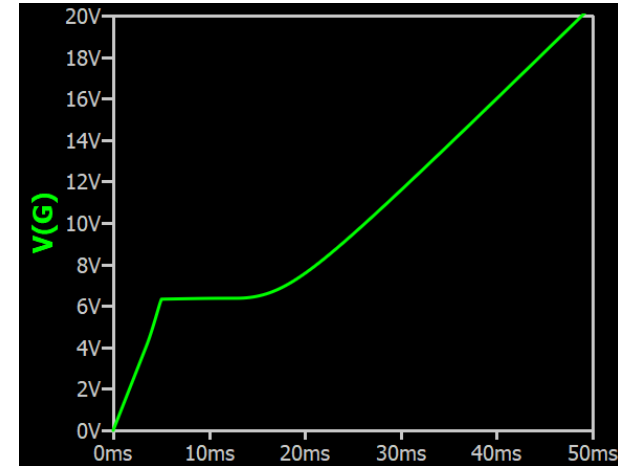
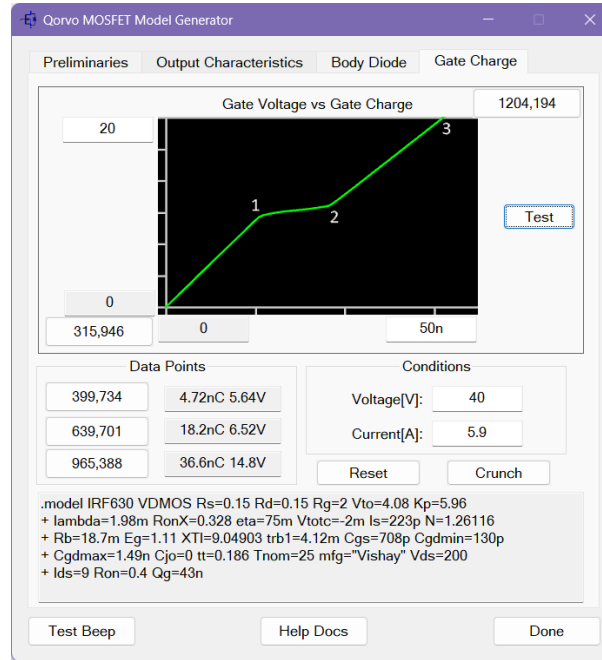
# Example – Vishay IRF630 Datasheet to Model Generator



91031\_06

**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**

According to Mike, Point #1 and #2 are sampled slightly lower and slightly higher than flat region



# MOSFET Model Generator

Example – pMOS  
DMP3099L

# pMOS DMP3099L – Preliminaries and Output Characteristics

Qorvo MOSFET Model Generator

Preliminaries Output Characteristics Body Diode Gate Charge

Model Name: DMP3099L

MFG: Diodes

Ids Rating[A]: -3

Vds Rating[V]: -30

Total Gate Charge[C]: 11n

Rg[Ω]: 10.3

Rds(on)[Ω]: 65m

Vgs @ Rds(on)[V]: 10

I @ Rds(on)[A]: 3.8

Rext ÷ (Rext + Rchannel): 0.75

Rd ÷ (Rd + Rs): 0.5

Technology: Silicon

Rev. Recovery Charge[C]: 10n

I @ Rev. Recovery Q[A]: 2

Zero-biased Output Cap.[F]: 300p

Display ONLY  
Can put -ve  
number in here

**\*\* All numbers should be positive  
even if modeling a P-polarity device**

Help Docs Next

Qorvo MOSFET Model Generator

Preliminaries Output Characteristics Body Diode Gate Charge

Id vs Vds 1662,270

Y Log ☐

0 1148,784 0 5 ☐ X Log ☒ P-MOS

Vgs1 Vgs2

Vgs: -2.5 Vgs: -3

1208,764 0.584V 0.778A 1661,658 4.99V 4.9A

1661,753 4.99V 1.21A

Rds: 0.347Ω Rds: 0.186Ω

Crunch .model DMP3099L VDMOS pchan Rs=24.4m Rd=24.4m  
+ Vto=-2.07 Kp=8.64 Lambda=0.157 RonX=0.91 eta=75m  
+ Vt0tc=2m tt=5n

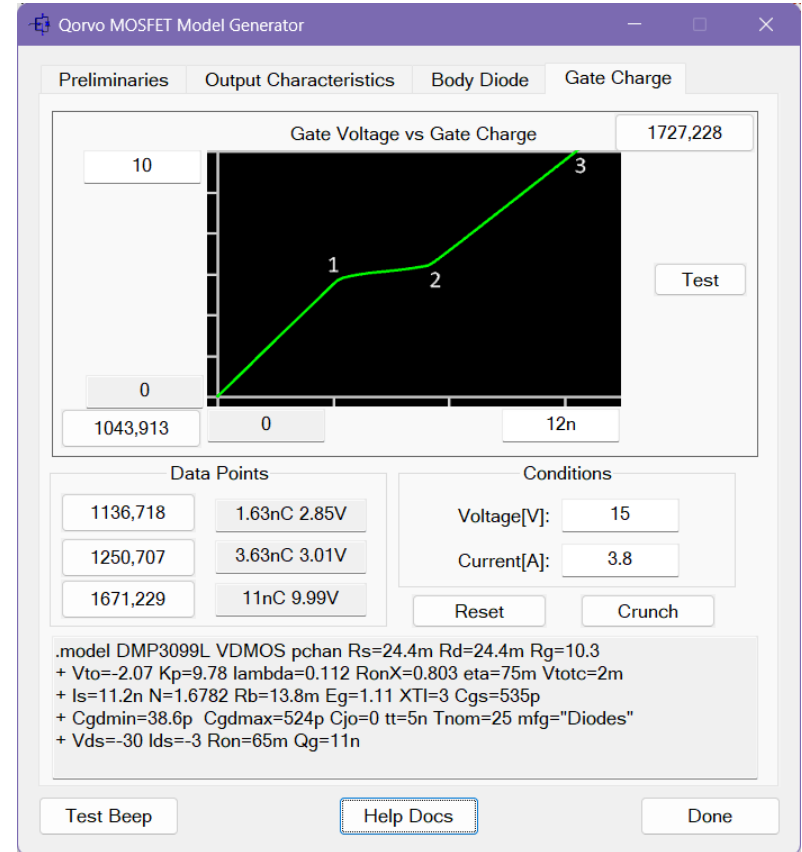
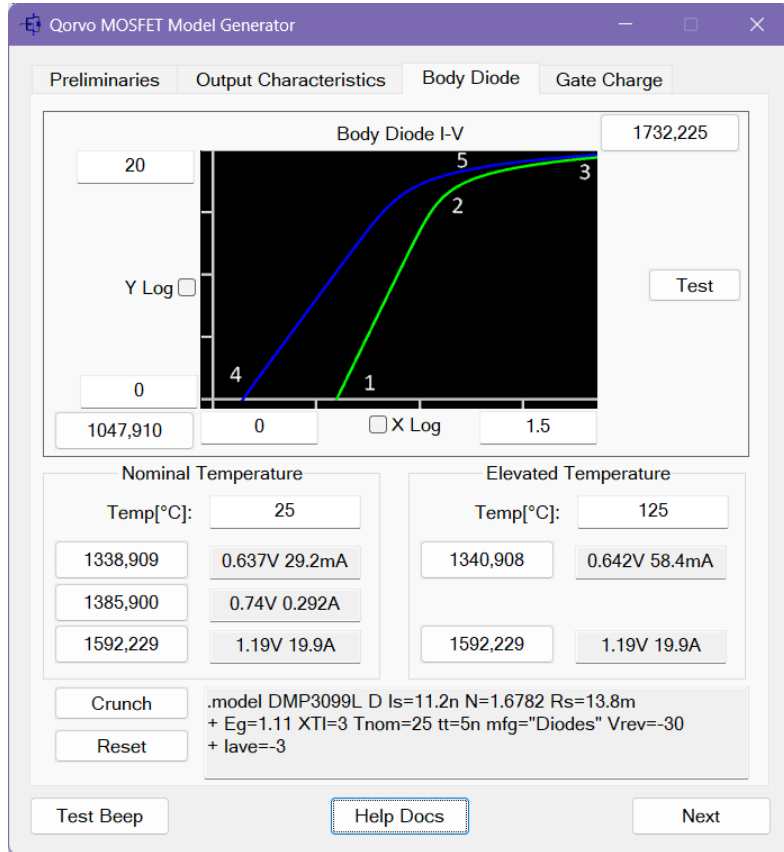
Reset

Test Beep Help Docs Next

P-MOS Vgs definition is -ve  
(accept +ve or -ve as absolute number is  
used in here for model generation)



# pMOS DMP3099L – Body Diode and Gate Charge

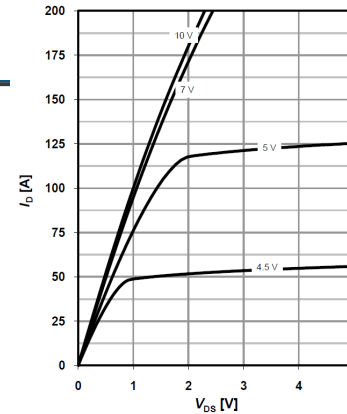


# MOSFET Model Generator

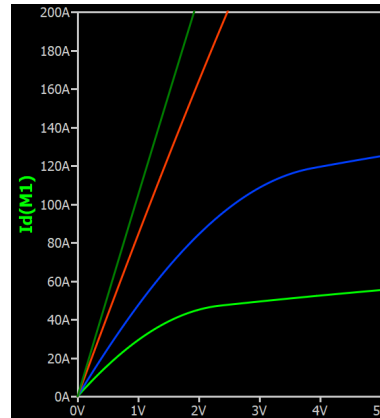
Effect of Parameters  
in Preliminaries Sheet

# Effect of $R_{ext} \div R_{ext} + R_{channel}$

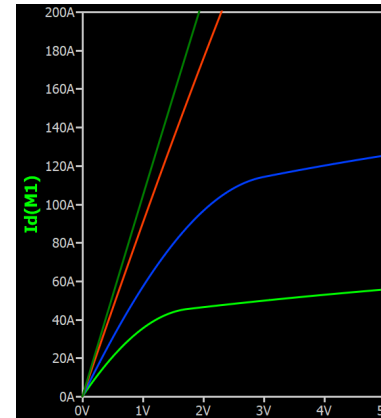
- $R_{ext} \div R_{ext} + R_{channel}$ 
  - Infineon IPB107N20N3G as example
  - Value = 0.75
    - .model IPB107N20N3G  
VDMOS Rs=3.6m Rd=3.6m  
Vto=3.84 Kp=294  
Lambda=0.167 RonX=0.243
  - Value = 0.85
    - .model IPB107N20N3G  
VDMOS Rs=4.08m Rd=4.08m Vto=3.88 Kp=379  
Lambda=0.197 RonX=0.318
  - Value = 0.95
    - .model IPB107N20N3G  
VDMOS Rs=4.56m Rd=4.56m Vto=3.92 Kp=505  
Lambda=0.241 RonX=0.727
- Adjusting the ratio of external and channel resistance affects the width ohmic region



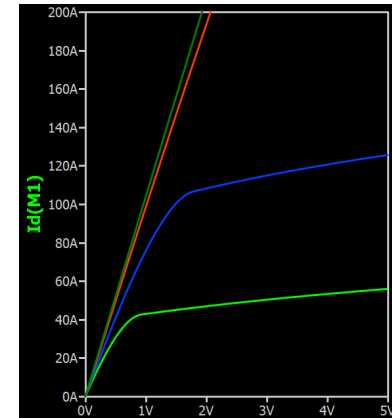
$R_{ext} \div R_{ext} + R_{channel}$   
= 0.75 (default)



$R_{ext} \div R_{ext} + R_{channel}$   
= 0.85 (default)



$R_{ext} \div R_{ext} + R_{channel}$   
= 0.95 (default)

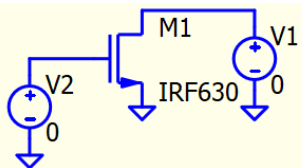


# MOSFET Model Generator

## Effect of Model Parameters

# #1 : Output Characteristic – Rs, Rd

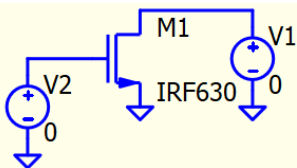
## Qspice : Sensitivity Study - Output Characteristic.qsch



Rs

```
.dc V1 0.1 50 1m V2 list 4.5 5  
.model IRF630 VDMOS Rs=0.15*chg Rd=0.15  
+ Vto=4.08 Kp=5.63 Lambda=3.85m  
+ RonX=0.348 eta=75m Vtotc=-2m tt=0.186
```

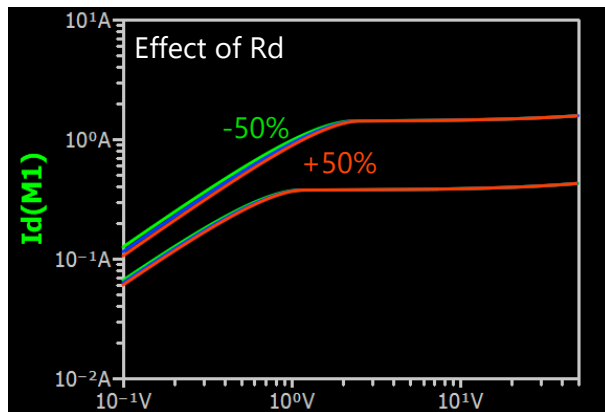
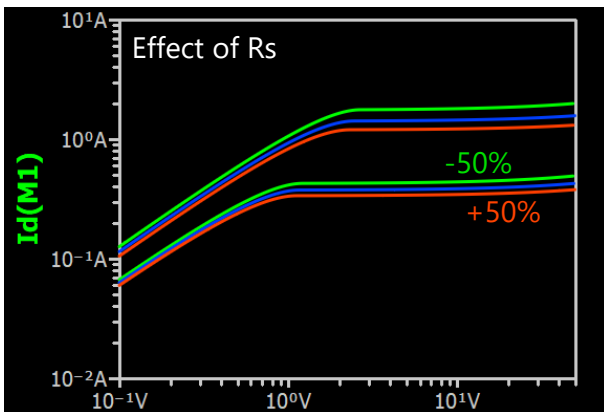
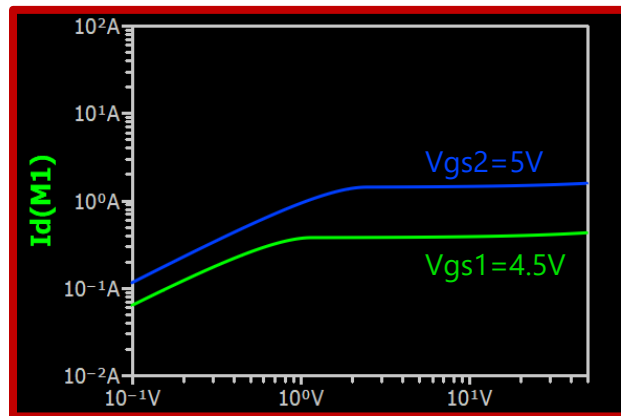
```
;multiple chg (*chg)  
.step param chg list 0.5 1 1.5
```



Rd

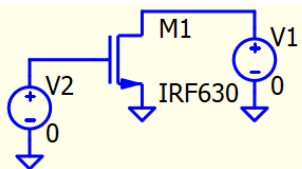
```
.dc V1 0.1 50 1m V2 list 4.5 5  
.model IRF630 VDMOS Rs=0.15 Rd=0.15*chg  
+ Vto=4.08 Kp=5.63 Lambda=3.85m  
+ RonX=0.348 eta=75m Vtotc=-2m tt=0.186
```

```
;multiple chg (*chg)  
.step param chg list 0.5 1 1.5
```



# #1 : Output Characteristic – Vto, Kp, Lambda

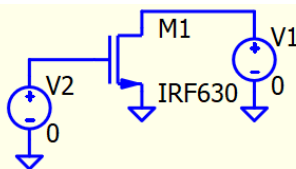
## Qspice : Sensitivity Study - Output Characteristic.qsch



Vto

```
.dc V1 0.1 50 1m V2 list 4.5 5  
.model IRF630 VDMOS Rs=0.15 Rd=0.15  
+ Vto=4.08*chg Kp=5.63 Lambda=3.85m  
+ RonX=0.348 eta=75m Vtotc=-2m tt=0.186
```

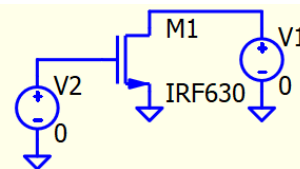
```
;multiple chg (*chg)  
.step param chg list 0.98 1 1.02
```



Kp

```
.dc V1 0.1 50 1m V2 list 4.5 5  
.model IRF630 VDMOS Rs=0.15 Rd=0.15  
+ Vto=4.08 Kp=5.63*chg Lambda=3.85m  
+ RonX=0.348 eta=75m Vtotc=-2m tt=0.186
```

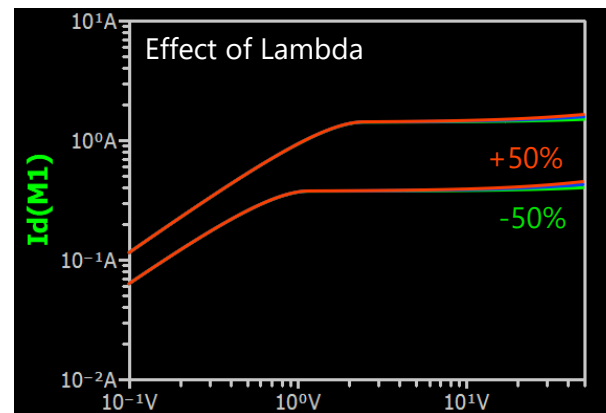
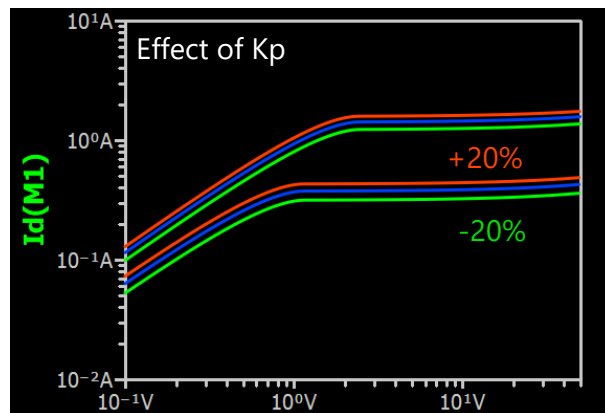
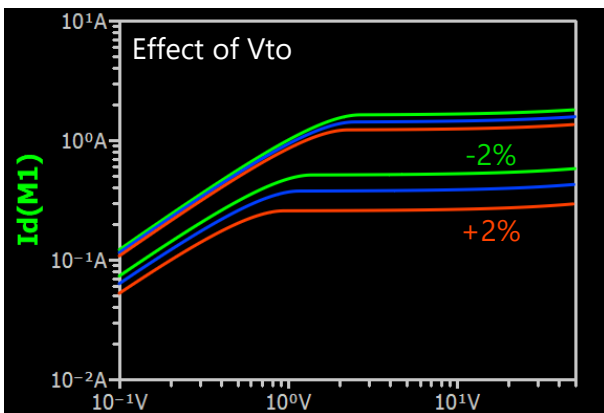
```
;multiple chg (*chg)  
.step param chg list 0.8 1 1.2
```



Lambda

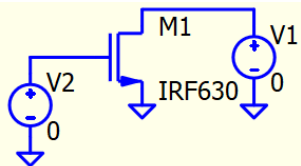
```
.dc V1 0.1 50 1m V2 list 4.5 5  
.model IRF630 VDMOS Rs=0.15 Rd=0.15  
+ Vto=4.08 Kp=5.63 Lambda=3.85m*chg  
+ RonX=0.348 eta=75m Vtotc=-2m tt=0.186
```

```
;multiple chg (*chg)  
.step param chg list 0.5 1 1.5
```



# #1 : Output Characteristic – RonX

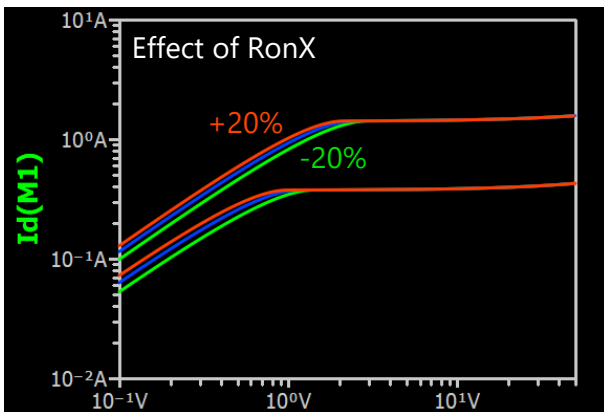
Qspice : Sensitivity Study - Output Characteristic.qsch



RonX

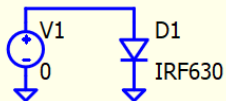
```
.dc V1 0.1 50 1m V2 list 4.5 5  
.model IRF630 VDMOS Rs=0.15 Rd=0.15  
+ Vto=4.08 Kp=5.63 Lambda=3.85m  
+ RonX=0.348*chg eta=75m Vtotc=-2m tt=0.186
```

```
;multiple chg (*chg)  
.step param chg list 0.8 1 1.2
```



# #2 : Bode Diode – XTI, trs1 (Temperature Effect)

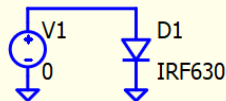
## Qspice : Sensitivity Study - Body Diode.qsch



XTI

```
.dc V1 0.5 1.5 1m
;temp 25 150
.model IRF630 D Is=785p N=1.33849 Rs=21m Eg=1.11
+ XTI=4.53261*chg Tnom=25 trs1=3.56m tt=0.186
+ mfg="Vishay" Vrev=200 Iave=9

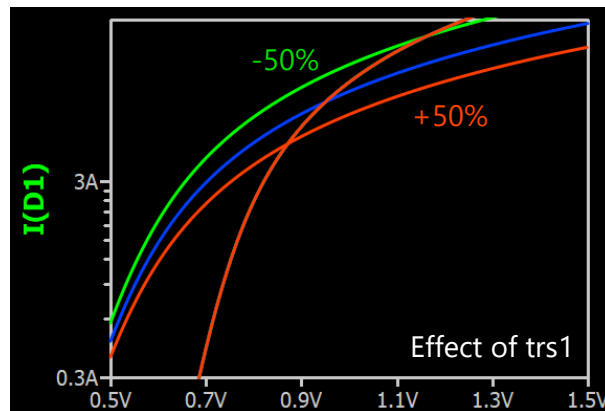
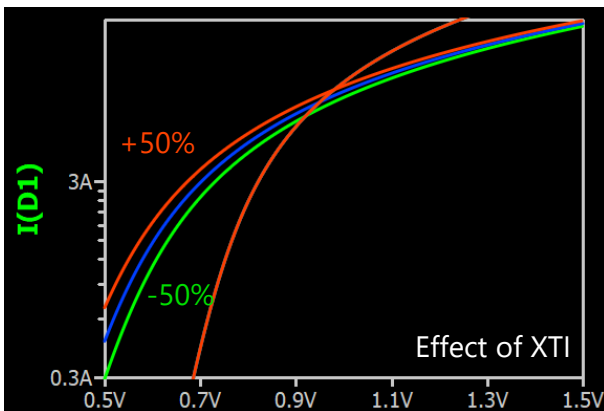
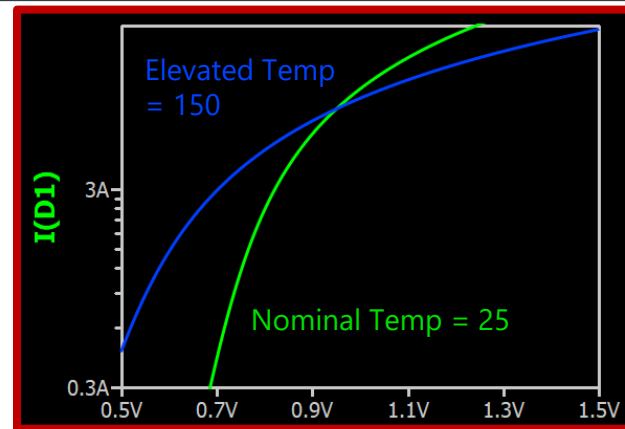
;multiple chg (*chg)
.step param temp list 25 150 param chg list 0.5 1 1.5
```



trs1

```
.dc V1 0.5 1.5 1m
;temp 25 150
.model IRF630 D Is=785p N=1.33849 Rs=21m Eg=1.11
+ XTI=4.53261 Tnom=25 trs1=3.56m*chg tt=0.186
+ mfg="Vishay" Vrev=200 Iave=9

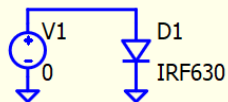
;multiple chg (*chg)
.step param temp list 25 150 param chg list 0.5 1 1.5
```





## #2 : Bode Diode – Is, N, Rs (Rb in MOS)

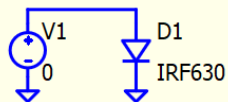
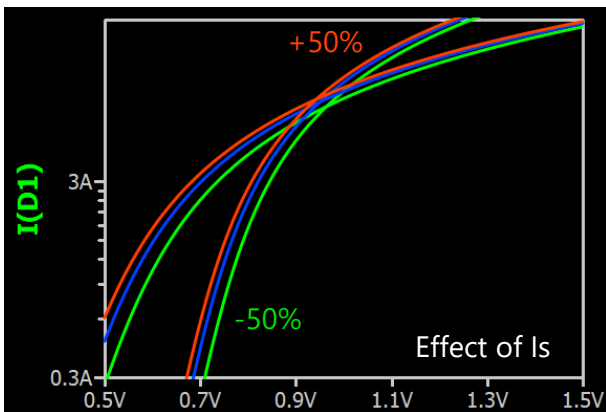
### Qspice : Sensitivity Study - Body Diode.qsch



Is

```
.dc V1 0.5 1.5 1m
;temp 25 150
.model IRF630 D Is=785p*chg N=1.33849 Rs=21m Eg=1.11
+ XTI=4.53261 Tnom=25 trs1=3.56m tt=0.186
+ mfg="Vishay" Vrev=200 Iave=9

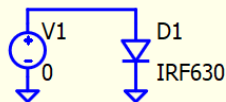
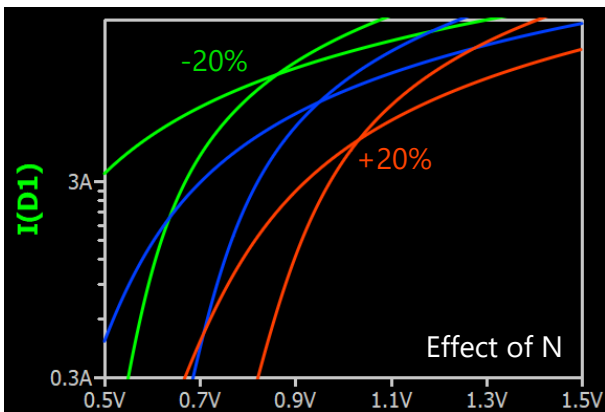
;multiple chg (*chg)
.step param temp list 25 150 param chg list 0.5 1 1.5
```



N

```
.dc V1 0.5 1.5 1m
;temp 25 150
.model IRF630 D Is=785p N=1.33849*chg Rs=21m Eg=1.11
+ XTI=4.53261 Tnom=25 trs1=3.56m tt=0.186
+ mfg="Vishay" Vrev=200 Iave=9

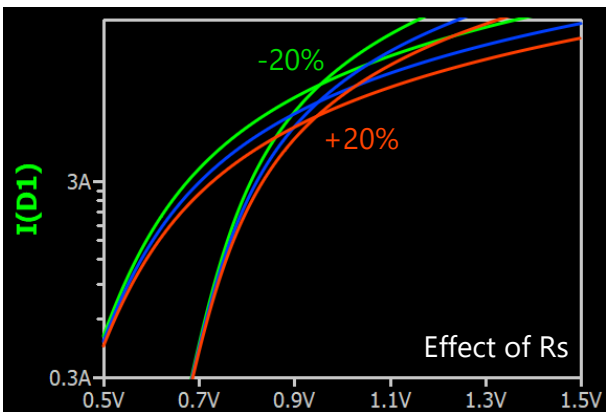
;multiple chg (*chg)
.step param temp list 25 150 param chg list 0.8 1 1.2
```



Rs (Rb in MOS)

```
.dc V1 0.5 1.5 1m
;temp 25 150
.model IRF630 D Is=785p N=1.33849 Rs=21m*chg Eg=1.11
+ XTI=4.53261 Tnom=25 trs1=3.56m tt=0.186
+ mfg="Vishay" Vrev=200 Iave=9

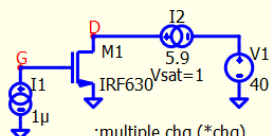
;multiple chg (*chg)
.step param temp list 25 150 param chg list 0.8 1 1.2
```



# #3 : Gate Charge – Cgs, Cgdmin, Cgdmax

## Qspice : Sensitivity Study - Gate Charge.qsch

### Ggs



```
.tran 0.05
```

```
.ic V(G)=0
```

```
.model IRF630 VDMOS Rs=0.15 Rd=0.15 Rg=2 Vto=4.08 Kp=5.63
```

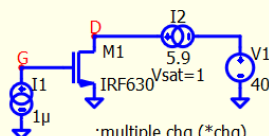
```
+ lambda=3.85m RonX=0.348 eta=75m Vt0c=-2m Is=785p N=1.33849
```

```
+ Rb=21m Eg=1.11 XTI=4.53261 trb1=3.56m Cgs=668p*chg Cgdmin=133p
```

```
+ Cgdmax=1.57n Cjo=0 tt=0.186 Tnom=25 mfg='Vishay' Vds=200
```

```
+ Ids=9 Ron=0.4 Qg=43n
```

### Ggdmin



```
.tran 0.05
```

```
.ic V(G)=0
```

```
.model IRF630 VDMOS Rs=0.15 Rd=0.15 Rg=2 Vto=4.08 Kp=5.63
```

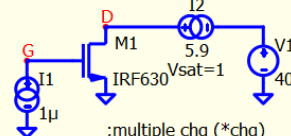
```
+ lambda=3.85m RonX=0.348 eta=75m Vt0c=-2m Is=785p N=1.33849
```

```
+ Rb=21m Eg=1.11 XTI=4.53261 trb1=3.56m Cgs=668p Cgdmin=133p*chg
```

```
+ Cgdmax=1.57n Cjo=0 tt=0.186 Tnom=25 mfg='Vishay' Vds=200
```

```
+ Ids=9 Ron=0.4 Qg=43n
```

### Ggdmax



```
.tran 0.05
```

```
.ic V(G)=0
```

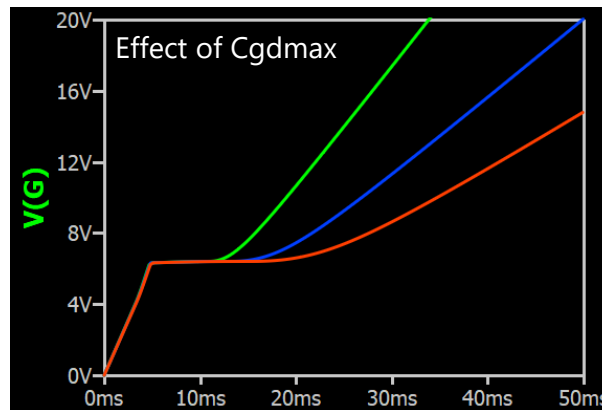
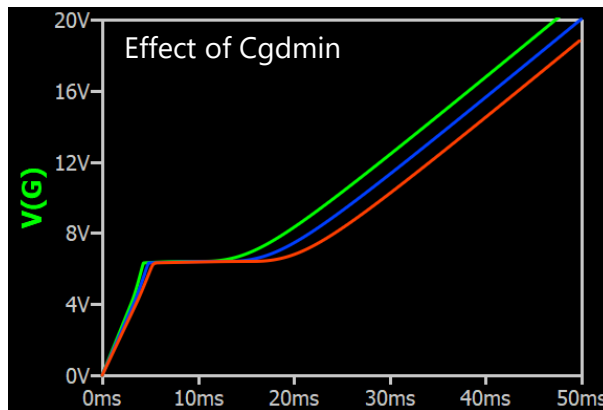
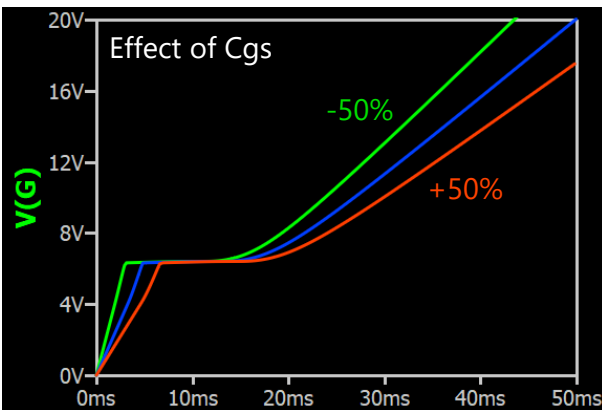
```
.model IRF630 VDMOS Rs=0.15 Rd=0.15 Rg=2 Vto=4.08 Kp=5.63
```

```
+ lambda=3.85m RonX=0.348 eta=75m Vt0c=-2m Is=785p N=1.33849
```

```
+ Rb=21m Eg=1.11 XTI=4.53261 trb1=3.56m Cgs=668p Cgdmin=133p
```

```
+ Cgdmax=1.57n*chg Cjo=0 tt=0.186 Tnom=25 mfg='Vishay' Vds=200
```

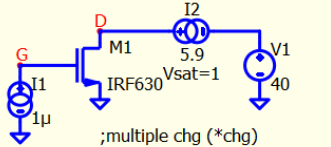
```
+ Ids=9 Ron=0.4 Qg=43n
```



# #3 : Gate Charge – Rs, Vto, Kp (from Output Characteristic Parameters)

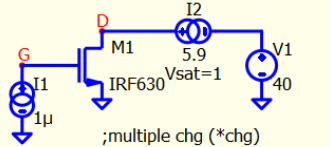
## Qspice : Sensitivity Study - Gate Charge.qsch

Rs



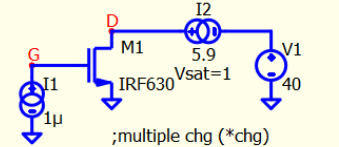
```
.tran 0.05
.ic V(G)=0
.model IRF630 VDMOS Rs=0.15*chg Rd=0.15 Rg=2 Vto=4.08 Kp=5.63
+ lambda=3.85m RonX=0.348 eta=75m Vt0tc=-2m Is=785p N=1.33849
+ Rb=21m Eg=1.11 XTI=4.53261 trb1=3.56m Cgs=668p Cgdmin=133p
+ Cgdmax=1.57n Cjo=0 tt=0.186 Tnom=25 mfg="Vishay" Vds=200
+ Ids=9 Ron=0.4 Qg=43n
```

Vto

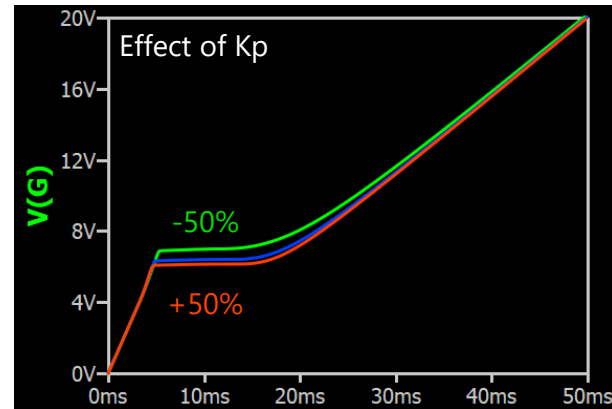
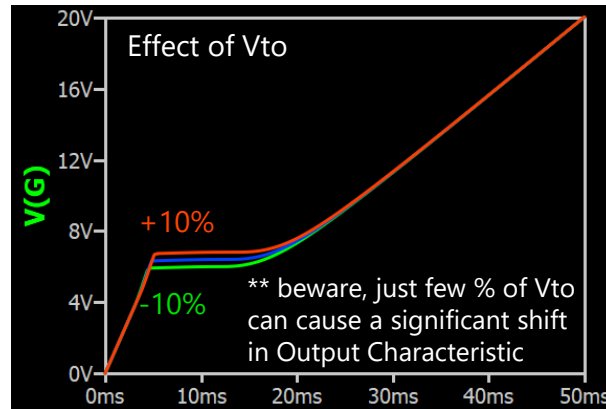
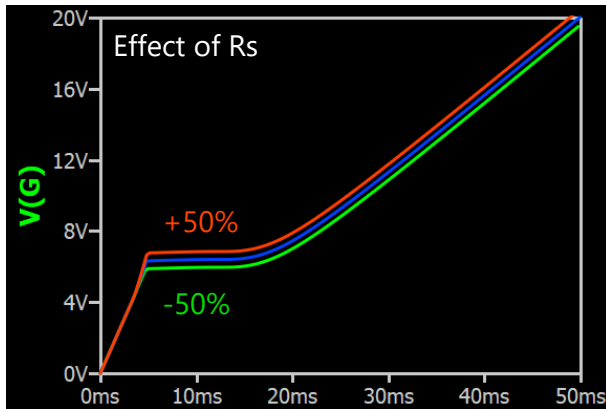


```
.tran 0.05
.ic V(G)=0
.model IRF630 VDMOS Rs=0.15 Rd=0.15 Rg=2 Vto=4.08*chg Kp=5.63
+ lambda=3.85m RonX=0.348 eta=75m Vt0tc=-2m Is=785p N=1.33849
+ Rb=21m Eg=1.11 XTI=4.53261 trb1=3.56m Cgs=668p Cgdmin=133p
+ Cgdmax=1.57n Cjo=0 tt=0.186 Tnom=25 mfg="Vishay" Vds=200
+ Ids=9 Ron=0.4 Qg=43n
```

Kp



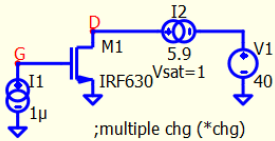
```
.tran 0.05
.ic V(G)=0
.model IRF630 VDMOS Rs=0.15 Rd=0.15 Rg=2 Vto=4.08 Kp=5.63*chg
+ lambda=3.85m RonX=0.348 eta=75m Vt0tc=-2m Is=785p N=1.33849
+ Rb=21m Eg=1.11 XTI=4.53261 trb1=3.56m Cgs=668p Cgdmin=133p
+ Cgdmax=1.57n Cjo=0 tt=0.186 Tnom=25 mfg="Vishay" Vds=200
+ Ids=9 Ron=0.4 Qg=43n
```



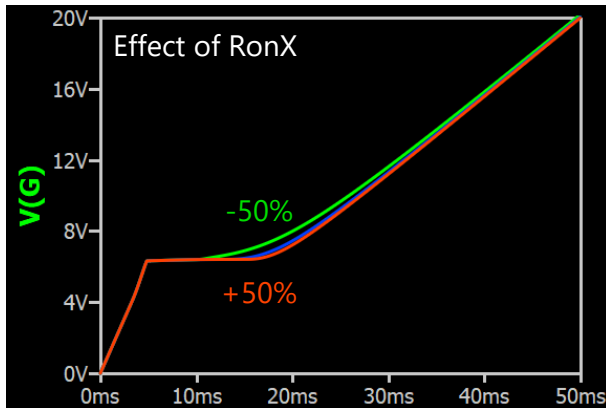
# #3 : Gate Charge – Rs, Vto, Kp (from Output Characteristic Parameters)

## Qspice : Sensitivity Study - Gate Charge.qsch

RonX



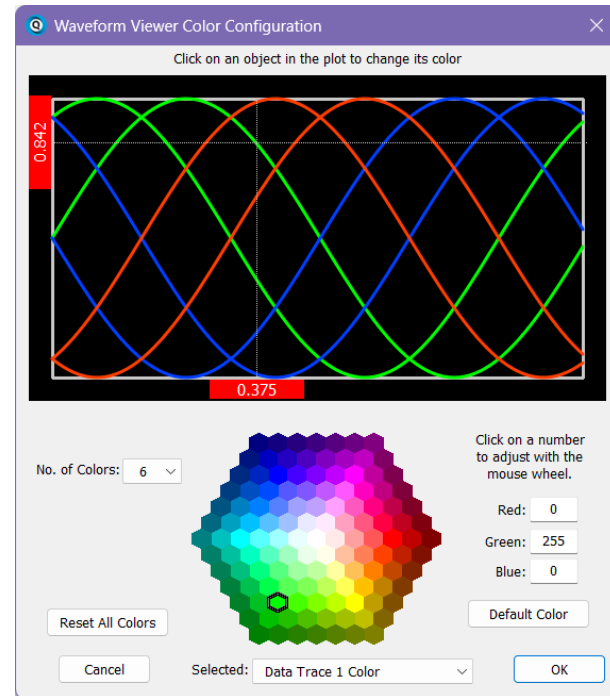
```
.tran 0.05
.ic V(G)=0
.model IRF630 VDMOS Rs=0.15 Rd=0.15 Rg=2 Vto=4.08 Kp=5.63
+ lambda=3.85m RonX=0.348*chg eta=75m Vt0tc=-2m Is=785p N=1.33849
+ Rb=21m Eg=1.11 Xf1=4.53261 trb1=3.56m Cgs=668p Cgdmin=133p
+ Cgdmax=1.57n Cjo=0 tt=0.186 Tnom=25 mfg="Vishay" Vds=200
+ Ids=9 Ron=0.4 Qg=43n
```



# Waveform Viewer Color Configuration for Sensitivity Study

- In sensitivity study, as triple sweep is used in Output Characteristic and Body Diode, color trace in waveform viewer is setup as

- Data Trace 1 Color : [0,255,0]
- Data Trace 2 Color : [0,255,0]
- Data Trace 3 Color : [0,63,255]
- Data Trace 4 Color : [0,63,255]
- Data Trace 5 Color : [255,63,0]
- Data Trace 6 Color : [255,63,0]



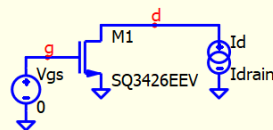
# MOSFET Model Generator

Example – Recreate  
from a model

# Determine $R_{ds(on)}$ , $V_{gs}$ , $I_{drain}$ @ $R_{ds(on)}$ and $R_{ext} \div (R_{ext} + R_{channel})$

Qspice : Preliminaries ( $R_{ds(on)}$   $V_{gs}$   $I_{drain}$  and  $R_{ext}$ ).qsch

- $R_{ext} : R_d + R_s$ 
  - $R_{ds(on)}$  is basically consist of  $R_{ext}$  (external resistance :  $R_d$ ,  $R_s$ ) and  $R_{channel}$  (channel resistance)
- To estimate  $R_{ext}$ , fully turn ON a FET model with extreme gate-source voltage, which minimized  $R_{channel}$  and  $R_{ds(on)}$  is dominated by  $R_{ext}$
- In this example,  $R_s + R_d = R_{ext} = 39.8m\Omega$ . And by extreme gate-source,  $R_{ext} = 40.6m\Omega$



```
; force Rext >> Rchannel with extreme Vgs
; therefore, Rext = Rd + Rs
.param Idrain=1

.dc Vgs 5 50 .1 ; sweep to unrealistically high for Rext
.func Rds() V(d)/I(Id)
.plot Rds()

.meas Rdsn max Rds()
.meas Ids@Rdsn min I(Id)
.meas Vgs@Rdsn min V(g)
.meas Rext min Rds()
.meas Req Rext/(Rext+(Rdsn-Rext))
```

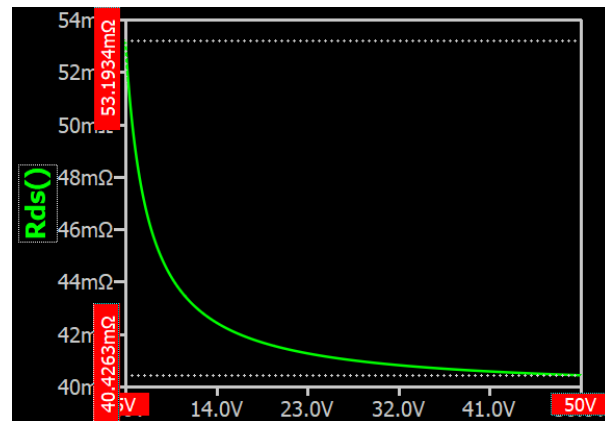
MOSFET Selection Guide

Gate Voltage:

| P/N          | Manufacturer             | Vds[V] | Ids[A] | $R_{ds(on)}[m\Omega]$ | $Q_g[nC]$ |
|--------------|--------------------------|--------|--------|-----------------------|-----------|
| BSC123N08NS3 | Infineon                 | 80     | 55     | 12.3                  | 19.0      |
| EPC2218      | EPC                      | 100    | 60     | 2.4                   | 10.5      |
| GS66508B     | GaN Systems              | 650    | 30     | 50.0                  | 6.1       |
| GS66516T     | GaN Systems              | 650    | 60     | 25.0                  | 14.2      |
| AO4262E      | Alpha & Omega            | 60     | 16     | 6.6                   | 15.0      |
| DM2600S      | ARK Microelectronics Co. | 600    | 0      | 700000.0              | 1.6       |
| FTA07N60     | ARK Microelectronics Co. | 600    | 7      | 900.0                 | 38.6      |
| SQ3426EEV    | Vishay                   | 60     | 7      | 57.0                  | 7.6       |
| UF3C065030   | Qorvo                    | 650    | 65     | 27.0                  | 51.0      |

.model SQ3426EEV VDMOS Rs=19.9m Rd=19.9m Rg=2.4 Vto=2.76 Kp=14.7  
+ lambda=0.123 RonX=2.3 eta=1.5 Rb=1.2362 Rb=1.4m  
+ Eg=1.11 XTJ=2.60857 tbt1=1.64m Cgs=700p Cgdm=40p Cjo=200p  
+ Cgdmax=700p mfg=Vishay Vds=60 Ids=7 Ron=57m Qg=7.6n

More Info Cancel OK

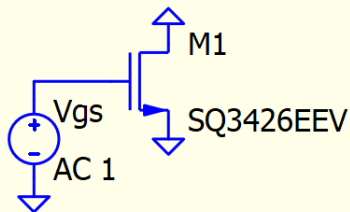


- Now put,
  - $R_{ds(on)} = 53.2m\Omega$
  - $V_{gs} @ R_{ds(on)} = 5V$
  - $I_{drain} @ R_{ds(on)} = 1A$
  - $R_{ext} = R_s + R_d = 40.6m\Omega$
  - $R_{channel} @ R_{ds(on)}$   
 $= R_{ds(on)} - R_{ext}$   
 $= 53.2m\Omega - 40.6m\Omega$   
 $= 12.6m\Omega$
  - $R_{ext} \div (R_{ext} + R_{channel})$   
 $= 40.6\Omega / (40.6\Omega + 12.6\Omega)$   
 $= 0.763\Omega$

# Determine $R_g$ from a MOSFET Model

## Qspice : Preliminaries - $R_g$ .qsch

- $R_g$ 
  - $R_g$  is series resistance in gate
  - $R_g$  can be identified with ac analysis and only read the real part with Cartesian representation
  - Now, put
    - $R_g$  = value of  $Z_r()$



```
.ac list 1Meg  
.func Zr() re(1/-I(Vgs))  
.plot Zr()  
.meas Rg param Zr()
```

