Qspice - Device Reference Guide by KSKelvin

KSKelvin Kelvin Leung

Created on 9-5-2023
Last Updated on 10-22-2023

B. Behavioral Source

B. Behavioral Source : Instance Parameters

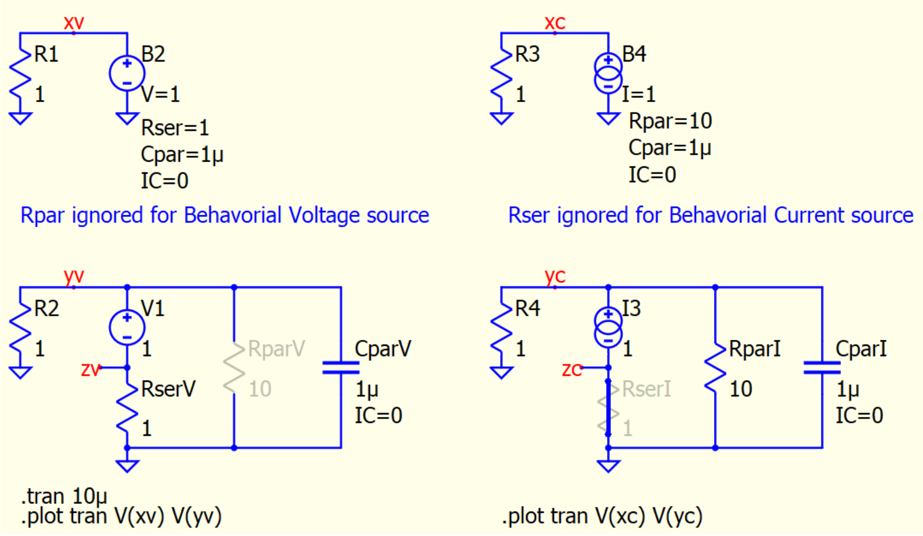
Behavioral Source Instance Parameters

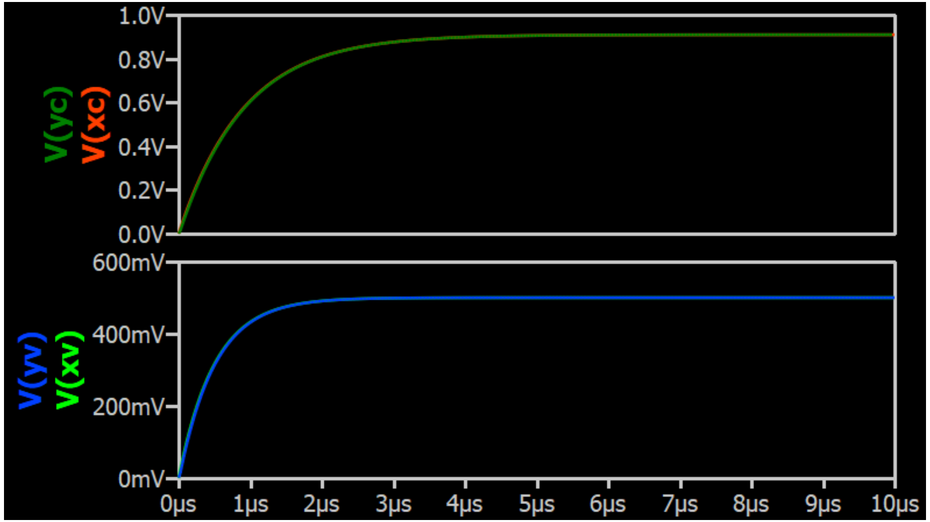
Name	Description	Units	Default
CPAR	Parallel capacitance	F	0.0
I[1]	Expression for current	A	(not set)
IC	Initial value	A or V	0.0
LAPLACE	Frequency dependence		(none)
NORTON	Use a Norton equivalent for a behavioral resistance		(not set)
R[1]	Expression for resistance	Ω	(not set)
RPAR	Parallel resistance Ignore in V	Ω	Infinite
RSER	Series resistance Ignore in I and R (Norton)	Ω	0.0
SYNTHESIZE	Use the synthesized Laplacian circuit even for .AC		(not set)
THEVENIN	Use the Thévenin equivalent for a behavioral resistance		(not set)
V[1]	Expression for voltage	V	(not set)

B. Instance Params : Rser, Rpar and Cpar

Qspice : B Source - Rpar Rser Cpar in V and I.qsch

- Rser, Rpar and Cpar in Behavioral Voltage and Current Source
  - Behavioral Voltage (V=<expression>) : Only Rser and Cpar are active
  - Behavioral Current (I=<expression>) : Only Rpar and Cpar are active
    - I don't recommend to use Rser and Rpar in Behavioral Resistance as it will be very confusing depends on Norton or Thevenin equivalent
  - In this example, IC initial value is used to allow 0V or 0A for transient simulation. As behavioral source not have effect in .ac (except for Laplace), .tran is used to reveal these parameters characteristic

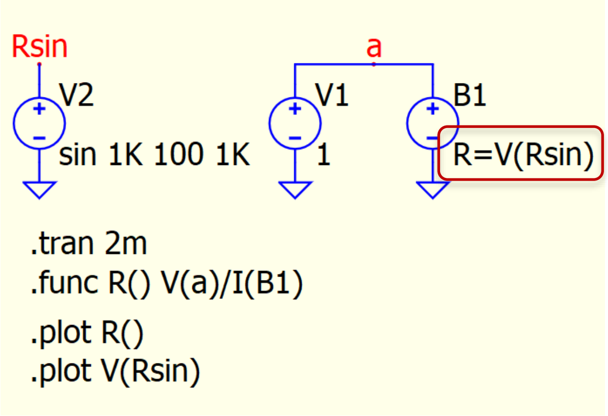


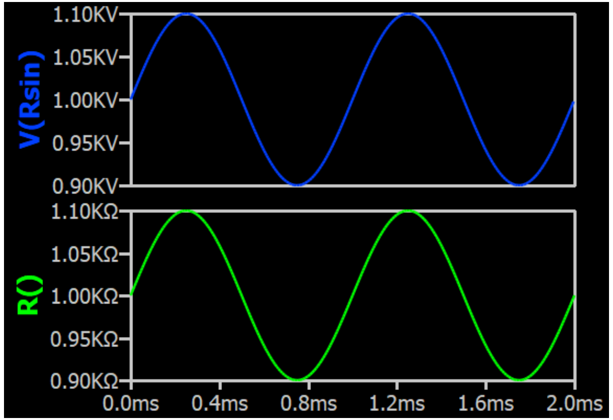


B. Instance Params : Behavioral Resistor

Qspice : B Source - Behavioral R.qsch

- Behavioral Resistor
  - Syntax : Bnnn n001 n002 R=<expression>

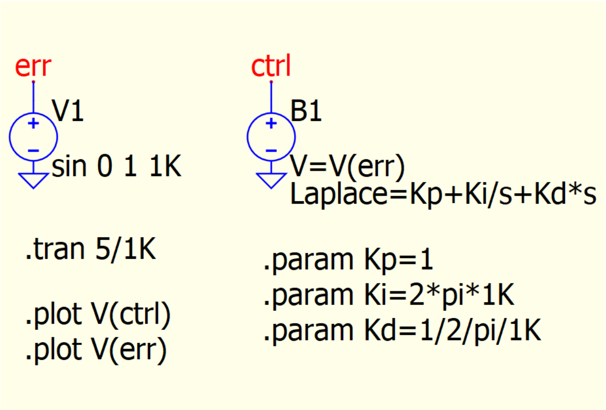


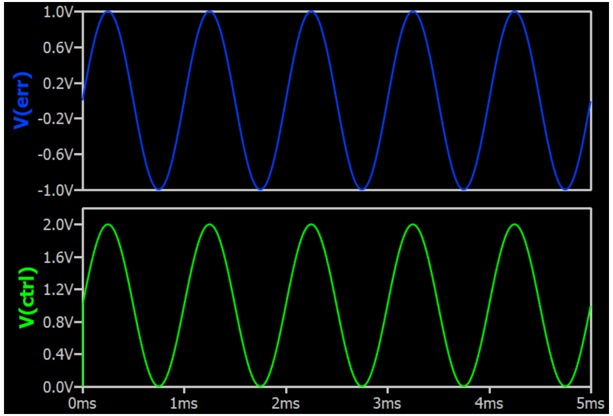


B. Instance Params : Laplace

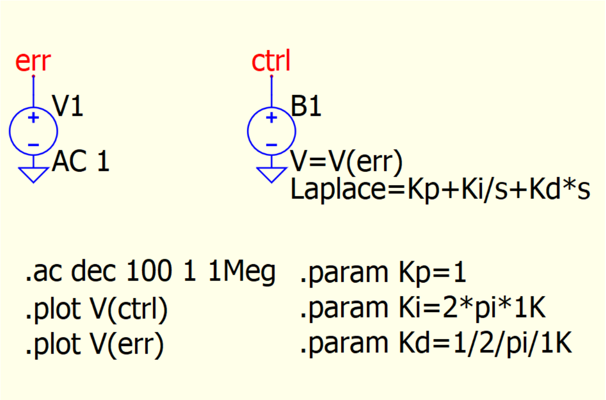
Qspice : B Source - Laplace (.tran).qsch ; B Source - Laplace (.ac).qsch

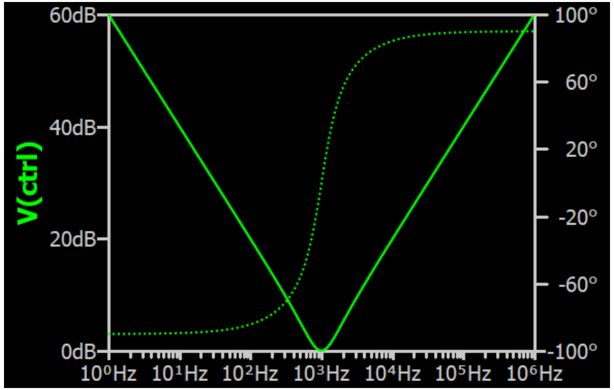
- Laplace (.tran)
  - Use Laplace equation, by adding a new attribute Laplace
  - In this simulation
    - $v_{ctrl} = \left(K_p + \frac{K_i}{s} + K_d s\right) v_{err}$





- Laplace (.ac)
  - Laplace supports .ac analysis





B. Function and Operators

HELP > Simulator > Device Reference > B. Behavioral Sources

Functions

Name		Description
abs(x)	$\lvert x \rvert$	Absolute value of x
acos(x)	$\cos^{-1} x$	arc cosine of x
arccos(x)		Synonym for acos()
acosh(x)		arc hyperbolic cosine of x
asin(x)	$\sin^{-1} x$	arc sine of x
arcsin(x)		Synonym for asin()
asinh(x)		Arc hyperbolic sine
atan(x)	$\tan^{-1} x$	Arc tangent of x
arctan(x)		Synonym for atan()
atan2(y,x)		Four quadrant arc tangent of y/x
atanh(x)		Arc hyperbolic tangent
buf(x)		1 if x > .5, else 0
ceil(x)		Integer equal or greater than x
cos(x)	$\cos x$	Cosine of x
cosh(x)		Hyperbolic cosine of x
ddt(x)	$dx/dtime$	Time derivitive x
delay(x,y)		x delayed by y
delay(x,y,z)		x delayed by y, but store no more than z history
dlim(x,y,z)		x bounded by y which it asymptotically starts to approach at y+z as a first inverse order Laurent series
exp(x)	e^x	e to the x
floor(x)		Integer equal to or less than x
hypot(x,y)	$\sqrt{x^2+y^2}$	sqrt(x^2 + y^2)
idt(x,y,z)		Time integral of x with initial condtion of y reset when z > .5

$$\int x\,dtime + y$$

if(x,y,z)		If x > .5, then y else z
int(x)		Convert x to integer
inv(x)		0. if x > .5, else 1.
limit(x,y,z)		Intermediate value of x, y, and z
ln(x)	$\log_e x$	Natural logarithm of x
log(x)	$\log_e x$	Alternate syntax for ln()
log10(x)	$\log_{10} x$	Base 10 logarithm
max(x,y)		The greater of x or y
min(x,y)		The smaller of x or y
pow(x,y)	x^y	x^y
pwr(x,y)	$\lvert x \rvert^y$	abs(x)^y
pwrs(x,y)		sgn(x)*abs(x)^y
random(x)		Random number from 0. to 1. depending on the integer value of x. Interpolation between random numbers is linear for non-integer x.
sin(x)	$\sin x$	Sine of x
sinh(x)		Hyperbolic sine of x
sqrt(x)	$\sqrt{x}$	Square root of x
table (x,a,b,c,d,...)		Interpolate x from the look-up table given as a set of pairs of constant values.
tan(x)	$\tan x$	Tangent of x.
tanh(x)		Hyperbolic tangent of x
ulim(x,y,z)		x bounded by y which it asymptotically starts to approach at y-z as a first inverse order Laurent series

Operators grouped in reverse order of precedence of evaluation

Operand	Description
&	Boolean AND
|	Boolean OR
>	True if expression on the left is greater than the expression on the right.
<	True if expression on the left is less than the expression on the right.
>=	True if expression on the left is greater than or equal the expression on the right.
<=	True if expression on the left is less than or equal the expression on the right.
+	Addition
-	Subtraction
*	Multiplication
/	Division
**	** / ^ Raise left hand side to power of right hand side. Same as '^'.
!	Boolean not the following expression.

Available Function in B source not listed

- Trunc(x) ; floor(x) ; int(x) : rounded down integer
- Rint(x) ; round(x) : rounded to nearest integer
- Ceil(x) : rounded up integer
- Ustep(x) : x > 0 ? 1 : 0
- Uramp(x) : x > 0 ? x : 0

Available Variable or Constant not listed in HELP

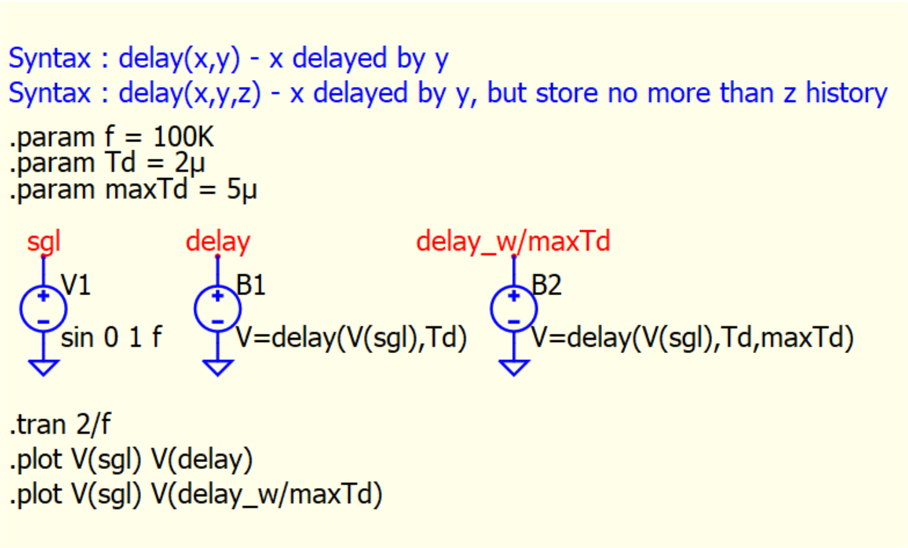
- Time : Simulation Time
- Temp : Temperature
- PI : 3.14159265358979323846
- E : 2.7182818284590452354
- K : 1.380649e-23 J/°K
- Q : 1.602176487e-19 Coulomb

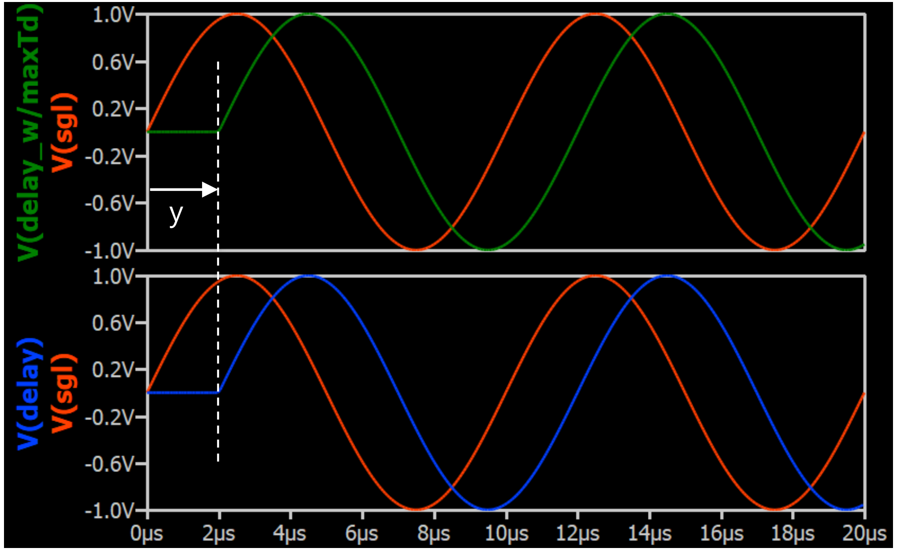
B. Function and Operators – delay(x,y) or delay(x,y,z)
Qspice : B Source - delay fix.qsch

- delay(x,y) or delay(x,y,z)
  - Delay(x,y,z) can reduce the amount of waveform memory that must be stored

delay(x,y)	x delayed by y
delay(x,y,z)[1]	x delayed by y, but store no more than z history

- y can be parameter and z must be fixed constant
- y must less than z or error will return

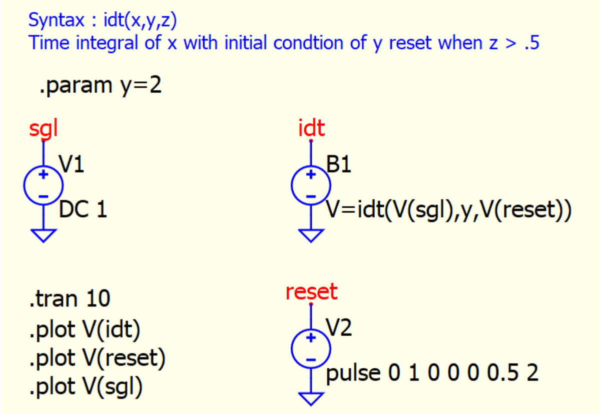


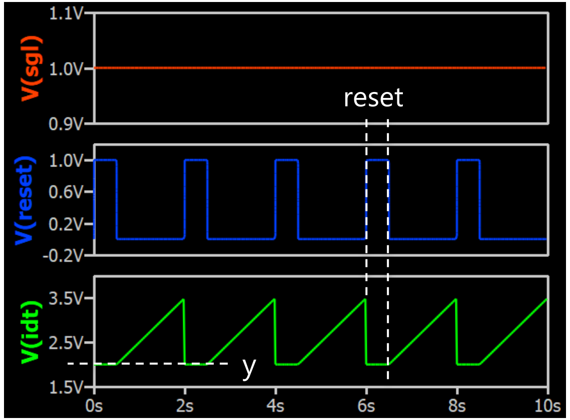


B. Function and Operators – Integral and Time Derivative idt(x,y,z) and ddt(x)

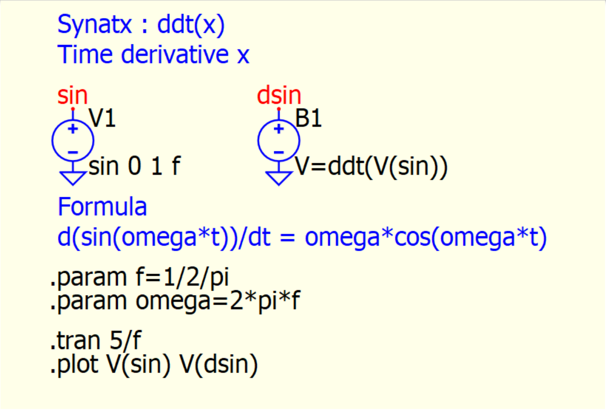
Qspice : B Source - idt.qsch ; B Source - ddt.qsch

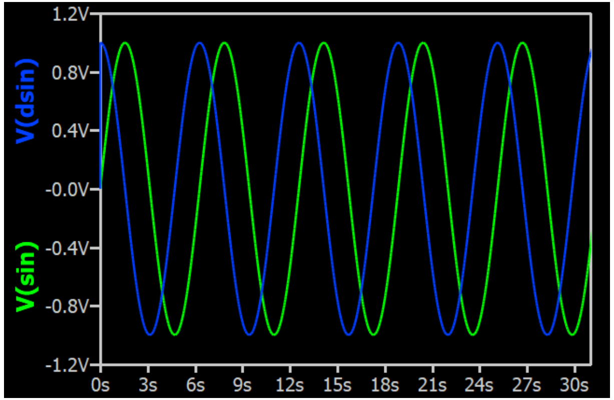
- idt(x,y,z)
  - Time Integral of x
  - $= \int x\, dt + y$
  - y is initial condition equivalent DC value during integral reset
  - z is to reset integral





- ddt(x)
  - Time derivative
  - $= \frac{dx}{dt}$

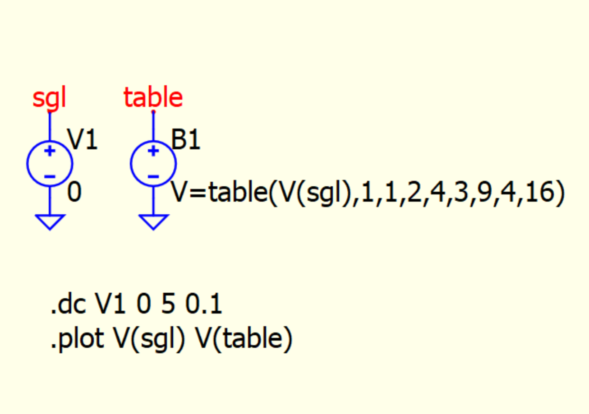


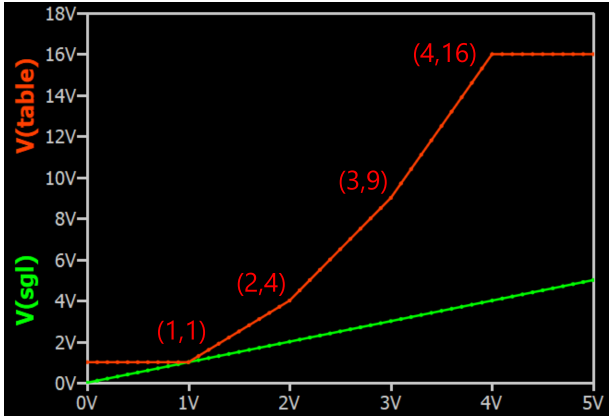


B. Function and Operators – table(x,a,b,c,d,…) and limit(x,y,z)

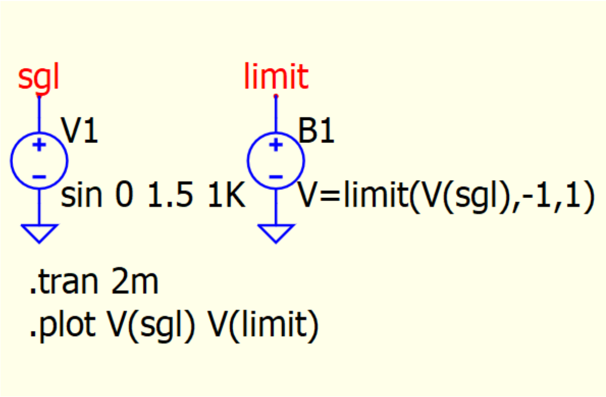
Qspice : B Source - table.qsch ; B Source - limit.qsch

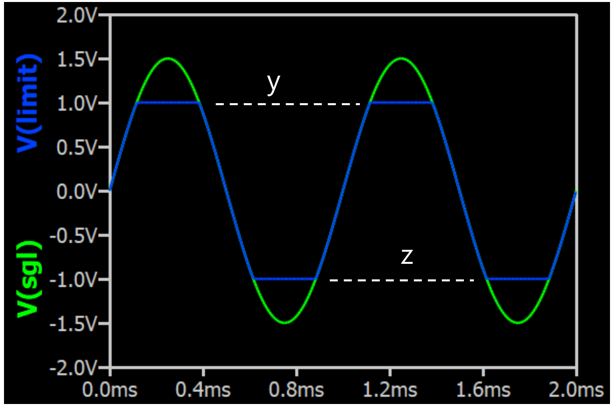
- Table(x,a,b,c,d,…)
  - Interpolate x from the look-up table given as a set of pairs of constant values





- limit(x,y,z)
  - Intermediate value of x, y, and z

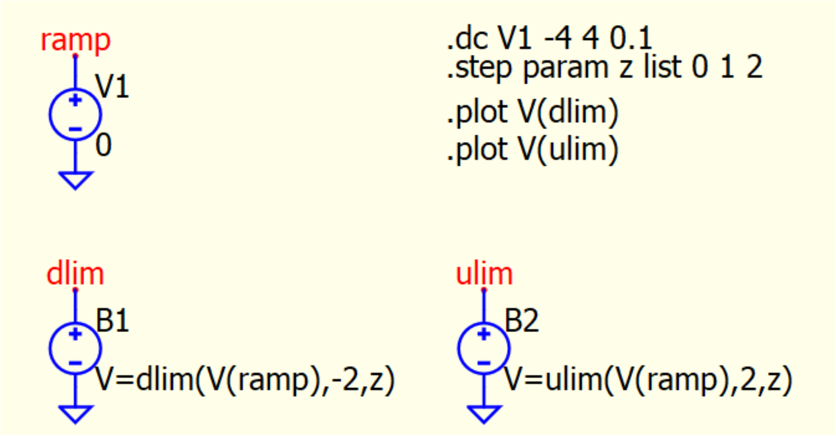


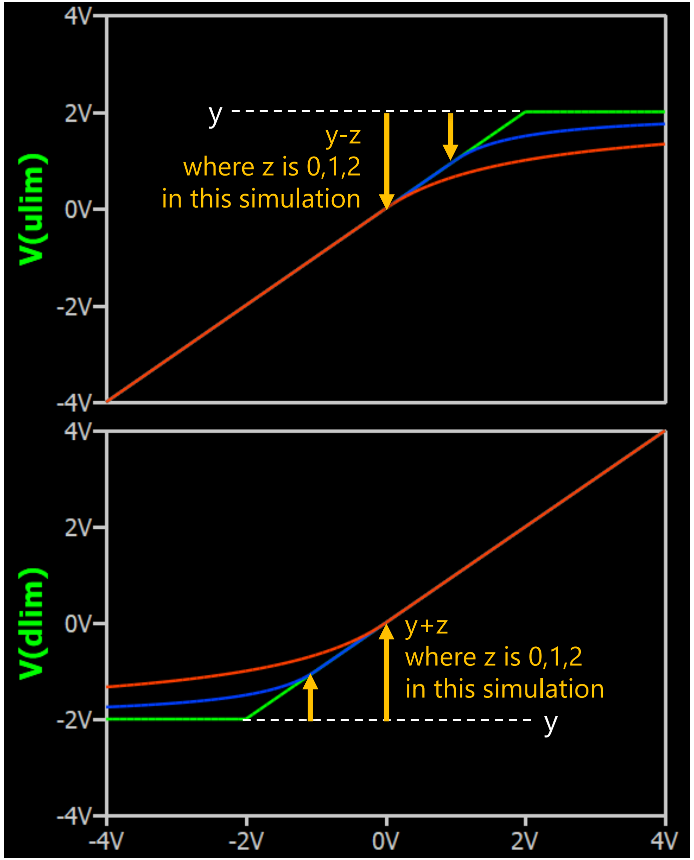


B. Function and Operators – dlim(x,y,z) and ulim(x,y,z)

Qspice : B Source - dlim ulim.qsch

- dlim(x,y,z) and ulim(x,y,z)
  - dlim(x,y,z) : x bounded by y which it asymptotically starts to approach at y+z as a first inverse order Laurent series
  - ulim(x,y,z) : x bounded by y which it asymptotically starts to approach at y-z as a first inverse order Laurent series
  - These functions are used for soft limit

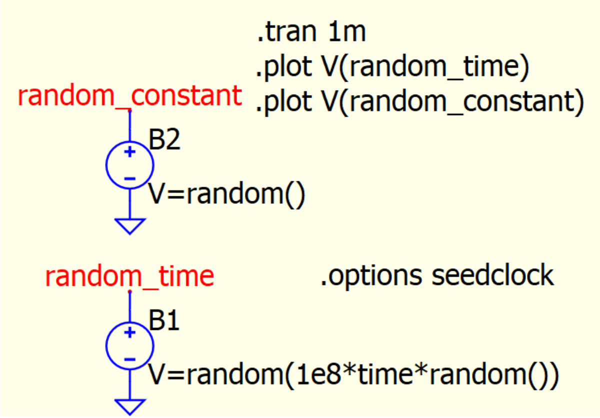


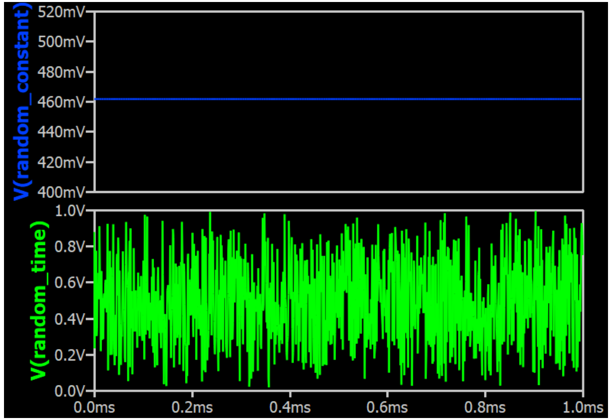


B. Function and Operators – random(x), variable/constant

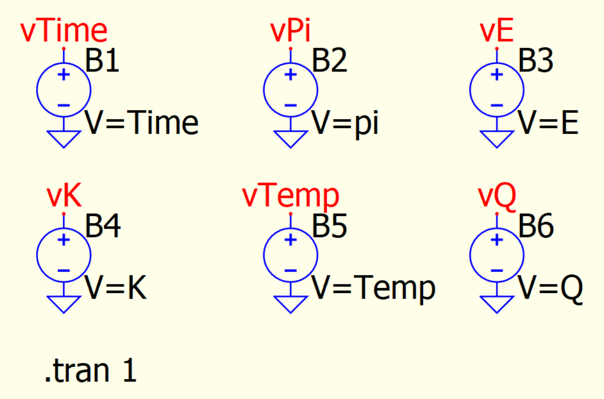
Qspice : B Source – random.qsch ; B Source - Buildin Variable Constant.qsch

- Random(x)
  - Random number from 0. to 1. depending on the integer value of x
  - The one without arguments must be processed in the preprocessor (explained by Mike Engelhardt)
  - To create a random sequence in transient, x must change in each time step : i.e. random(1e8*time), multiple with 1e8 is for x to be a large integer for random generation





- Build-in Variable / Constant
  - Time : Simulation Time
  - Temp : Temperature
  - PI : 3.14159265358979323846
  - E : 2.7182818284590452354
  - K : 1.380649e-23 J/°K
  - Q : 1.602176487e-19 Coulomb



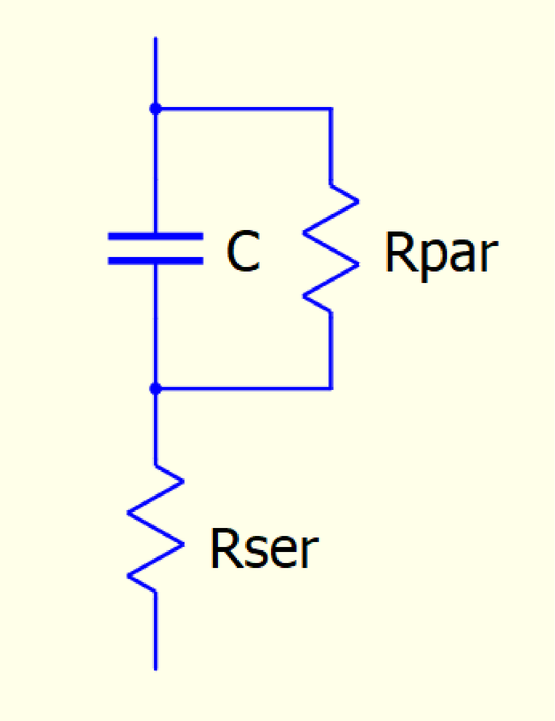
C. Capacitor

Capacitor C Instance Parameters in Qspice HELP

Capacitor Instance Parameters

Name	Description	Units	Default
CAPACITANCE	Capacitance(not usually labeled)	F	0.0
CSAT	Capacitance asymptotically approached in saturation	F	10% of CAPACITANCE
IC	Initial voltage on capacitor	V	0.0
L[1]	Length	m	0.0
M	Number of identical parallel devices		1.0
RPAR	Equivalent parallel resistance	Ω	Infinite
RSER	Equivalent series resistance	Ω	0.0
SATFRAC	Fractional drop in capacitance at VSAT		0.7
TEMP	Instance temperature	°C	Circuit temperature
VSAT	Voltage that drops capacitance to SATFRAC×CAPACITANCE	V	Infinite
W[1]	Width	m	0.0

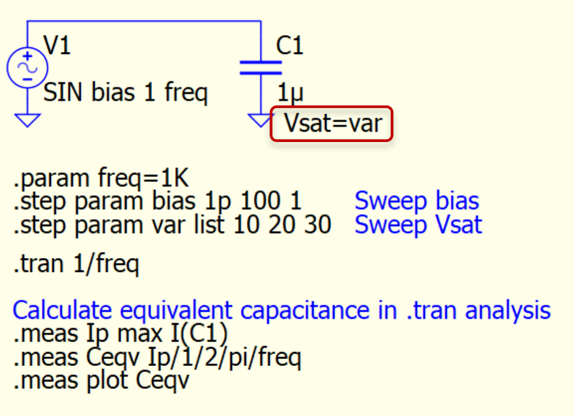
Rpar and Rser in C model

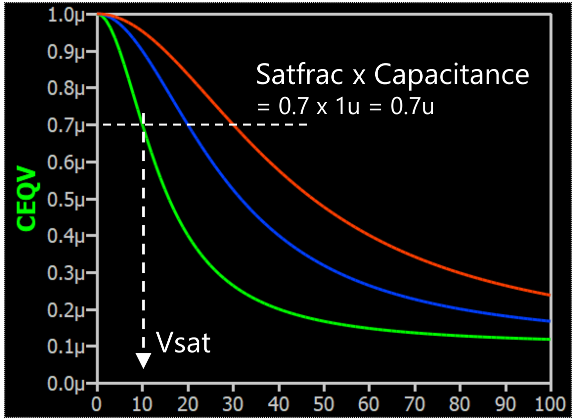


C. Instance Params : Vsat, Csat, Satfrac : For Nonlinear Capacitance

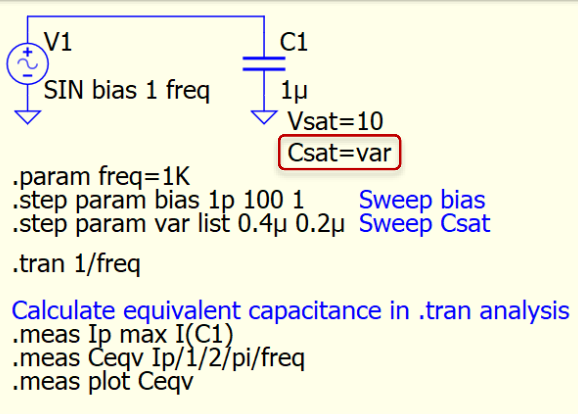
Qspice : C Capacitor - Vsat (.ac).qsch ; C Capacitor - Csat (.tran).qsch

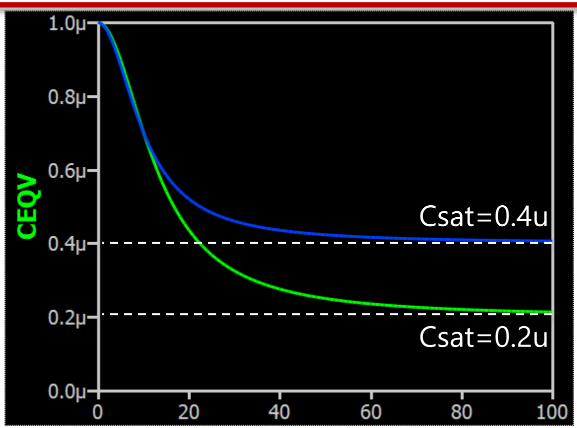
- Vsat and Satfrac
  - **Vsat** : Voltage that drops capacitance to ***Satfrac x Capacitance***
  - **Satfrac** : Fractional drop in capacitance at Vsat
    - default = 0.7





- Csat
  - **Csat** : Capacitance asymptotically approached in saturation
    - ** Vsat must be set to see it effect

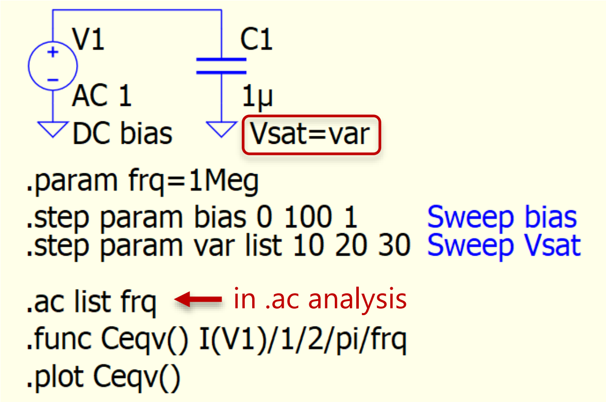


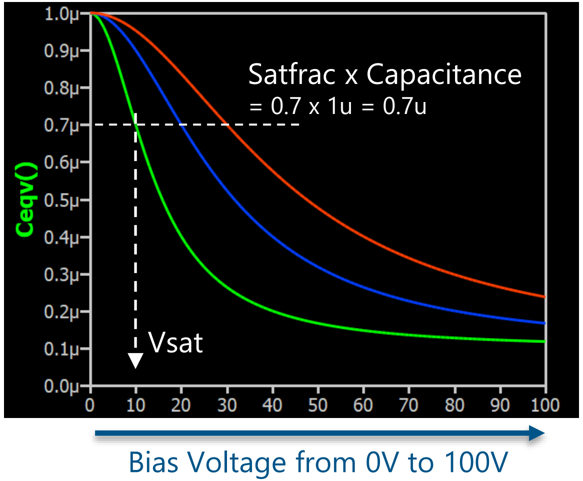


C. Instance Params : Replicate previous graph with .ac analysis

Qspice : C Capacitor - Vsat (.ac).qsch

- Vsat and Satfrac
  - **Vsat** : Voltage that drops capacitance to ***Satfrac x Capacitance***
  - **Satfrac** : Fractional drop in capacitance at Vsat
    - default = 0.7

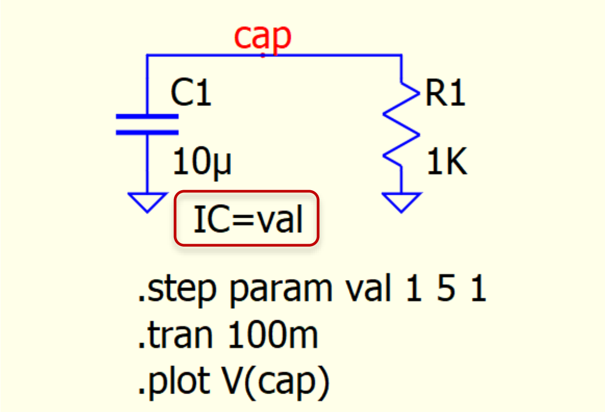


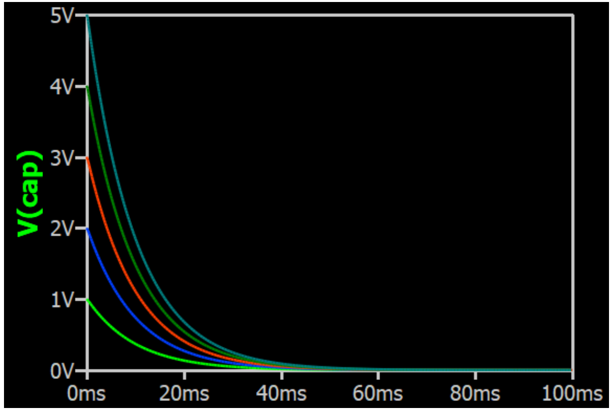


- Capacitance equation
  - $X_C = \frac{1}{\omega C} = \frac{V_C}{I_C}$
  - $C = \frac{|I_C|}{|V_C|}\frac{1}{\omega} = \frac{|I_C|}{2\pi f |V_C|}$
  - This formula is used to calculate equivalent capacitance (small signal model) at different capacitor bias voltage

C. Instance Params : IC Initial Condition
Qspice : Capacitor - IC.qsch

- IC
  - IC : Initial Condition
  - **Default IC=0**
  - Use in transient analysis for initial voltage of capacitor at time=0s





D. Diode

Diode Model Parameters

Diode Model Parameters in Qspice HELP

Diode Instance Parameters

Name	Description	Units	Default
AREA	Relative area		1.0
M	Number of identical parallel devices		1.0
TEMP	Instance temperature	°C	Circuit temperature

Diode Model Parameters

Name	Description	Units	Default
AF	Flicker noise exponent	1.	1.0
BV	Reverse breakdown voltage	V	Infinite
CJO	Zero-bias junction capacitance	F	0.0
EG	Activation energy	eV	1.11
FC	Forward-bias depletion capacitance coefficient		0.5
GMAX	Maximum conductivity(straight-line extension)	℧	10000.
GP	Parallel conductivity added in lieu of global Gmin	℧	0.
IBV	Current at breakdown voltage	A	1e-10
IBVL	Low-level reverse breakdown knee current	A	0.0
IKF	High-injection knee current	A	1e308
IS	Saturation current	A	1e-14
ISR	Recombination current parameter	A	0.0
KF	Flicker noise coefficient		0.0
M	Grading coefficient		0.5
N	Emission coefficient		1.0
NBV	Reverse breakdown emission coefficient		1.0
NBVL	Low-level reverse breakdown emission coefficient		1.0
NR	ISR emission coefficient		2.0
RS	Series resistance	Ω	0.0
TBV1	1st order BV temperature coefficient	$°C^{-1}$	0.0
TBV2	2nd order BV temperature coefficient	$°C^{-2}$	0.0
TIKF	IKF temp coefficient	$°C^{-1}$	0.0
TNOM	Parameter measurement temperature(aka TREF)	°C	27
TG11	1st order GP temperature coefficient[1]	$°C^{-1}$	0.0
TGP2	2nd order GP temperature coefficient[1]	$°C^{-2}$	0.0
TRS1	1st order RS temperature coefficient[1]	$°C^{-1}$	0.0
TRS2	2nd order RS temperature coefficient[1]	$°C^{-2}$	0.0
TT	Transit-time[2]	sec	0.0
VJ	Junction potential	V	1.0
XTI	Saturation current temperature exponent		3.0

.model available parameters but not in HELP

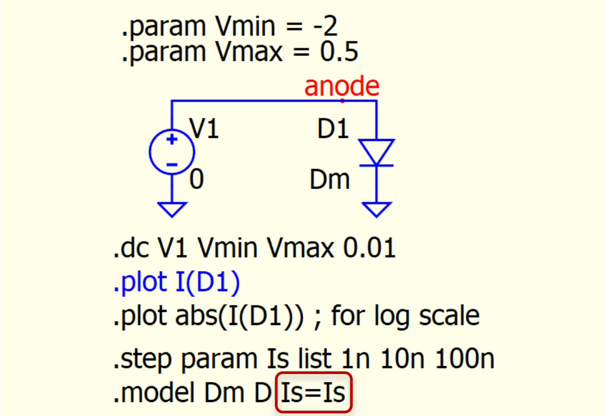
- VP : Soft reverse recovery parameter (Default VP=0.01)

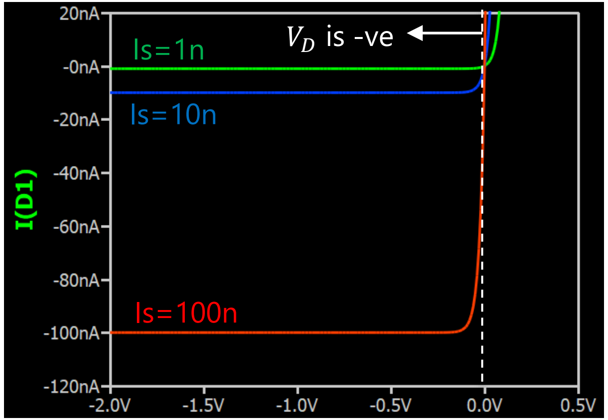
.model parameters only for information display but no electrical behavior

- MFG : manufacturer name
- Vrev : Peak reverse voltage
- Iave : Average current rating

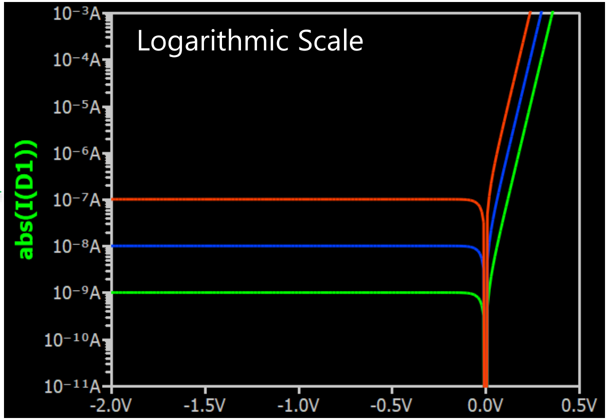
D. Diode Model (I-V Characteristic) : IS
Qspice : Dmodel - IS.qsch

- IS
  - Is : Saturation current
    - Saturation current in reverse region
  - **Default IS = 1e-14A**
  - $I_D = I_s\left(e^{\frac{qV_D}{nkT}} - 1\right)$
    - $\frac{kT}{q}$ is called thermal voltage
      - q : electronic charge
        - 1.602176487e-19 Coulomb
      - k : Boltzmann constant
        - 1.380649e-23 J/°K
      - T : Temperature in Kelvin
        - $T = T_{celsius} + 273.15°C$
    - V_D : Diode voltage
    - n : emission coefficient





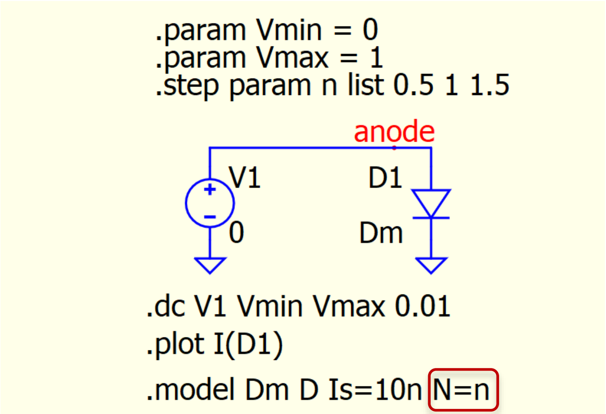
$|I_d|$
Magnitude only

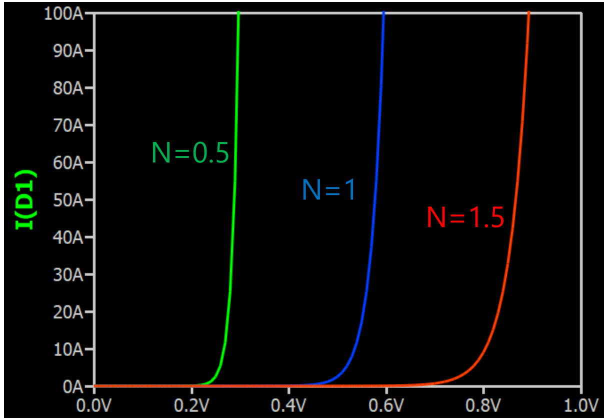


D. Diode Model (I-V Characteristic) : N and Rs

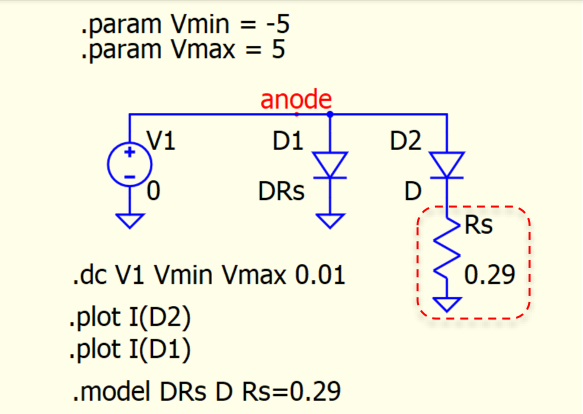
Qspice : Dmodel - N.qsch / Dmodel - Rs.qsch

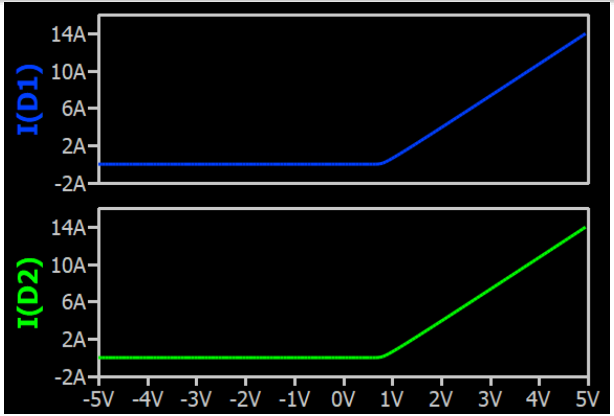
- N
  - n : emission coefficient
  - **Default N=1**
  - $I_D = I_s\left(e^{\frac{qV_D}{nkT}} - 1\right)$
  - N affects threshold voltage in forward bias





- RS
  - Rs : Series resistance
  - **Default RS=0Ω**
  - This is equivalent to resistor added in series to diode
  - ** V_D in $I_D = I_s\left(e^{\frac{qV_D}{nkT}} - 1\right)$ formula only represent diode model voltage drop. If RS is added, diode model anode to cathode voltage is $V_D + I_D R_S$





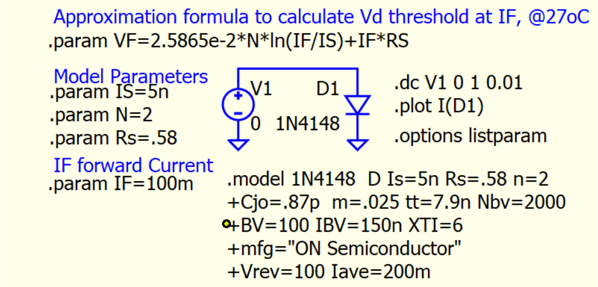
Forward Voltage (VF) or Threshold @ Specified Forward Current (IF)

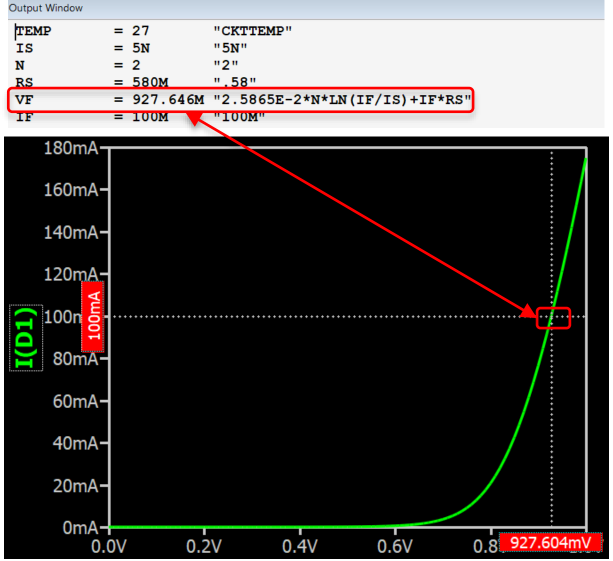
** Condition : Recombination current is not used : ISR=0

- Background
  - In datasheet, it generally specify forward threshold by defining as forward voltage drop (VF) at a specified forward current level (IF)

- Diode model include RS
  - $V_{D,ext} = V_D + I_D R_S$ and $I_d = I_s\left(e^{\frac{qV_D}{nkT}} - 1\right)$
    - where $V_{D,ext}$ is diode voltage drop including series resistance
  - Re-arrange I_d formula : $V_D = n\frac{kT}{q}\ln\left(\frac{I_d}{I_S} + 1\right)$
  - Therefore,
    - $V_{D,ext} = n\frac{kT}{q}\ln\left(\frac{I_d}{I_S} + 1\right) + I_D R_S$
  - Substitute $V_{D,ext}$ by VF and I_D by IF and Qspice .model parameters
    - $\mathrm{V_F} = \mathrm{N}\frac{kT}{q}\ln\left(\frac{\mathrm{IF}}{\mathrm{IS}} + 1\right) + \mathrm{IF} \times \mathrm{Rs}$
      - where Qspice default temperature T is 27°C = 300.15K
      - k=1.380649e-23 J/°K and q=1.602176487e-19C → $\frac{kT}{q}$ = 2.5865e-2
      - Equation can be simplified with IF ≫ IS where $\left(\frac{\mathrm{IF}}{\mathrm{IS}} + 1\right) \to \frac{\mathrm{IF}}{\mathrm{IS}}$

- Simplified Results in Qspice
  - VF = 2.5865e-2***N***ln(**IF**/**IS**) + **IF** * **RS**
    - IS, N and RS are in diode .model
    - IF is specified forward current for diode threshold (e.g. IF=100mA)



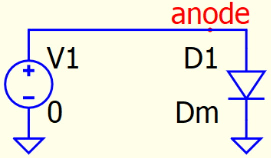


D. Diode Model (I-V Characteristic : Breakdown) : BV, IBV and NBV

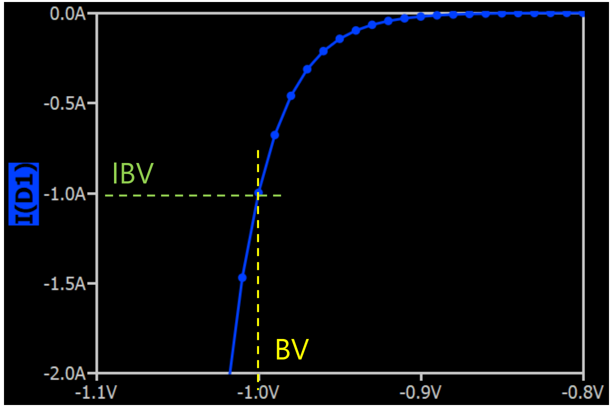
Qspice : Dmodel - BV IBV.qsch / Dmodel - NBV.qsch

- BV and IBV
  - BV : Breakdown Voltage
  - IBV : Current at breakdown voltage
  - **Default BV=Infinite**
  - **Default IBV=1e-10**
  - Breakdown region eqn
    - $I_D = -\mathrm{IBV}\, e^{-\frac{q(\mathrm{BV}+V_D)}{kT}}$

```
.param Vmin = -1.2
.param Vmax = 0
```

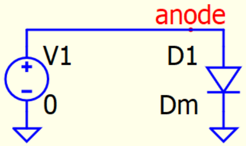



```
.dc V1 Vmin Vmax 0.01
.plot I(D1)
.model Dm D BV=1 IBV=1
```

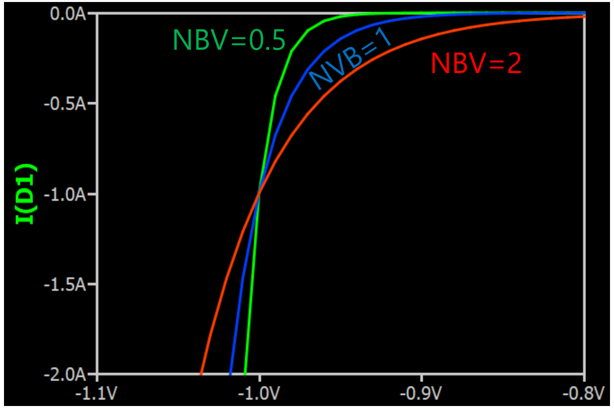


- NBV
  - NBV : Reverse breakdown emission coefficient
  - **Default NBV=1**
  - Change the sharpness of breakdown reverse current

```
.param Vmin = -1.2
.param Vmax = 0
```




```
.dc V1 Vmin Vmax 0.01
.plot I(D1)
.model Dm D BV=1 IBV=1 NBV=nbv
.step param nbv list 0.5 1 2
```

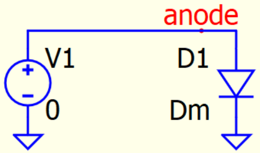


D. Diode Model (I-V Characteristic : Breakdown) : IBVL and NBVL

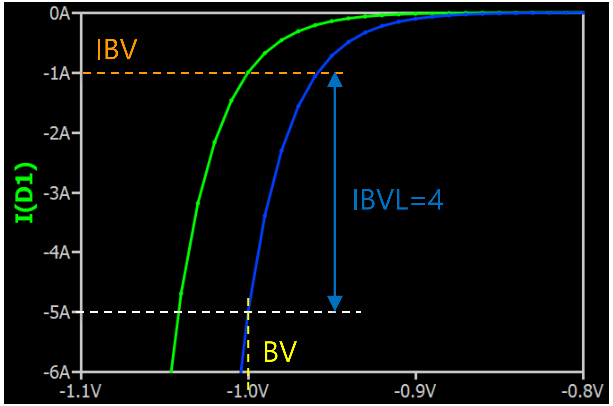
Qspice : Dmodel - IBVL.qsch / Dmodel - NBVL.qsch

- IBVL
  - IBVL : low-level reverse breakdown knee current
  - **Default IBVL=1**

```
.param Vmin = -1.2
.param Vmax = -0.6
```

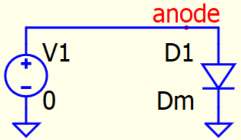



```
.dc V1 Vmin Vmax 0.01
.plot I(D1)
.step param ibvl list 0 4
.model Dm D BV=1 IBV=1 IBVL=ibvl
```

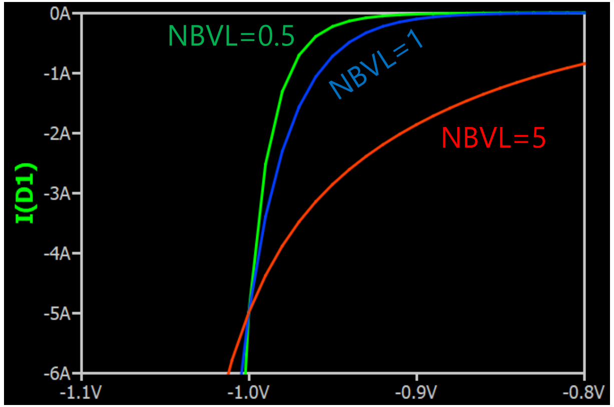


- NBVL
  - NBVL : Low-level reverse breakdown emission coefficient
  - **Default NBVL=1**
  - Change the sharpness of breakdown reverse current when IBVL is used

```
.param Vmin = -1.2
.param Vmax = -0.6
```




```
.dc V1 Vmin Vmax 0.01
.plot I(D1)
.step param nbvl list 0.5 1 5
.model Dm D BV=1 IBV=1 IBVL=4
+NBVL=nbvl
```

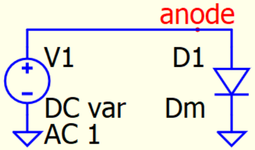


D. Diode Model (Capacitance) : CJO and M

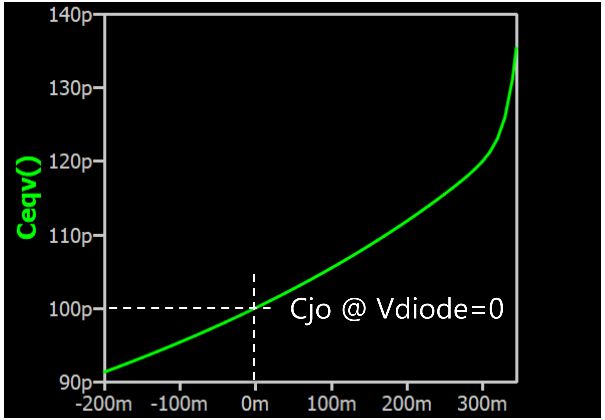
Qspice : Dmodel - CJO.qsch / Dmodel - M.qsch

- CJO
  - Cjo : Zero-bias junction capacitance
  - **Default CJO=0F**
  - $C_j = \dfrac{C_{jo}}{\left(1-\frac{V_D}{\Phi_0}\right)^m}$
    - Φ_0 : Junction potential (VJ)
    - m : Grading coefficient
      - M = 0.33 : linearly garded
      - M = 0.5 : abrupt junction

```
.param Vmin = -0.2
.param Vmax = 0.345
.param f = 1K
```

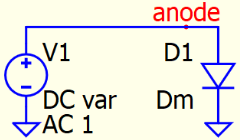



```
.model Dm D Cjo=100p
.func Zim() imag(V(anode)/I(D1))
.func Ceqv() -1/2/pi/f/Zim()

.ac list f
.step param var Vmin Vmax 0.01
.plot Ceqv()
```

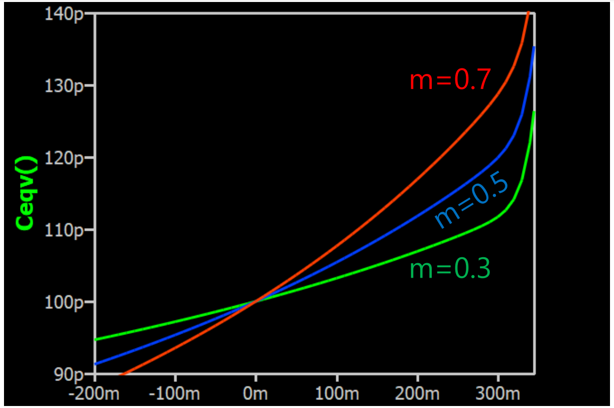


- M
  - m : grading coefficient
  - **Default M=0.5**
  - $C_j = \dfrac{C_{jo}}{\left(1-\frac{V_D}{\Phi_0}\right)^m}$
    - m : Grading coefficient
      - M = 0.33 : linearly garded
      - M = 0.5 : abrupt junction

```
.param Vmin = -0.2
.param Vmax = 0.345
.param f = 1K
```



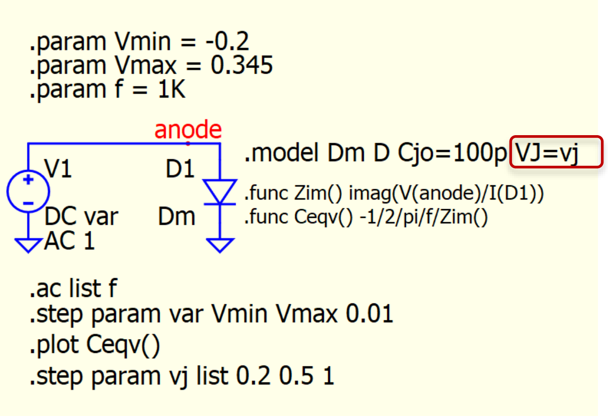

```
.model Dm D Cjo=100p m=m
.func Zim() imag(V(anode)/I(D1))
.func Ceqv() -1/2/pi/f/Zim()

.ac list f
.step param var Vmin Vmax 0.01
.plot Ceqv()
.step param m list 0.3 0.5 0.7
```

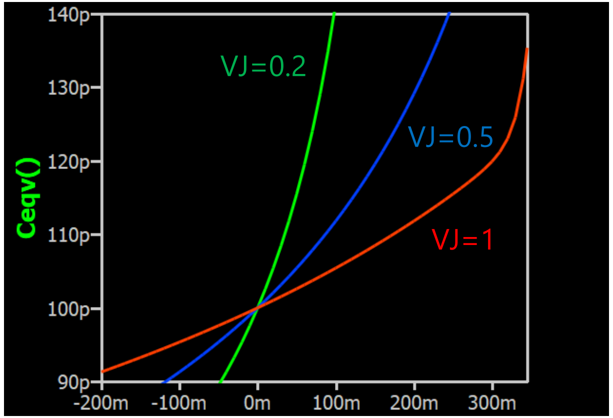


D. Diode Model (Capacitance) : VJ

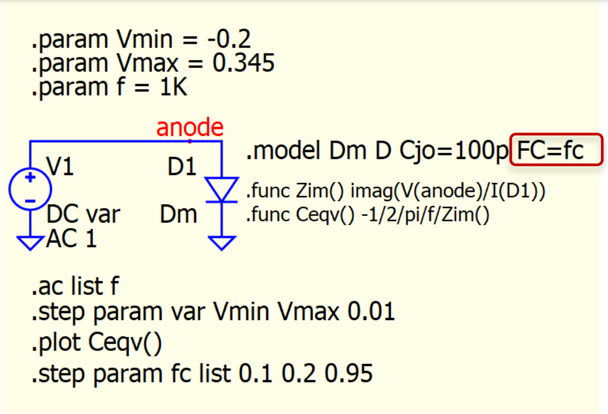
Qspice : Dmodel - VJ.qsch

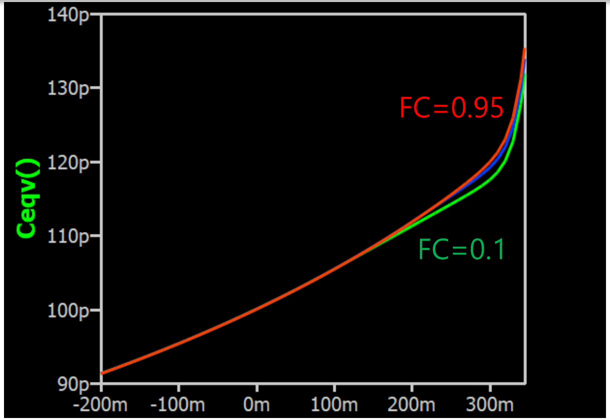
- VJ
  - Vj : Junction potential
  - **Default VJ=1V**
  - $C_j = \frac{C_{jo}}{\left(1-\frac{V_D}{\Phi_0}\right)^m}$
    - Φ_0 : Junction potential (VJ)
      - may range from 0.2 to 1V





- FC
  - Fc : Forward-bias depletion capacitance coefficient
  - **Default FC=0.5**
  - A factor between 0 and 0.95 (limit by 0.95 in Qspice), which determines how the junction capacitance is calculated when the junction is forward-biased

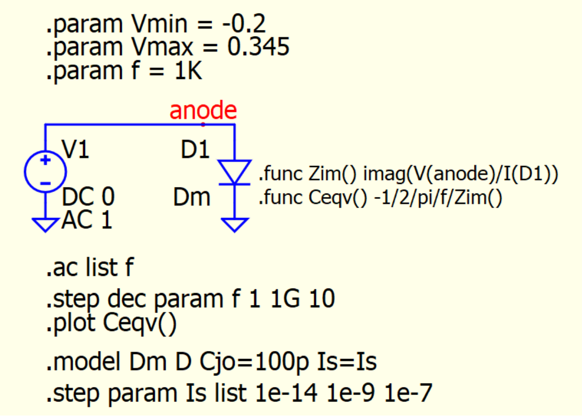


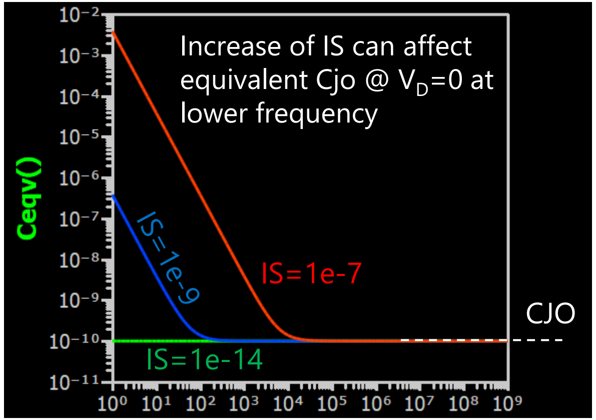


D. Diode Model (Capacitance) : Parameters can affect Cj in frequency

Qspice : Dmodel - Cj Effect – IS.qsch

- Params can affect Cj in frequency
  - IS : Saturation current

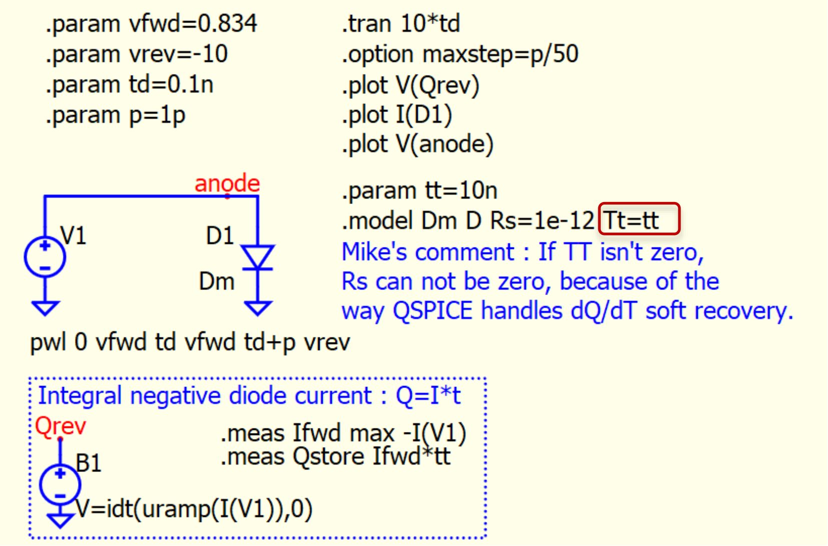


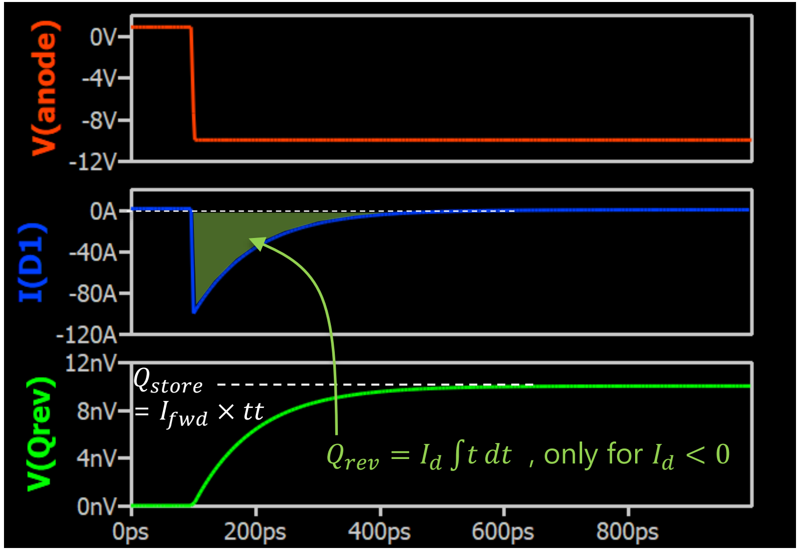


D. Diode Model (Reverse Recovery) : TT

Qspice : Dmodel - TT.qsch

- TT : Transit-time
  - TT is not the time it takes a diode to turn off. It's a measure of the amount of charge that needs to be pulled out to turn the diode off. Specifically, the stored charge is TT times the forward current. For the product to be Coulomb, the dimensions of TT must be time
  - $Q_{store} = I_{fwd} \times tt$, where tt is transit-time in Qspice
  - **Default TT=0s** [equivalent to disable reverse recovery from TT]
    - ** If TT is used, Rs must be non-zero (it can affect forward I-V characteristic if Rs=0 with a finite TT

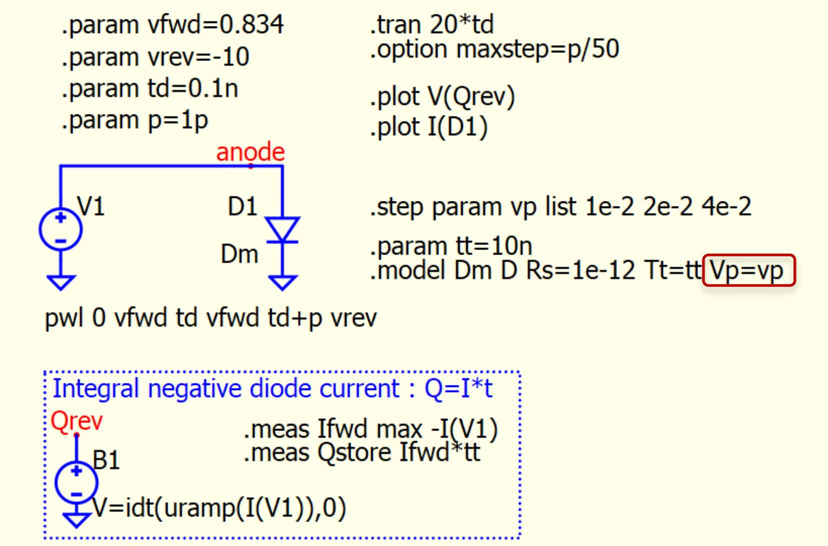


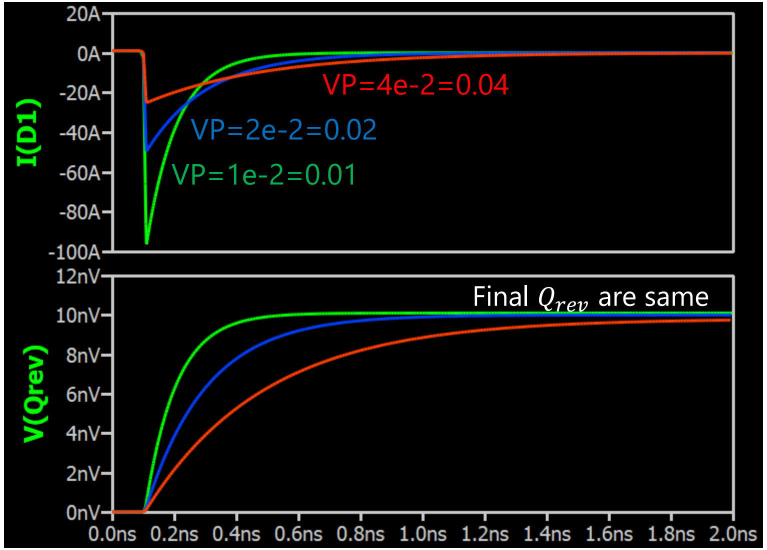


D. Diode Model (Reverse Recovery) : VP

Qspice : Dmodel - VP.qsch

- VP : Soft reverse recovery parameter
  - No description in Qspice HELP
  - **Default VP=1e-2 (i.e. Default VP=0.01)**
  - It affect current amplitude at reverse recovery
    - Increase VP can reduce current amplitude but increase reverse recovery time

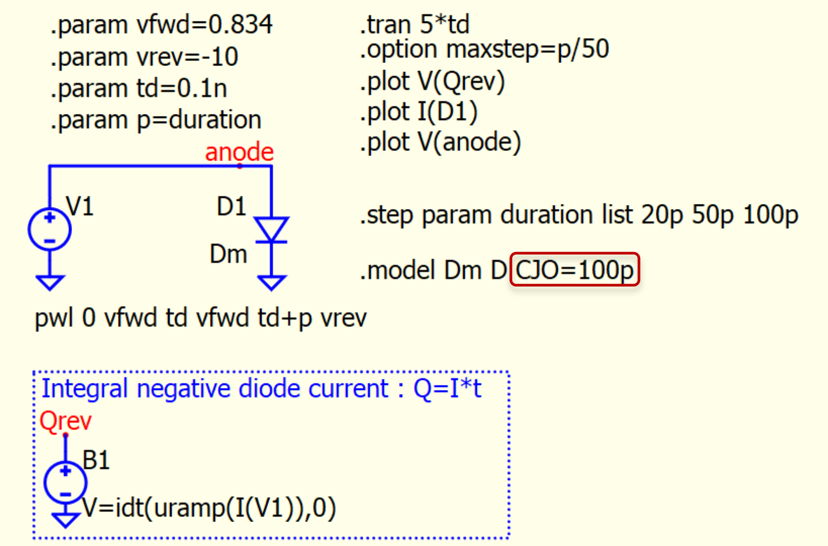


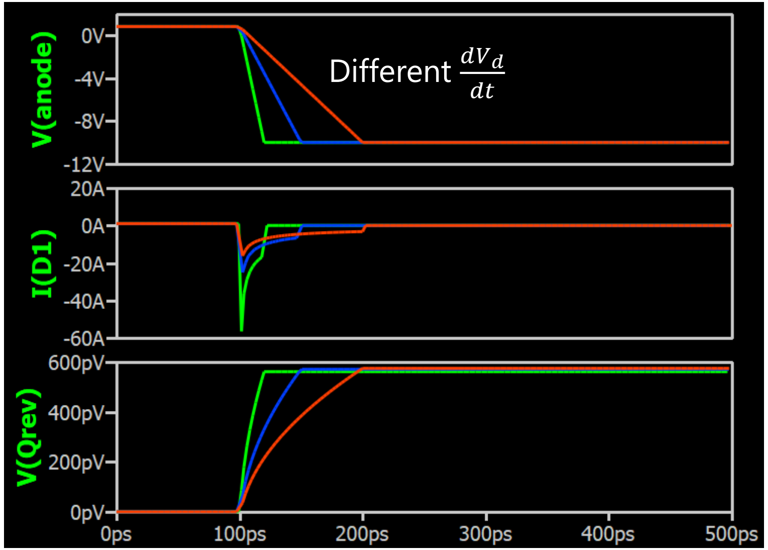


D. Diode Model (Reverse Current) : CJ

Qspice : Dmodel - CJO (RR).qsch

- CJ : Junction capacitance
  - Junction capacitance leads to reverse current but ***NOT*** a reverse recovery
    - For example, SiC has negligible reverse recovery and it model may not have TT but with CJO
  - Reverse charge depends on junction capacitance and reverse voltage
  - $\frac{dV_d}{dt}$ or $\frac{dI_d}{dt}$ are factor can affect peak reverse current in reverse recovery

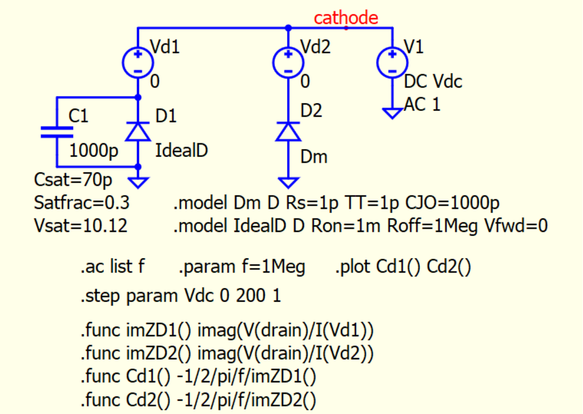


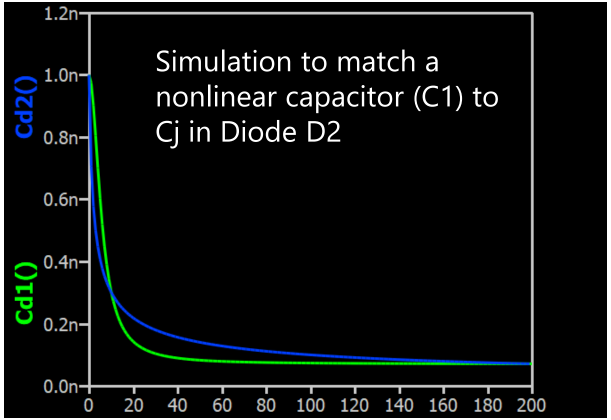


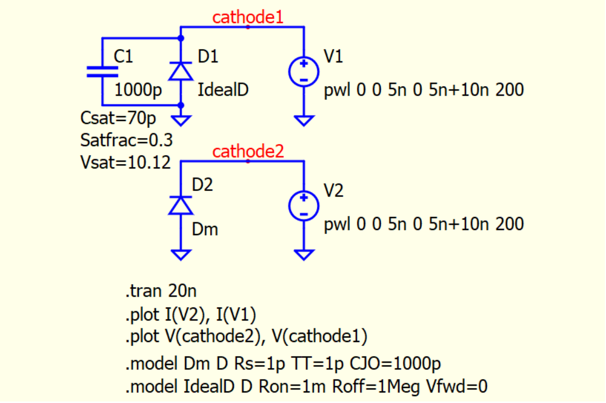
D. Diode Model (Reverse Current) : CJ

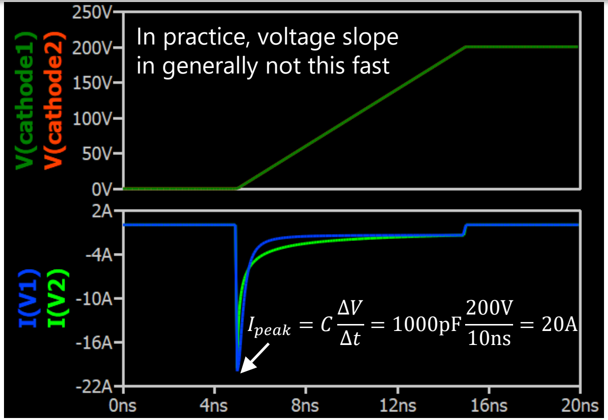
Qspice : Dmodel - CJ in Reverse Voltage.qsch / Dmodel - CJ in Reverse Current.qsch

- Cj Explanation
  - Junction capacitance is in parallel to diode and its capacitance is a function of diode reverse voltage
  - Simulation #1
    - Cj is nonlinear to diode reverse voltage, to model Cj, it requires use non-linear capacitor with Csat, Satfrac and Vsat
  - Simulation #2
    - Apply reverse voltage can simulate capacitor charging current, which act like reverse recovery but actually is not
    - Reverse recovery rely on forward current as reverse recovery is to remove this charge to turn off the diode
    - However, Cj is simply a mechanism that current charging a nonlinear capacitor





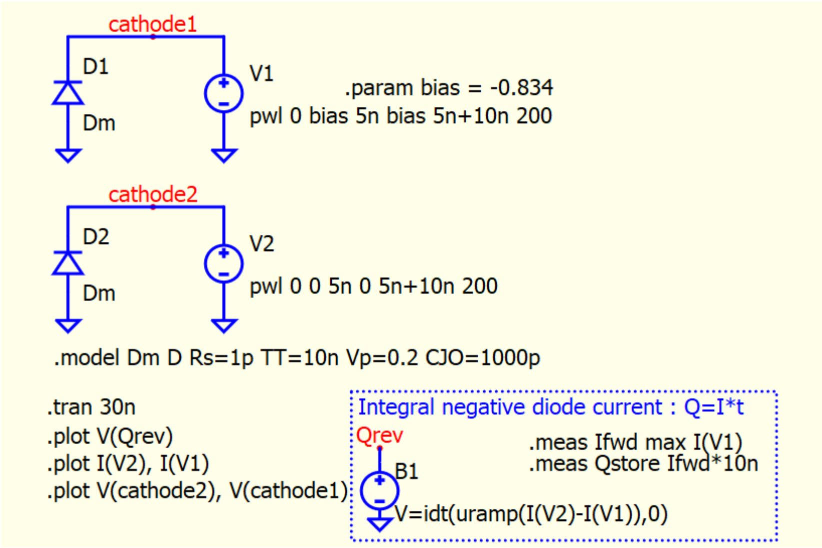


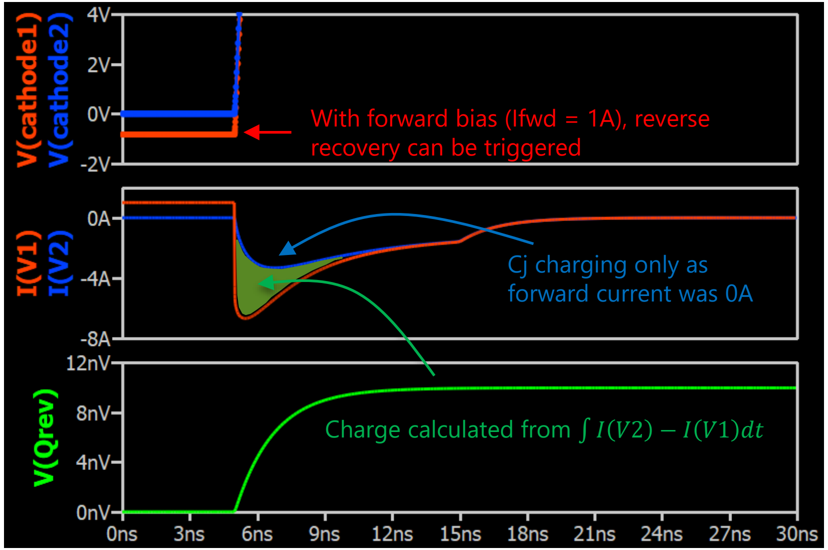


Explanation of Reverse Recovery and Junction Capacitance Charging

Qspice : Dmodel - Reverse Recovery and Capacitor Charging.qsch

- Explanation of Reverse Recovery and Junction Capacitance Charging Current
  - Reverse Recovery is only preset if forward current is applied
  - If forward current is 0A, reverse current is by charging junction capacitance (Cj), and this is a nonlinear capacitance (capacitance decrease with cathode voltage) and therefore, reverse current reduce over time even ramp of cathode voltage is constant, where $I_d = C_j \frac{dV_d}{dt}$, where C_j is a function of V_d
  - If forward current is preset, reverse recovery is applied (TT and Vp). A extra potion of reverse current is generated and this extra charge equal $I_{fwd} \times TT$





PSPICE Static Model Params (Recombination) : IKF, ISR and NR

** Modeling of Recombination Current

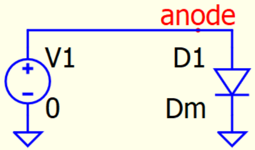
- Semiconductor Device Modeling with SPICE (Section 1.9.1)
  - $I_D = \left(K_{hli} I_F + K_{gen} I_R\right) - I_{Breakdown}$
    - $I_F = I_S\left(e^{\frac{qV_D}{nkT}} - 1\right)$
      - I_S is IS : Saturation current (default = 1e-14A)
      - n is N : Emission coefficient (default = 1)
    - $K_{hli} = \sqrt{\frac{I_{KF}}{I_{KF}+I_F}}$ for $I_{KF} > 0$: If $I_{KF} \rightarrow \infty$, $K_{hli} = 1$
      - I_{KF} is IKF : High injection knee current (default = 1e308)
    - $I_R = I_{SR}\left(e^{\frac{qV_D}{n_R kT}} - 1\right)$
      - I_{SR} is ISR : Recombination current parameter (default = 0A)
      - n_R is NR : ISR emission coefficient (default = 2)
    - $K_{gen} = \sqrt{\left[\left(1 - \frac{V_D}{\Phi_0}\right)^2 + 0.005\right]^m}$
      - m is M : Grading coefficient (default = 0.5)
      - Φ_0 is VJ : Junction potential (default = 1V)
    - $I_{Breakdown} = IBV\ e^{-\frac{q(BV+V_D)}{kT}}$
      - IBV is IBV : Current at breakdown voltage (default = 1e-10A)
      - BV is BV : Reverse breakdown voltage (default = Infinite V)
      - This is equation to describe breakdown region. Reverse leakage is described in $\left(K_{hli} I_F + K_{gen} I_R\right)$

D. Diode Model (Recombination) : IKF

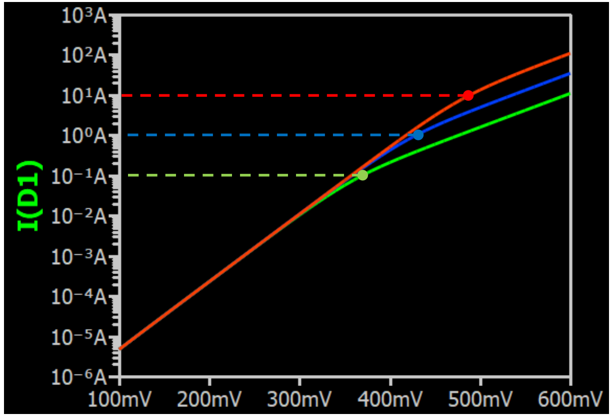
Dmodel - IKF.qsch

- IKF
  - IKF : High injection knee current
  - **Default IKF=1e308**
  - $I_D = \left(K_{hli} I_F + K_{gen} I_R\right)$
  - $I_D = K_{hli} I_F$
    - $K_{hli} = \sqrt{\frac{I_{KF}}{I_{KF}+I_F}}$ for $I_{KF} > 0$
  - The modification effect may only be easily observed with ID in log scale

```
.param Vmin = 0.1
.param Vmax = 0.6
```



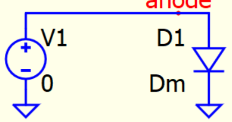

```
.dc V1 {Vmin} {Vmax} 0.01
.plot I(D1)

.step param ikf list 0.1 1 10
.model Dm D Is=100n N=1 IKF={ikf}
```



D. Diode Model (Recombination) : ISR
Qspice : Dmodel - ISR.qsch

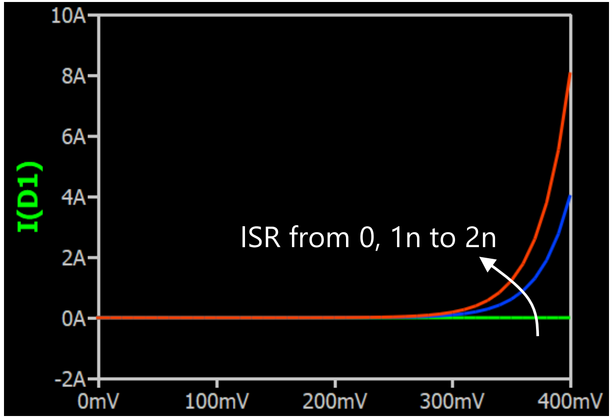
- ISR
  - Isr : Recombination current parameter
  - **Default ISR=0A**
  - $I_D = (K_{hli} I_F + K_{gen} I_R)$
  - In following examples, I_F is forced to be negligible as compare to $K_{gen} I_R$ in calculating I_D
  - $I_D = K_{gen}\, I_{SR} \left(e^{\frac{qV_D}{n_R kT}} - 1\right)$
    - $K_{gen} = \sqrt{\left[\left(1 - \frac{V_D}{\Phi_0}\right)^2 + 0.005\right]^m}$
    - n_R is NR : default = 2V
    - m is M : default = 0.5
    - Φ_0 is VJ : default = 1V

.param Vmin = -5
.param Vmax = 0.4



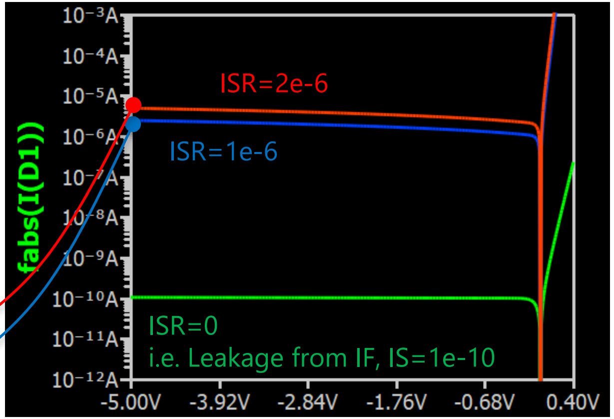
.dc V1 Vmin Vmax 0.01
.plot I(D1)

.step param isr list 0 1e-6 2e-6
.model Dm D Is=1e-10 N=2 $\boxed{\text{ISR=isr}}$ NR=1
Is and N are set to equivalent with negligible If as compare to Ir to demonstrate Ir effect



- Remark
  - As IS is set to 1e-12, in reverse and ISR=0, leakage current can still be observed through equation I_F
  - $@V_D = -5V$

    $K_{gen} = \sqrt{\left[\left(1 - \frac{-5}{1}\right)^2 + 0.005\right]^{0.5}}$ =2.4495
  - Therefore
  - ID for ISR=2e-6, VD=-5 is 4.8990uA
  - ID for ISR=1e-6, VD=-5 is 2.4495uA

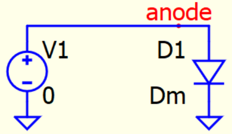


D. Diode Model (Recombination) : NR and M

Qspice : Dmodel - NR.qsch / Dmodel - M (Recombination).qsch

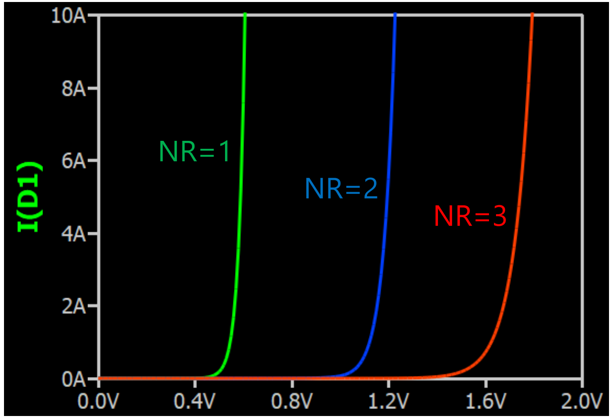
- NR
  - Nr : ISR emission coefficient
  - **Default NR=2**
  - $I_D = K_{gen}\, I_{SR} \left(e^{\frac{qV_D}{n_R kT}} - 1 \right)$

```
.param Vmin = 0
.param Vmax = 2
```



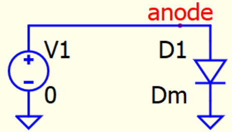

```
.dc V1 Vmin Vmax 0.01
.plot I(D1)

.step param nr list 1 2 3
.model Dm D Is=1e-12 N=5 ISR=1e-9 NR=nr
```

Is and N are set to equivalent with negligible If as compare to Ir to demonstrate Ir effect



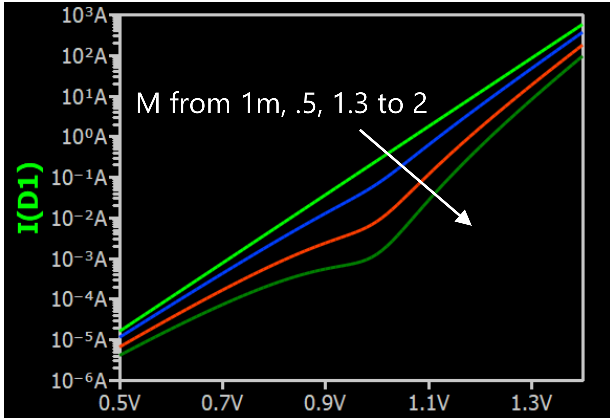
- M
  - M : Grading coefficient
  - **Default M=0.5**
  - $K_{gen} = \sqrt{\left[\left(1 - \frac{V_D}{\Phi_0}\right)^2 + 0.005 \right]^m}$
  - The modification effect may only be easily observed with ID in log scale

```
.param Vmin = 0.5
.param Vmax = 1.4
```




```
.dc V1 Vmin Vmax 0.01
.plot I(D1)

.step param m list 1m 0.5 1.3 2
.model Dm D Is=1e-12 N=5 ISR=1e-9 NR=2 M=m
```

Is and N are set to equivalent with negligible If as compare to Ir to demonstrate Ir effect



D. Diode

Behavioral Diode Model Parameters

Behavioral Diode Model Parameters in Qspice HELP

QSPICE includes a simplified, behavioral, diode. To use those device equations, specify a non-zero RON.

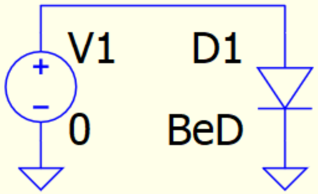
Behavioral Diode Model Parameters

Name	Description	Units	Default
RON	Forward on resistance	Ω	0.0[3]
ROFF	Off resistance	Ω	1./GMIN
RZEN	Breakdown resistance(aka RREV)	Ω	RON
VFWD	Forward voltage drop	V	0.0
VREV	Reverse voltage drop	V	0.0
EPSILON	Width of quadratic region splining off and on regions	V	0.0
REVEPSILON	Width of quadratic region splining breakdown and on regions	V	0.0
CJO	Shunt capacitance	F	0.0

3] The value of zero means don't use these equations, but the conventional SPICE semiconductor diode equations.

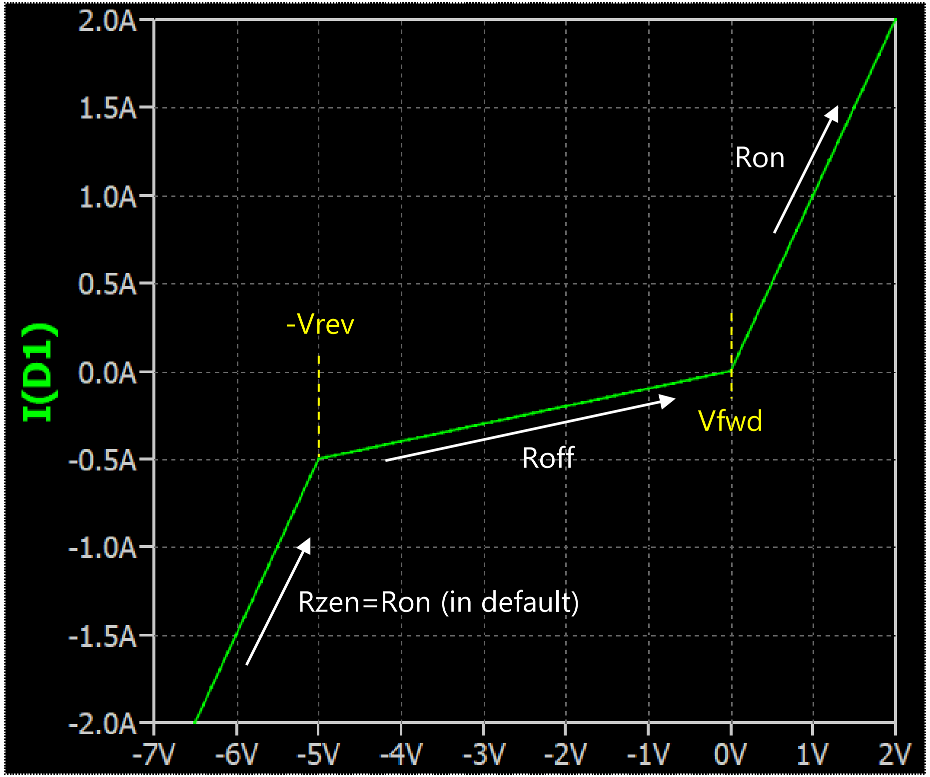
Behavioral Diode Model Params : Ron, Roff, Vfwd, Vrev

Qspice : Behavioral D Model - Ron Roff Vfwd Vrev.qsch



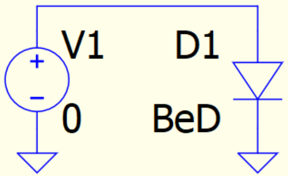
.model BeD D Ron=1 Roff=10 Vfwd=0 Vrev=5
+ Epsilon=0 Revepsilon=0

.dc V1 -7 2 0.1
.plot I(D1)



Behavioral Diode Model Params : Rzen, Epsilon, Revepsilon

Qspice : Behavioral D Model - Epsilon Revepsilon Rzen.qsch

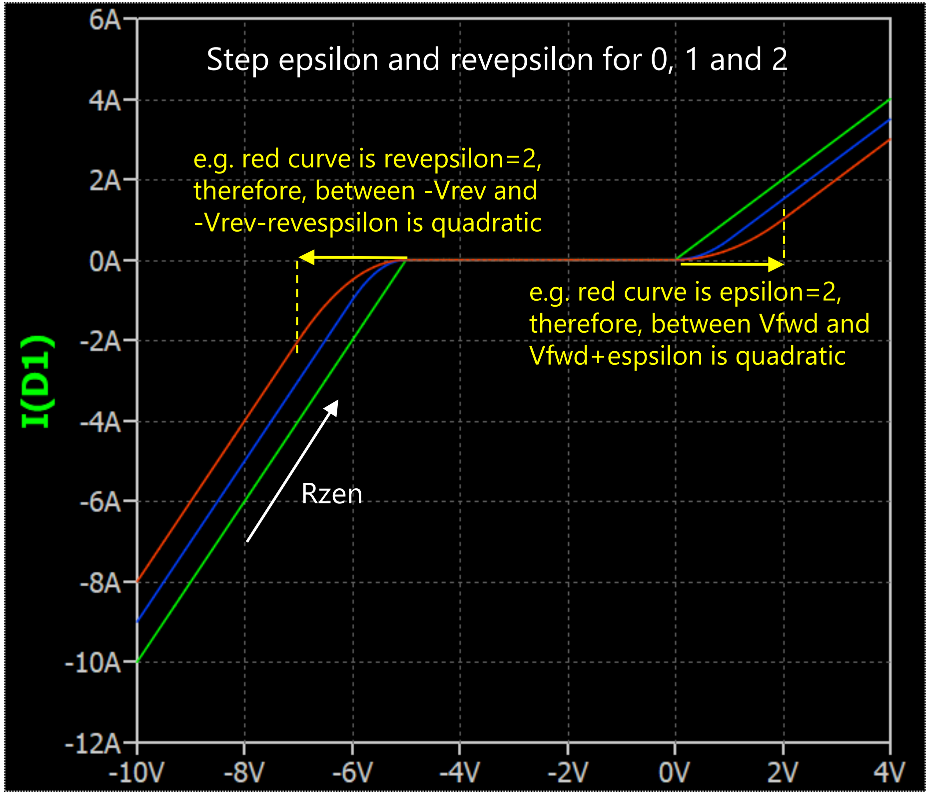


.model BeD D Ron=1 Roff=10Meg Vfwd=0 Vrev=5
+ Epsilon={val} Revepsilon={val} Rzen=0.5

.dc V1 -10 4 0.1
.plot I(D1)

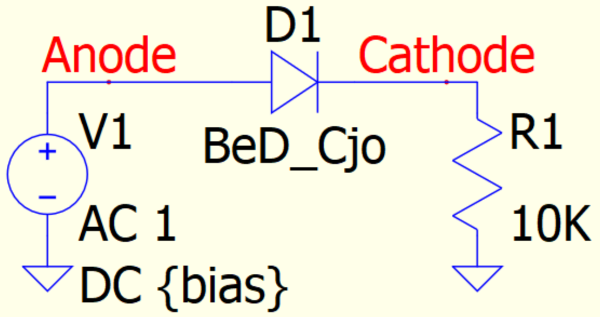
.param val=0
.step param val 0 2 1

* Roff change to 10Meg in this study



Behavioral Diode Model Params : Cjo

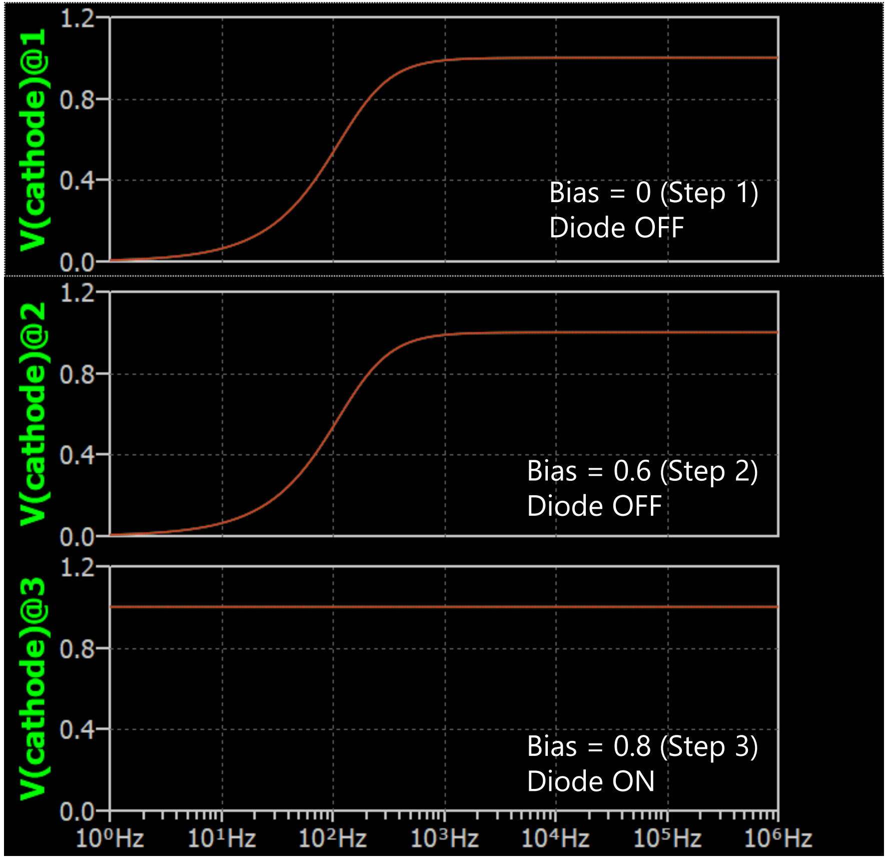
Qspice : Behavioral D Model - Cjo.qsch



.param bias = 0
.model BeD_Cjo D Ron=1m Roff=1Meg
+ Vfwd=0.7 Cjo=100n

Cjo is equivalent to a capacitor parallel the behavioral diode

.ac dec 100 1 1Meg
.step param bias list 0 0.6 0.8



D. Diode
Ideal Diode .model

Ideal Diode Model

Qspice : Special - IdealD (.dc).qsch / Special - IdealD (.tran).qsch

- Ideal Diode Characteristic
  - No breakdown current
  - No reverse leakage
  - No capacitance effect
  - No reverse recovery

- Ideal Model with Diode .model
  - .model Idlm D N=0.01 RS=10µ ; Vf@1A=0
  - .model Idlm D N=0.36 RS=10µ ; Vf@1A=0.3
  - .model Idlm D N=0.85 RS=10µ ; Vf@1A=0.7
  - ** RS is added to prevent gmin stepping without series resistance

- Ideal Model with Behavioral Diode .model
  - .model IdealD D Vfwd=0 Ron=1m Roff=100Meg ; Vf,th=0
  - .model IdealD D Vfwd=0.3 Ron=1m Roff=100Meg ; Vf,th=0.3
  - .model IdealD D Vfwd=0.7 Ron=1m Roff=100Meg ; Vf,th=0.7

Diode Type

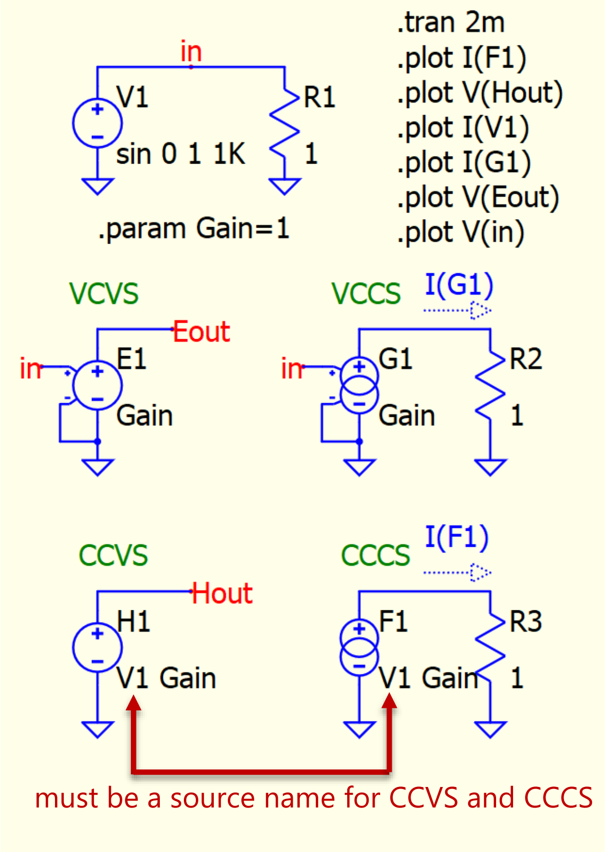
- Germanium
  - Bandgap : 0.67eV
- Silicon
  - Bandgap : 1.1eV
- Ultra-fast Recovery
- Silicon-Schottky
  - Bandgap : 0.69eV
- SiC-Schottky
  - Bandgap : 3.2eV
- GaN
  - Bandgap : 3.4eV
- Zener

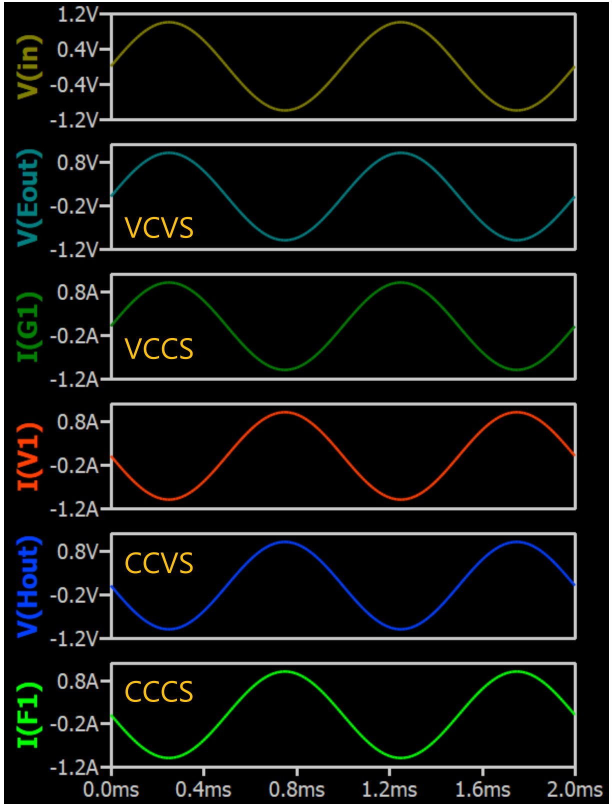
E. F. G. H.
Dependent Sources

E. F. G. H. Dependent Sources

Qspice : Dependent Source - Basic.qsch

- Dependent Sources
  - [E] VCVS : Voltage Dependent Voltage Source
  - [G] VCCS : Voltage Dependent Current Source
  - [H] CCVS : Current Dependent Voltage Source
  - [F] CCCS : Current Dependent Current Source





I. Current Source

I. Current Source : Instance Parameters

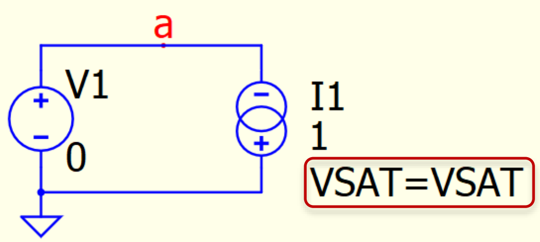
Current Source Instance Parameters

Name	Description	Units	Default
AC	AC magnitude, optionally followed by phase angle	A, °	0.
ACMAG	AC magnitude	A	0.
ACPHASE	AC phase	°	0.
DC	DC value of source	A	0.
EXP	Exponential source description		
LOG	Interpolate between PWL and CHIRP points		(not set)
PULSE	Pulse description		
PWL	Piecewise linear description		
SFFM	Single frequency FM description		
SINE	Sinusoidal source description(aka SIN)		
TIMECTRL	Time step control, one of NONE, LIMITS[1], BREAKS[2], or BOTH	String	LIMITS
VSAT[3]	Don't source power(example)	V	0.
VSAT2	Don't source power and don't conduct in reverse	V	0.
XTRAP	Extrapolate beyond PWL and CHIRP points		(not set)

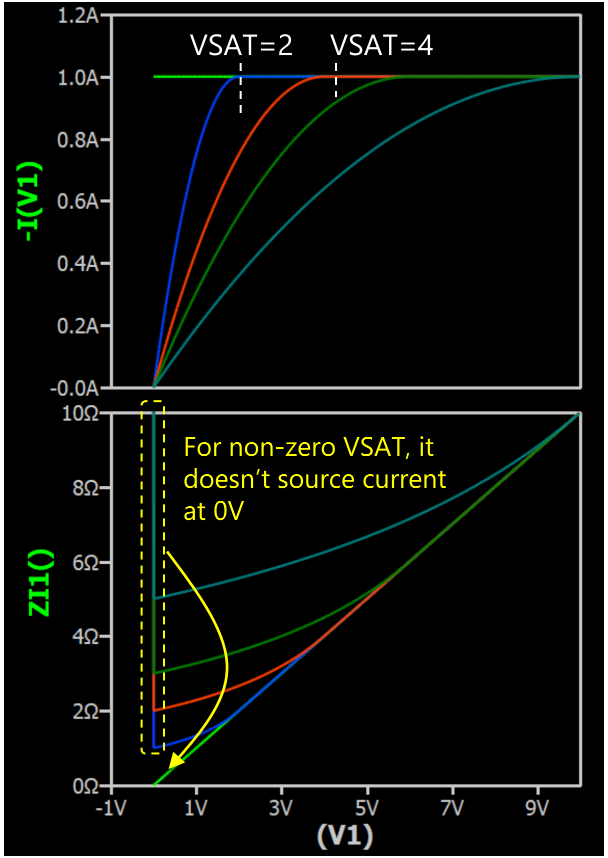
I. Instance Params : VSAT

Qspice : I Source - VSAT.qsch

- VSAT
  - VSAT : Don't source power
  - Characteristic
    - Only source current when V(-ve,+ve) > VSAT
    - Current source doen't source current at V(-ve,+ve)=0
      - Equivalent to Open
    - Not to apply negative voltage between V(-ve,+ve) as it will have current flow out from -ve
  - Usage
    - Useful for modeling an active load or a bias current in a macromodel



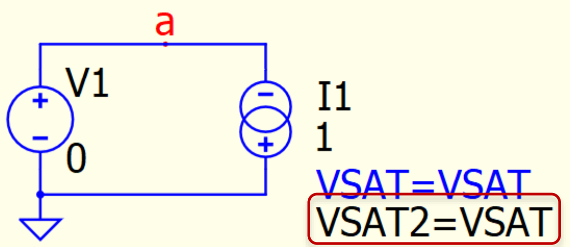

```
.dc V1 0 10 0.1
.step param VSAT list 0 2 4 6 10
.func ZI1() V(a)/-I(V1)
.plot ZI1()
.plot -I(V1)
```



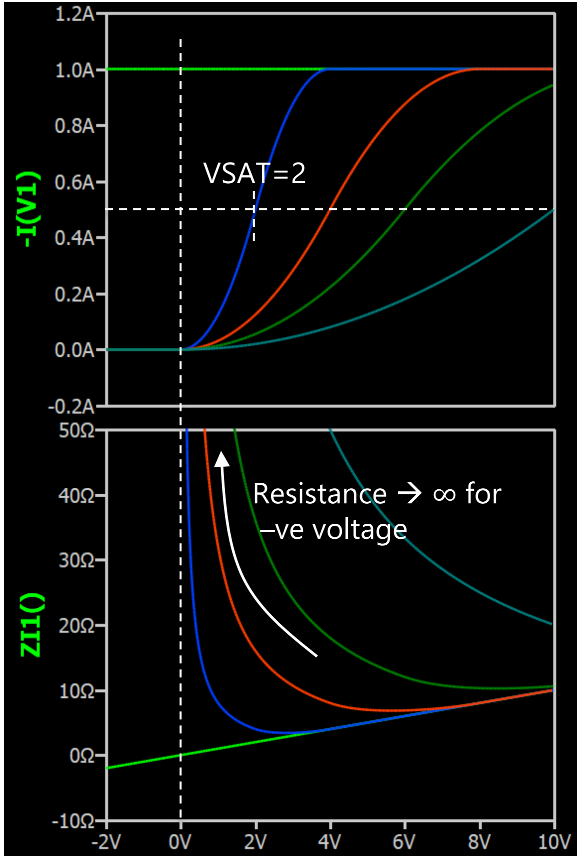
I. Instance Params : VSAT2

Qspice : I Source - VSAT2.qsch

- VSAT2
  - VSAT2 : Don't source power and don't conduct in reverse
  - If VSAT2 is used, VSAT will be override



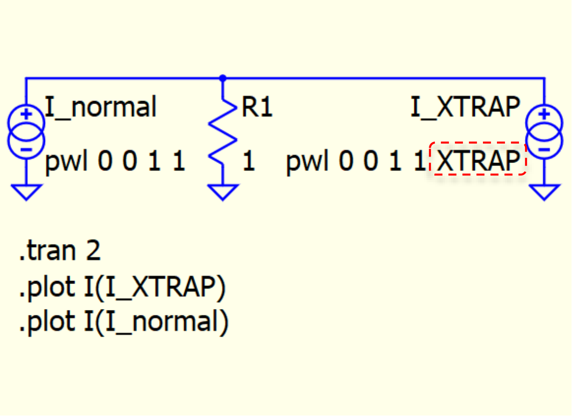

```
.dc V1 -2 10 0.01
.step param VSAT list 0 2 4 6 10
.func ZI1() V(a)/-I(V1)
.plot ZI1()
.plot -I(V1)
```

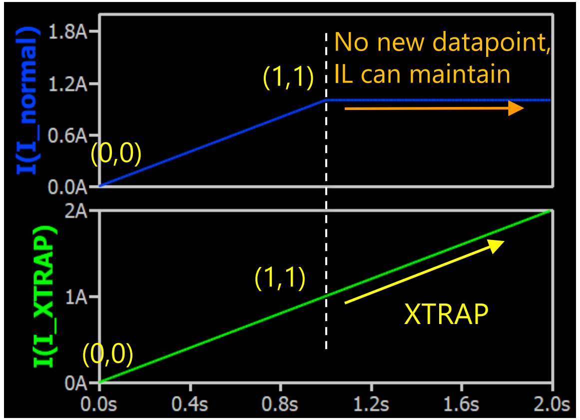


I. Instance Params : XTRAP

Qspice : I Source - XTRAP.qsch

- XTRAP
  - Extrapolate beyond PWL and CHIRP points
  - Without XTRAP, for times after the last time, the current is the last current.

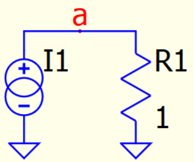




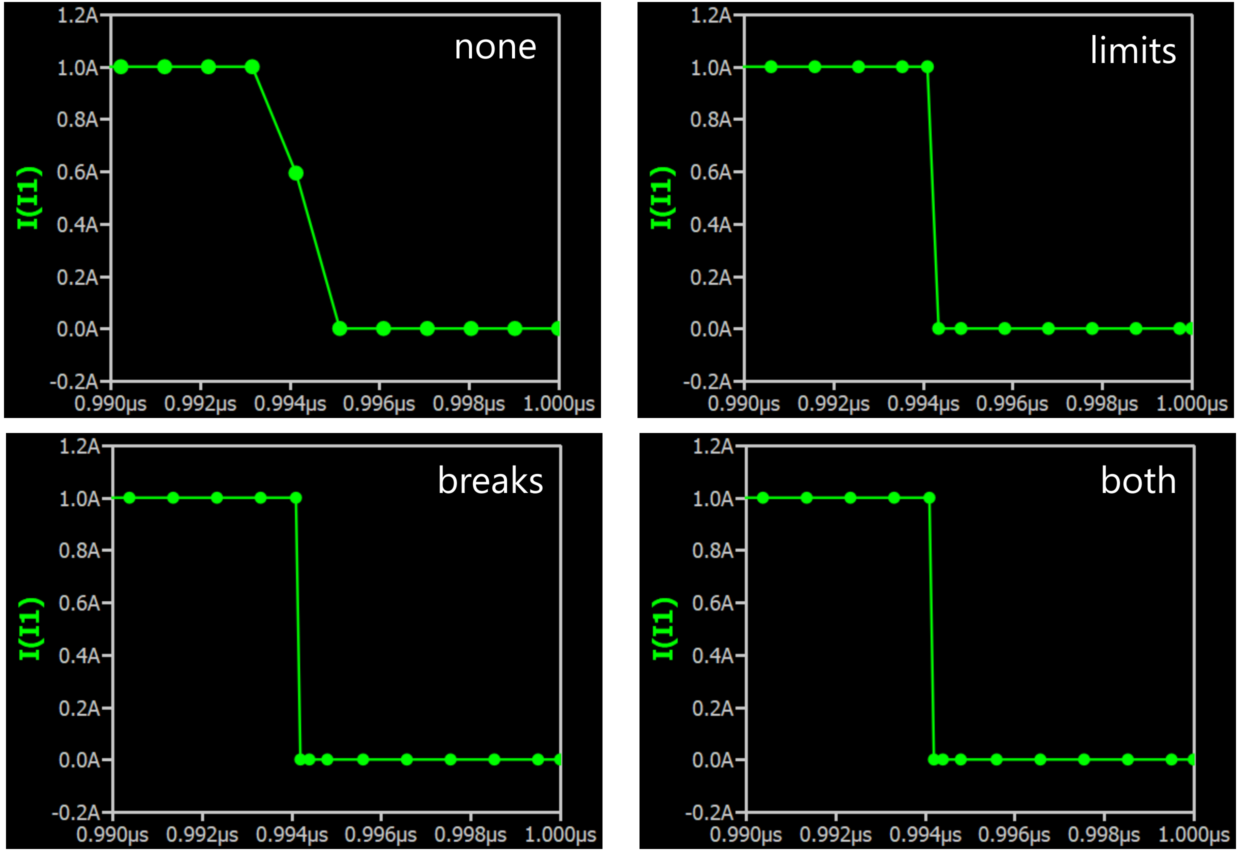
I. Instance Params : Timectrl

Qspice : I Source - TIMECTRL.qsch

- TIMECTRL
  - Timectrl : Time step control
    - None
    - Limits
    - Breaks
    - Both
  - **Default Timectrl=Limits**



pulse 0 1 4n 0 0 10n 20n
Timectrl=none
Timectrl=limits
Timectrl=breaks
Timectrl=both
.tran 1000n
.plot I(I1) I(I2)



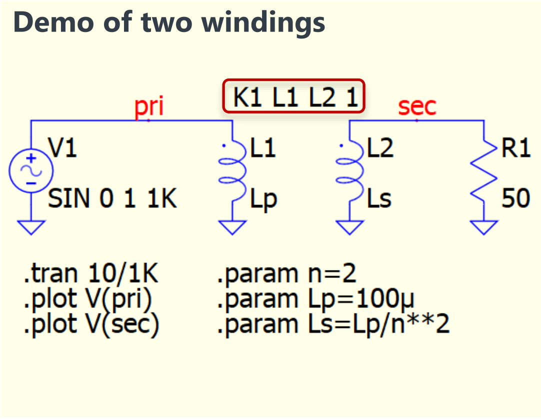
J. JFET Transistor

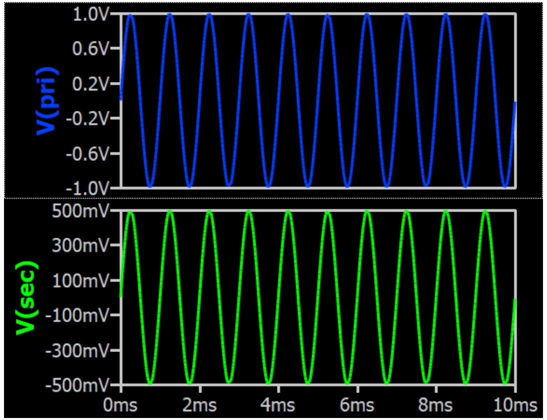
K. Mutual Inductance

K. Mutual Inductance

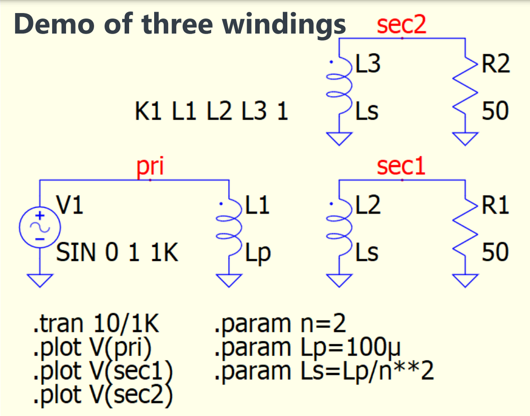
Qspice : K Mutual - Two Winding.qsch / K Mutual - Three Winding.qsch

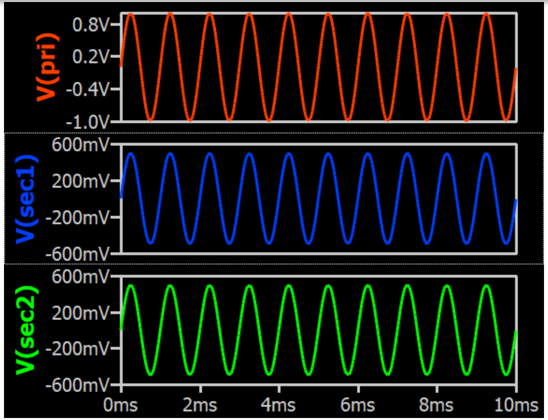
- K Mutual Inductance
  - K is coupling coefficient of coupled inductors
    - Ideal coupling : 1
    - Range : -1 to 1
  - Two or more coupled inductors are required
    - Press L two times to get symbol with a dot notation (not necessary, but recommend for current direction)





- Inductors as Transformer
  - $\frac{L_p}{N_p^2} = \frac{L_s}{N_s^2}$ and $n = \frac{N_p}{N_s}$
    - N is number of turns
  - $L_p = n^2 L_s$ or $L_s = \frac{1}{n^2} L_p$
  - In practice, Lp is measured from primary with secondary open





L. Inductor

Inductor L Instance Parameters in Qspice HELP

Inductor Instance Parameters

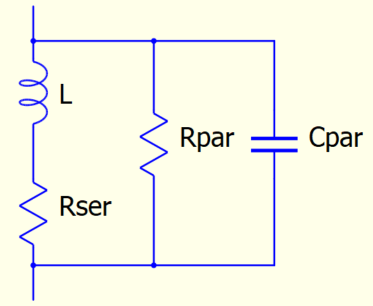
Name	Description	Units	Default
AG	Wire or stripline is made of gold		
AL	Wire or stripline is made of aluminum		see below
AU	Wire or stripline is made of silver		
BEND	Fractional inductance correction for wire bend or proximity effects		1.
CPAR	Parallel capacitance	F	0.
CU	Wire or stripline is made of copper		see below
DIAMETER	Diameter of wire or air coil	m	
FREQUENCY	Frequency at Q. Also used to compute Rser due to skin effect		
HEIGHT	Height of PCB stripline above ground plane	m	
IC	Initial current if uic is specified on .tran statement	A	none
INDUCTANCE	Inductance of inductor	H	0.0
ISAT	Current causing inductance to drop to SATFRAC×INDUCTANCE	A	Infinite
LENGTH	Length of wire, stripline, or air coil	m	
LSAT	Inductance asymptotically approached in saturation	H	10% of INDUCTANCE
M	Number of parallel inductors		1.0
NI	Wire is made of nickel		
Q	Quality factor at FREQUENCY		
RPAR	Equivalent parallel resistance	Ω	Infinite
RSER	Equivalent series resistance	Ω	0.0
SATFRAC	Fractional drop in inductance at ISAT		0.7
THICK	Thickness of stripline on top of a PCB	m	0.0
TURNS	Number of turns of an air coil		
VERBOSE	Print wire L, Rser, Rpar results on the console		(not set)
WIDTH	Width of stripline on top of a PCB	m	

Arbitrary Inductance Device

QSPICE also supports an arbitrary inductance device. To use it, give an equation for the flux due to the inductor. The equation can include any circuit node voltages or device currents of devices modeled as Thévenin equivalents(V-, L-, E-, or H- devices). In the interest of completeness, the device supports transinductance.

Syntax: Cnnn N1 N2 Q=<expression> [additional instance parameters]

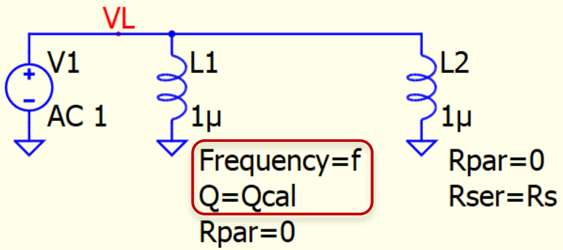
Name	Description	Units	Default
FLUX	Equation of flux(aka F)	Weber	
IC	Initial flux due to the inductor	Weber	
M	Number of identical parallel devices		1.0
RPAR	Equivalent parallel resistance	Ω	Infinite
RSER	Equivalent series resistance	Ω	0.0
NOISELESS	Ignore the noise contribution from RPAR and RSER		not set
TEMP	Instance temperature	°C	Circuit temperature



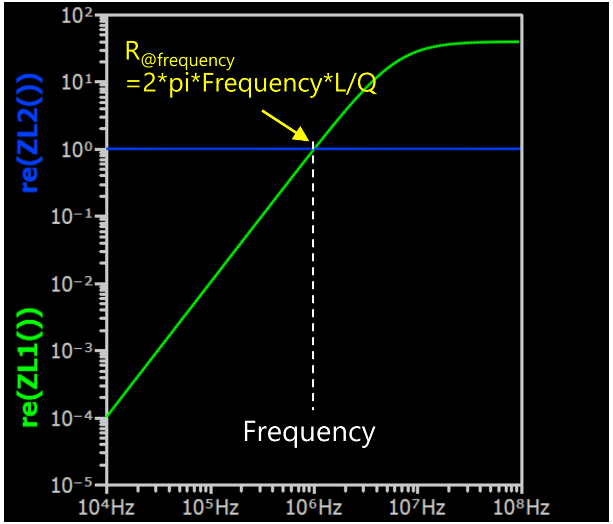
L. Instance Params : Frequency and Q
Qspice : Inductor - Frequency Q.qsch

- Frequency and Q
  - Frequency : Frequency at Q
    - Also used to compute Rser due to skin effect
  - Q : Quality factor at FREQUENCY

- Formula
  - $Q = \frac{X_L}{R} = \frac{2\pi f L}{R_{@f}}$
  - Using Frequency and Q is not same as using Rser modeling
    - Rser is a constant over frequency but Frequency/Q pair give Rser with skin effect



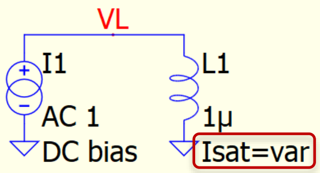
User Parameters and Q calculation
```
.param f=1Meg
.param Rs=1
.param Qcal = 2*pi*f*1µ/Rs
```
AC Sweep and Impedance calculation
```
.ac dec 100 10K 100Meg
.func ZL1() V(VL)/I(L1)
.func ZL2() V(VL)/I(L2)
```
Plot Real Part of Impedance
```
.plot re(ZL1()) re(ZL2())
```



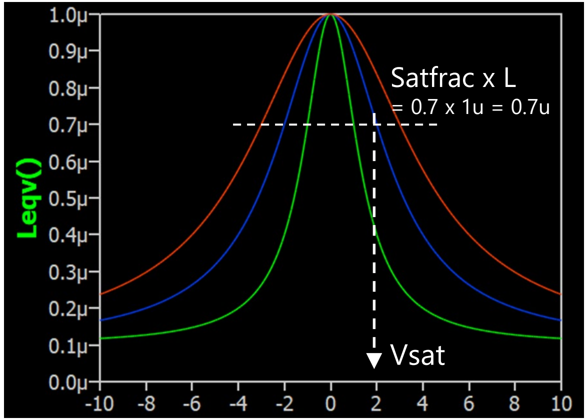
L. Instance Params : Isat, Lsat, Satfrac : For Nonlinear Inductance

Qspice : L Inductor - Isat (.ac).qsch

- Isat and Satfrac
  - **Isat** : Current that drops inductance to ***Satfrac x Inductance***
  - **Satfrac** : Fractional drop in inductance at Isat
    - default = 0.7
  - Nonlinear effect is valid in +ve and –ve current direction




```
.param frq=1Meg
.step param bias -10 10 0.1    Sweep bias
.step param var list 1 2 3     Sweep Isat

.ac list frq
.func Leqv() V(VL)/1/2/pi/frq
.plot Leqv()
```



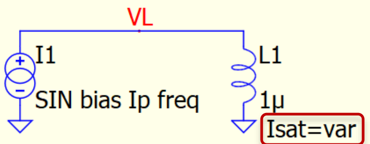
Bias Current from -10V to 10V

- Inductance equation
  - $X_L = \omega L = \frac{V_L}{I_L}$
  - $L = \frac{|V_L|}{|I_L|}\frac{1}{\omega} = \frac{|V_L|}{2\pi f\,|I_L|}$
  - This formula is used to calculate equivalent inductance (small signal model) at different inductor bias current

L. Instance Params : Isat, Lsat, Satfrac : For Nonlinear Inductance

Qspice : L Inductor - Isat (.tran).qsch / L Inductor - Lsat (.tran).qsch

- Isat and Satfrac
  - **Isat** : Current that drops inductance to ***Satfrac x Inductance***
  - **Satfrac** : Fractional drop in inductance at Isat
    - default = 0.7



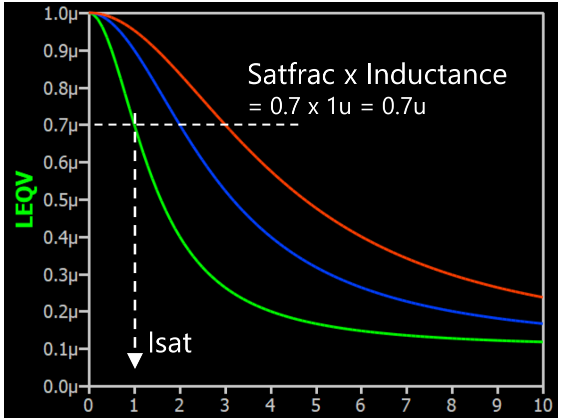

```
.param Ip = 0.1
.param freq=1K
.step param bias 1p 10 0.1
.step param var list 1 2 3
.tran 0 10/freq 9/freq
```

Ip needs small for small signal in transient anslysis

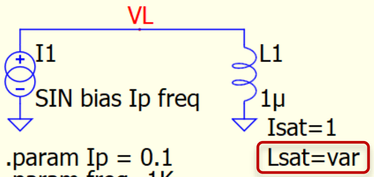
Sweep bias
Sweep Vsat

Calculate equivalent capacitance in .tran analysis

```
.meas Vp max V(VL)
.meas Leqv Vp/Ip/2/pi/freq
.meas plot Leqv
```



- Lsat
  - **Lsat** : Inductance asymptotically approached in saturation
    - ** Isat must be set to see it effect

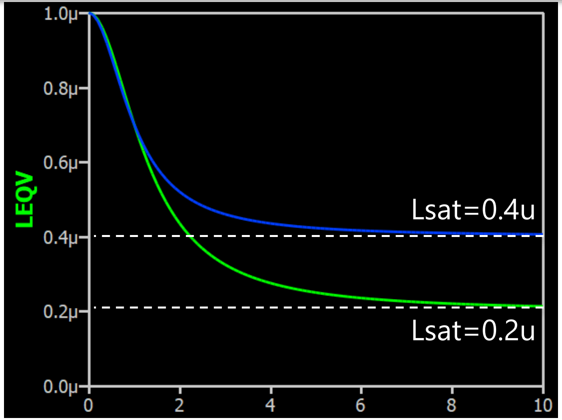



```
.param Ip = 0.1
.param freq=1K
.step param bias 1p 10 0.1
.step param var list 0.4μ 0.2μ
.tran 1/freq
```

Sweep bias
Sweep Lsat

Calculate equivalent capacitance in .tran analysis

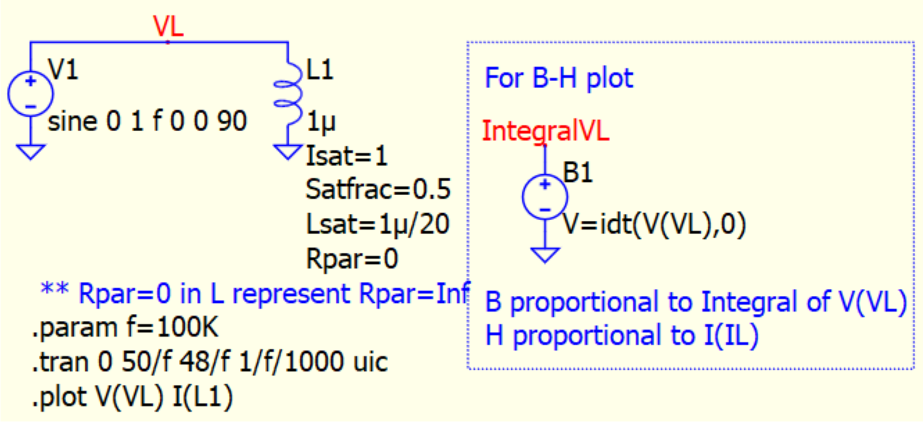
```
.meas Vp max V(VL)
.meas Leqv Vp/Ip/2/pi/freq
.meas plot Leqv
```

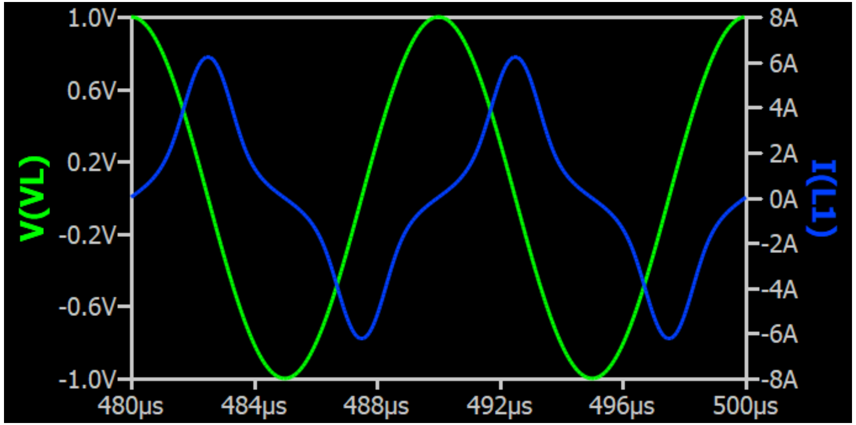


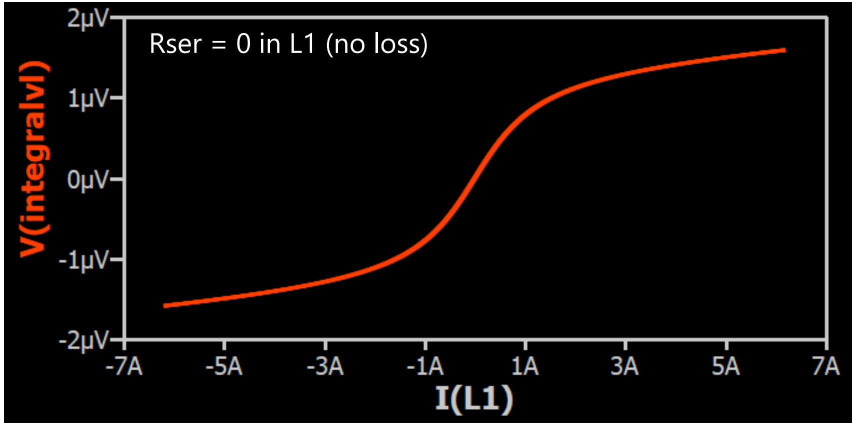
Demonstration of Nonlinear Inductor (model B-H saturation)

Qspice : L Inductor Nonlinear (Tran) - Current and BH.qsch

- Nonlinear Inductor in Qspice
  - This simulation demonstrate transient of non-linear inductor with a sinusoidal voltage source, which can expect a non-linear current
- Reference : B and H for inductor
  - Magnetic field intensity $H = \frac{B}{\mu} = \frac{N}{l_e} i_L$ (unit : A/m)
  - Magnetic field strength $B = \frac{\phi_B}{A_e} = \frac{1}{N\,A_e} \int v_L\, dt$ (unit : Tesla)
    - B also called magnetic flux density

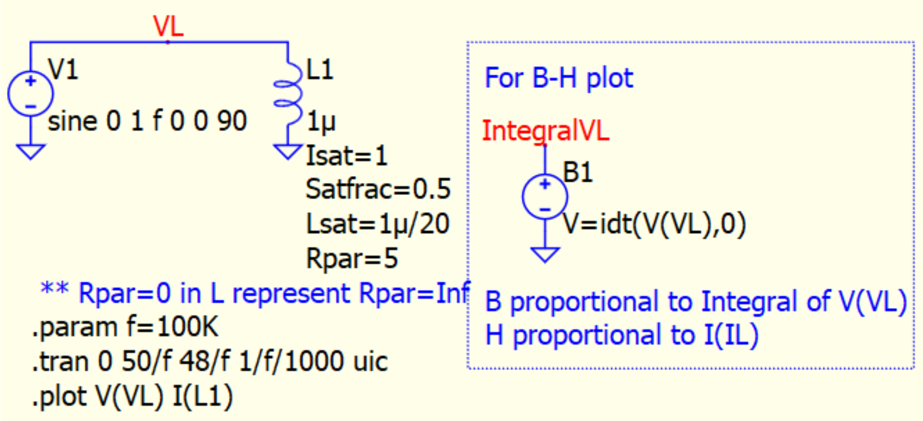


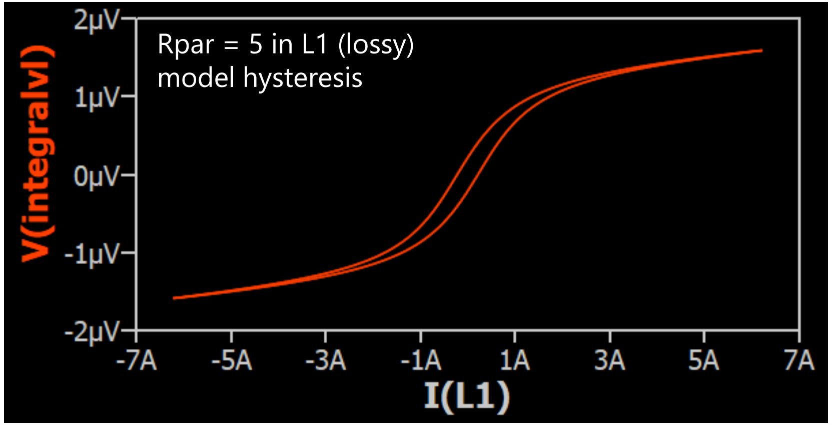




Demonstration of Nonlinear Inductor (model B-H hysteresis : lossy)

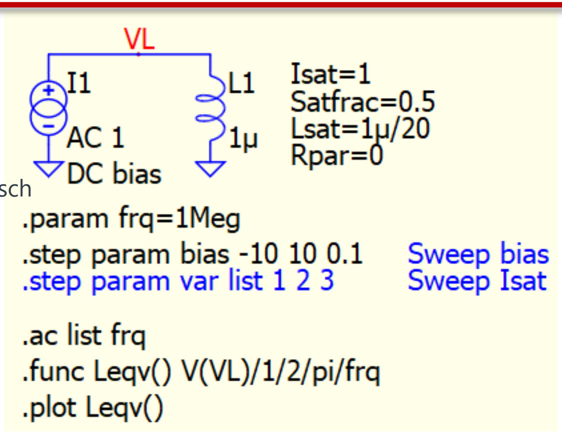
Qspice : L Inductor Nonlinear (Tran) - Current and BH.qsch

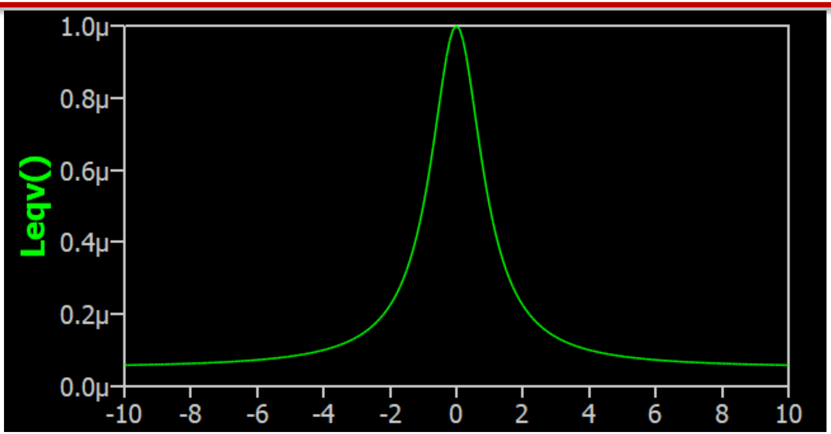




Plot equivalent L

L Inductor (AC) - Current and BH.qsch





Comment about Saturation and Hysteresis of B-H curve

Isat, Lsat and Satfrac are key parameters in Qspice for non-linear inductance modeling. General interest is just a saturating include. This represents inductor saturating when current reach certain level (i.e. inductance drop according to current, which can model by Isat, Lsat and Satfrac). This characteristic is saturation in B-H curve.

For hysteresis of B-H curve, it can generally model with a parallel resistor Rpar to represent loss.

May be some people prefer to model non-linear inductor with other way, but I found Qspice definition generally good enough as L vs bias current can be easily measure practically.

L. Arbitrary Inductance : Inductor modeling with FLUX

Qspice : Flux formula.qsch

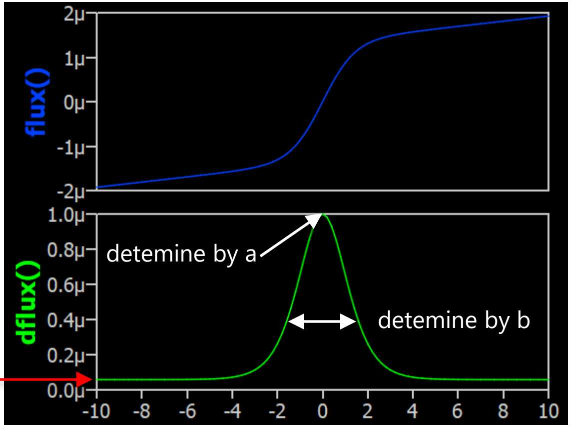
- Basic equation of Inductor
  - [equation 1] : Voltage v_L and Flux ϕ Relationship : $v_L = \frac{d\phi}{dt}$
  - [equation 2] : Voltage v_L and Current i_L Relationship : $v_L = L\frac{di_L}{dt}$
  - Therefore, by $\frac{d\phi}{dt} = L\frac{di_L}{dt}$, Inductor $L = \frac{d\phi}{di_L}$

- Qspice inductor modeling with Flux ϕ
  - For linear inductor, $\frac{d\phi}{di_L}$ is constant → $\phi = L\, i_L$
    - Therefore, $L = \frac{\phi}{i_L}$
    - In Qspice : flux = L * I(L1) , where L1 is inductor name
  - For nonlinear inductor, ϕ can be approximate by $\phi = a\tanh(b\, i_L)$
    - Therefore, $L = \frac{d\phi}{di_L} = \frac{d\, a\tanh(b\, i_L)}{di_L} = a\, b\,(1 - \tanh^2(b\, i_L))$
    -
    - In Qspice : flux = a*tanh(b*I(L1))
      - L0A @ 0A = a * b
      - b determines the spread
      - If $b\, i_L$ is large, $(1 - \tanh^2(b\, i_L)) = 0$, therefore, this formula will give 0H inductance when i_L is large
  - It can combine nonlinear and linear to handle 0H inductance when i_L is large
    - In Qspice : flux = a*tanh(b*I(Ln)) + Lmin * I(Ln)
    - L0A @ $i_L = 0$: a*b – Lmin
    - Lmin @ $i_L = \infty$: Lmin
    - b determines the spread


```
Assum flux formula is a*tanh(b*IL)+Lmin*IL
.param b = 0.7
.param L0A = 1µ
.param a = (L0A-Lmin)/b
.param Lmin=58n
.func flux() a*tanh(b*IL)+Lmin*IL
Calculate dflux/dIL
.func dflux() D(flux())
Sweep IL from -10A to 10A
.step param IL -10 10 0.2
.op
.plot dflux()
.plot flux()
```

dflux() = Leqv

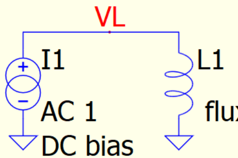
detemine by Lmin



L. Arbitrary Inductance : Inductor modeling with FLUX

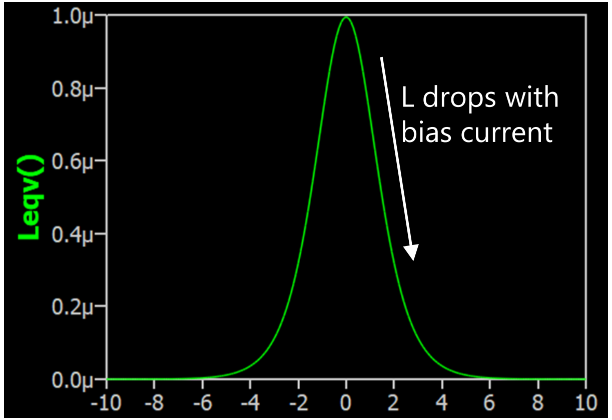
Qspice : L Inductor (AC) - Flux eqn 1.qsch ; L Inductor Nonlinear (Tran) - Flux eqn 1.qsch

- Flux model
  - .ac is used to calculate inductance and bias current relationship
  - .tran is used to demonstrate non-linear inductor current and proportional B-H curve
  - Flux equation uses format
    - Flux = a*tanh(b*I(L1))



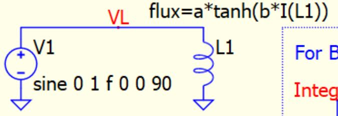

```
.param b = 0.59
.param L0A = 1µ
.param a = L0A/b
flux=a*tanh(b*I(L1))

.param frq=1Meg
.step param bias -10 10 0.1     Sweep bias
.step param var list 1 2 3      Sweep Isat

.ac list frq
.func Leqv() V(VL)/1/2/pi/frq
.plot Leqv()
```

Flux model with .ac

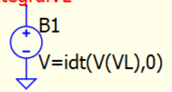


Flux model with .tran

```
.param b = 0.59
.param L0A = 1µ
.param a = L0A/b
flux=a*tanh(b*I(L1))
```

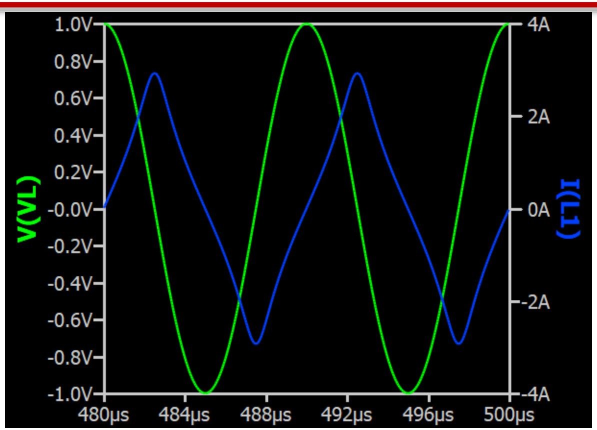


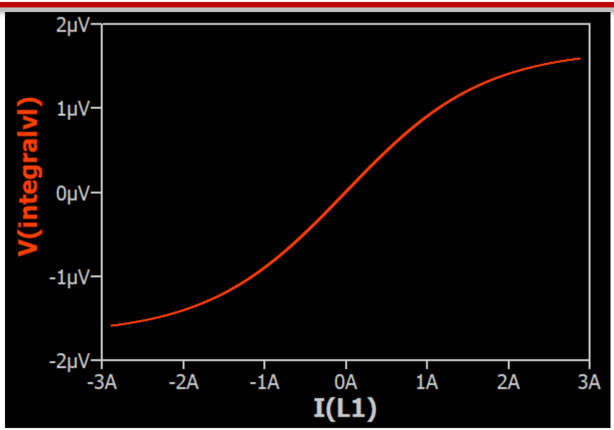
For B-H plot



B proportional to Integral of V(VL)
H proportional to I(IL)

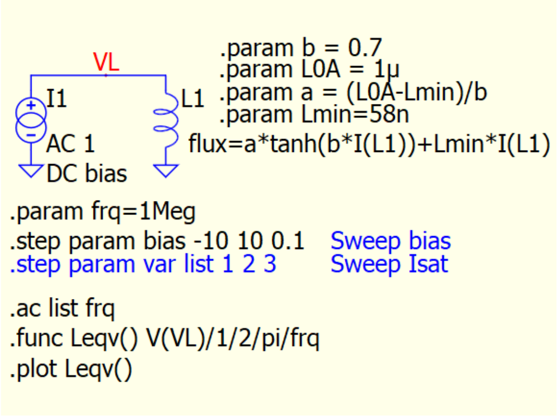
```
.param f=100K
.tran 0 50/f 48/f 1/f/1000 uic
.plot V(VL) I(L1)
```

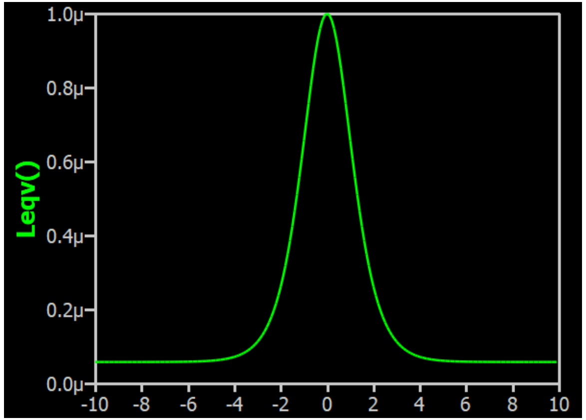


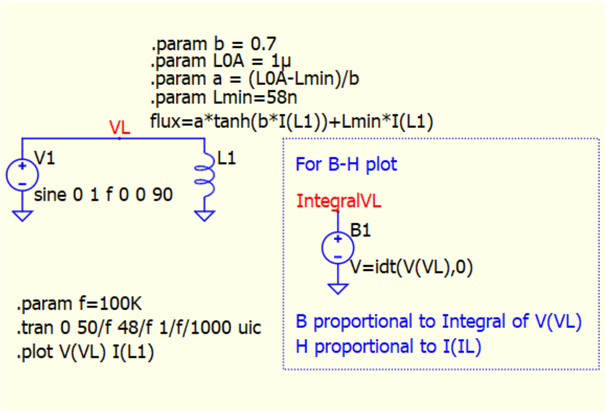


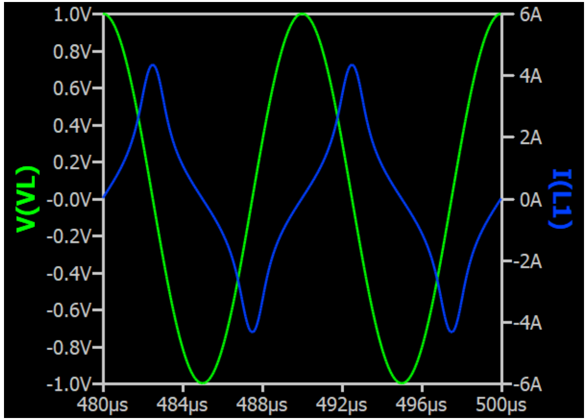
L. Arbitrary Inductance : Inductor modeling with FLUX – Nonlinear with Lmin
Qspice : L Inductor (AC) - Flux eqn 2.qsch ; L Inductor Nonlinear (Tran) - Flux eqn 2.qsch

- Flux Model
  - This is nonlinear flux model include Lmin at large inductor current
  - Flux equation uses format
    - Flux = a*tanh(b*I(L1))+Lmin*I(L1)









L. Inductor

Parameter : Rpar
(Special Topic)

Inductor L Parameter : Rpar

- In Help, L. Inductor section, RPAR is mentioned default = Infinite

RPAR	Equivalent parallel resistance	Ω	Infinite
RSER	Equivalent series resistance	Ω	0.0

- However, this is not absolute truth according to Mike Engelhardt in a Qspice forum, default $\mathrm{Rpar} = \frac{1\mathrm{Meg}}{\mathrm{L}}$

Engelhardt 17d

I think it's hard to find an inductor with less parallel loss than the minimum added by default in QSPICE.

But if you don't like QSPICE'S help on this, you can add an attribute "Rpar=0" to the inductor.

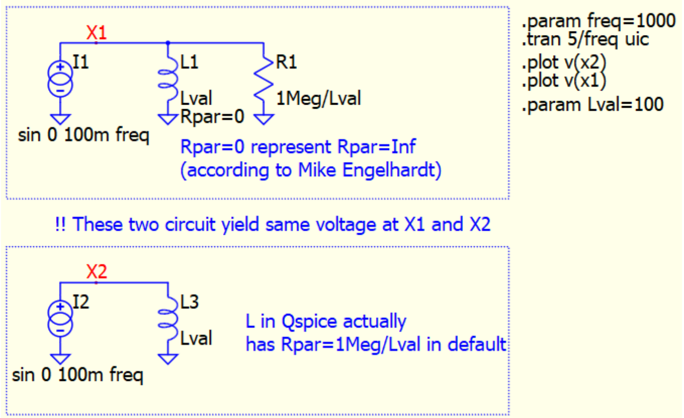
You might want to do the same for the capacitors.

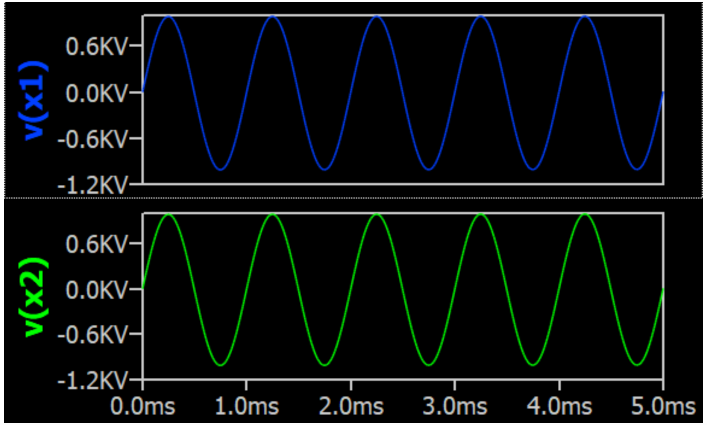
- Setting Rpar = 0 can force equivalent parallel resistance to truly infinite

Prove Rpar = 1Meg/L in Default

Actual Rpar in Default L model - Tran.qsch

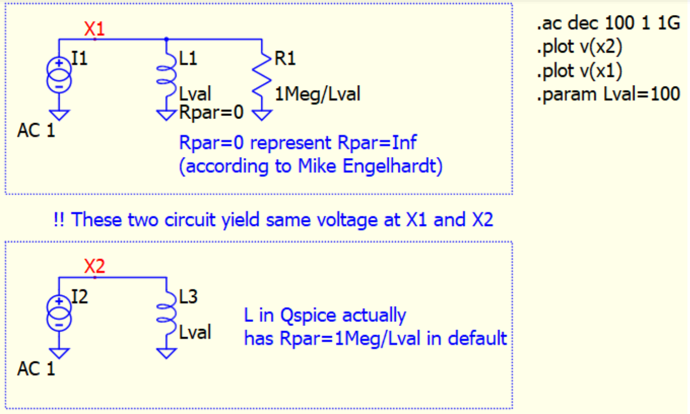
In .tran
Forced Rpar=0 (equal INF)
By adding a 1Meg/L resistor in parallel to L1, its simulation result is same as default L3

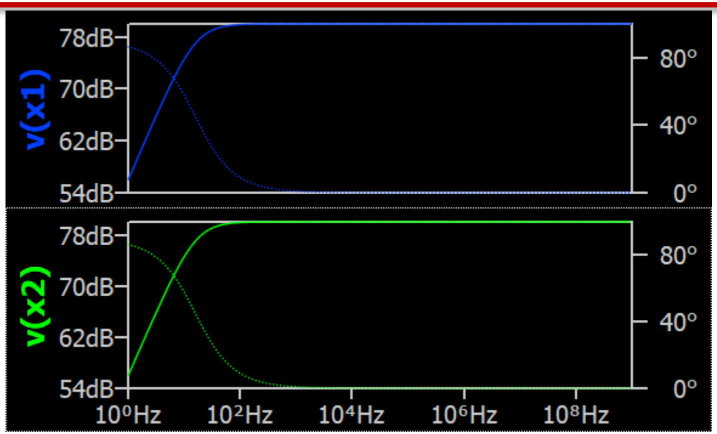




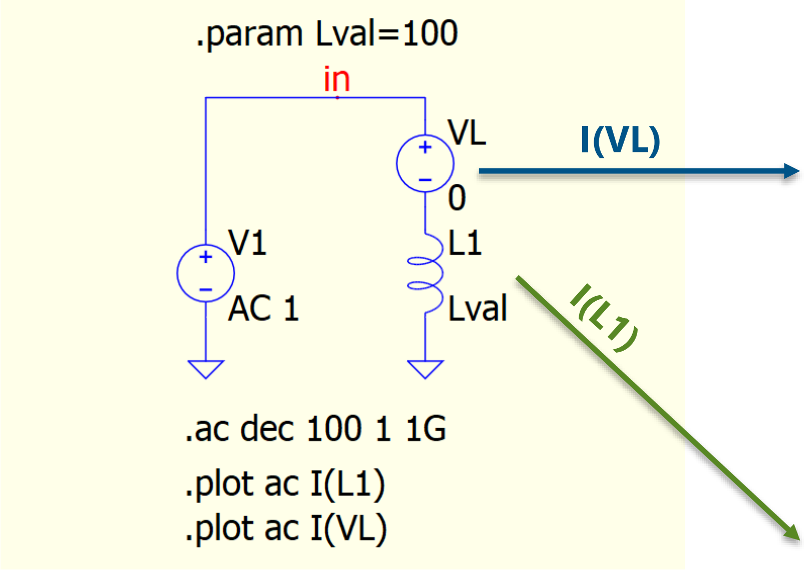
Actual Rpar in Default L model - AC.qsch

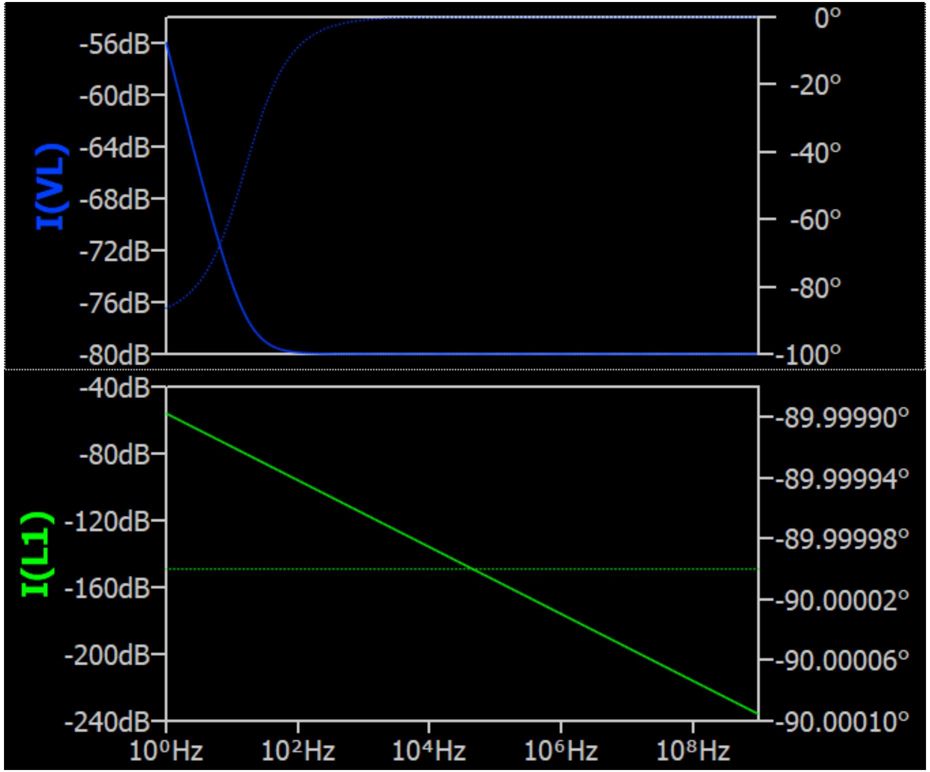
In .ac
Forced Rpar=0 (equal INF)
By adding a 1Meg/L resistor in parallel to L1, its simulation result is same as default L3





What Inductor Current Actually Measured?





L1 has a Rpar = 1Meg/L resistor in parallel
But current probe I(L1) only return current through L but not Rpar, that is why I(VL) ≠ I(L1) as I(VL) measures total current of L and Rpar

Therefore, user may not aware there is a finite Rpar if using voltage source across L and measure current of it

M. MOSFET

(VDMOS)

** VDMOS with different default as monolithic MOSFET models, it popularly used in board level SMPS

MOSFET Level 1 Model Parameters

Refer D. Diode .model parameters

MOSFET Level 1 Model Parameters

Name	Description	Units	Default
A	Additional non-linear Gate-drain capacitance abruptness		1.0
AD	Default drain area	m^2	0.0
AF	Flicker noise exponent		1.0
AS	Default source area	m^2	0.0
BV	Body diode breakdown voltage	V	Infinite
CAPOP [9]	Charge(Capacitance) model		1
CBD	Zero-bias B-D junction capacitance	F	0.0
CBS	B-S junction capacitance	F	0.0
CGBO	Gate-bulk overlap capacitance	F/m	0.0
CGDMAX [8]	Maximum additional non-linear Gate-Drain capacitance	F	0.0
CGDMIN [8]	Minimum additional non-linear Gate-Drain capacitance	F	0.0
CGDO	Gate-drain overlap capacitance	F/m	0.0
CGS	Gate-source capacitance that doesn't scale with width	F	0.0
CGSO	Gate-source overlap capacitance	F/m	0.0
CJ	Bottom junction cap per area	F/m^2	0.0
CJO	Body diode zero-bias capacitance	F	0.0
CJSW	Side junction cap per length	F/m	0.0
EG	Body diode activation energy	V	1.11
ETA [8]	Philips, et al.-style subthreshold conduction parameter		0.0
ETA2	Inverse sharpness of Ids limit for non-square law variation		0.0
FC	Forward bias junction fit parameter		0.5
GAMMA	Bulk threshold parameter	$V^{1/2}$	0.0
GDSNOI	Channel shot noise coefficient(nlev=3)		1.0
GM	Ideal transconductance for non-square law variation	℧	none
GMAX	Maximum bulk PN conductivity	℧	1000.
IBV	Body diode current at breakdown voltage	A	1e-10
IDS	Maximum drain current for non-square law variation	A	Infinite
IGSS	Gate-Source leakage current	A	0.0
IS	Bulk junction saturation current	A	1e-14
JS	Bulk junction saturation current density	A/m^2	0.0
K1 [10]	Threshold voltage sensitivity to bulk node	$V^{1/2}$	0.25
KF	Flicker noise coefficient		0.0
KP	Transconductance parameter	A/V^2	2e-5
L	Default channel length	m	1e-5
LAMBDA	Channel length modulation	V^{-1}	0.0
LD	Lateral diffusion	m	0.0
MJ	Bulk grading coefficient		0.5
MJSW	Side grading coefficient		0.33
N	Bulk(or Body) PN junction emission coefficient		1.0
NBV	Body diode breakdown emission coefficient		1.0
NLEV	Noise level(equation selector)		0
NRD	Default drain squares		0.0
NRB	Default bulk squares		0.0
NRG	Default gate squares		0.0
NRS	Default source squares		0.0
NSS	Surface state density	cm^{-2}	0.0
NSUB	Substrate doping	cm^{-2}	0.0
PB	Bulk junction potential	V	1.0
PD	Default drain perimeter	m	0.0
PHI	Surface potential	V	1.0
PCHAN	Flag to specify vertical PMOS geometry		not set
PS	Default source perimeter	m	0.0
RB	Bulk resistance	Ω	0.0
RD	Drain resistance	Ω	0.0
RDS	Additional Drain-Source shunt resistance	Ω	Infinite
RG	Gate resistance	Ω	0.0
RON	Ron at zero drain current for non-square law variation	Ω	none
RONX [8]	Channel conductivity multiplier in linear region		1.0
RS	Source resistance	Ω	0.0
RSH	Sheet resistance	Ω/□	0.0
TNOM	Parameter measurement temperature(aka TREF)	°C	27.0
TOX	Oxide thickness	m	1.5e-8
TPG	Gate type		1
TT	Bulk PN junction Transit-time	sec	0.0
U0	Surface mobility(aka UO)	$cm^2/V\times sec$	600
VDMOS [8]	Flag to specify vertical geometry		not set
VFB [10]	Flat band voltage	V	-1.0
VIGSS	Voltage at which IGSS was measured	V	5.0
VJ	Body diode Junction potential	V	1.0
VT0	Threshold voltage(aka VTO)	V	0.0
W	Default channel width	m	1e-5
XPART [10]	Channel charge partitioning		1
XTI	Body diode Saturation current temperature exponent		3

Display purpose only

- Vds : VDS rating
- Qq : Gate charge
- Mfg : manufacturer

Linear and Saturation Region : VTO, KP, W, L, LD, LAMBDA

- From Semiconductor Device Modeling with Spice (Section 4.2.3)
  - Linear region : $V_{GS} > V_{TH}$ and $V_{DS} < V_{GS} - V_{TH}$
    - $I_{DS} = KP \frac{W}{L-2X_{jl}}\left(V_{GS} - V_{TH} - \frac{V_{DS}}{2}\right) V_{DS}(1 + \lambda V_{DS})$
  - Saturation region : $V_{GS} > V_{TH}$ and $V_{DS} > V_{GS} - V_{TH}$
    - $I_{DS} = \frac{KP}{2} \frac{W}{L-2X_{jl}}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$
  - where
    - V_{TH} : VTO , zero-bias threshold voltage (Default VTO=0 V)
    - KP : KP , transconductance (Default KP=1 A/V^2)
    - W : W, channel width (Default W=1e-4 m)
    - L : L, channel length (Default L=1e-4 m)
    - X_{jl} : LD, lateral diffusion (Default LD=0 m)
    - λ : LAMBDA channel-length modulation (Default LAMBDA=0 V^{-1})

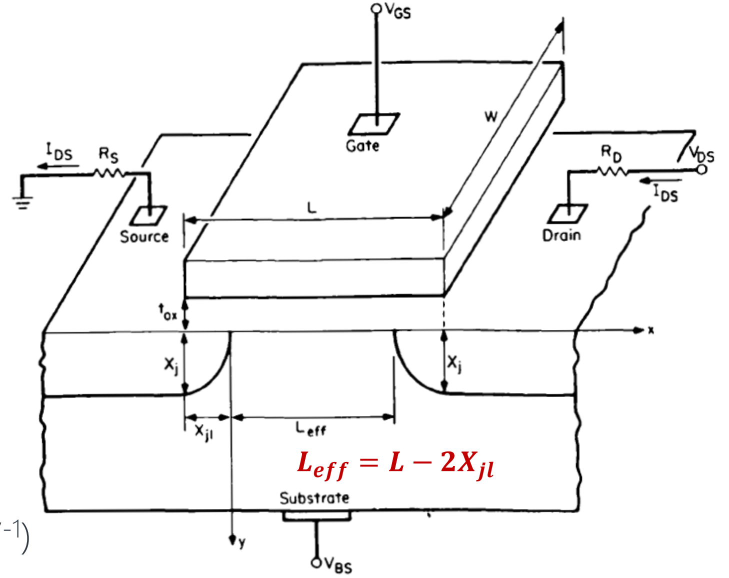


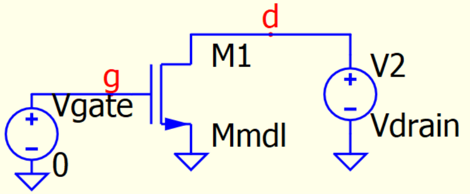
Figure 4-1 Structure of the MOST.

M. MOSFET Params : VTO, KP, W and L

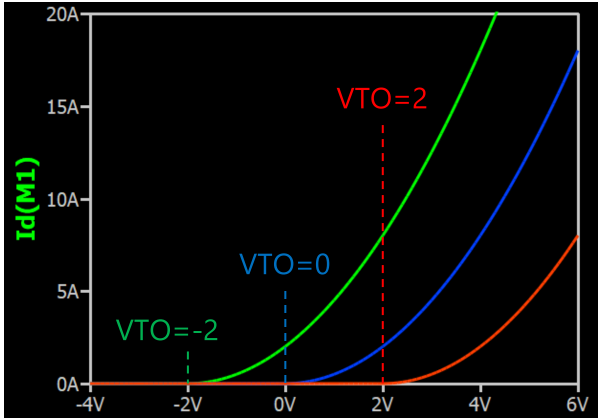
Qspice : VDMOS - VTO.qsch / VDMOS - KP.qsch / VDMOS - W.qsch / VDMOS - L.qsch

- VTO
  - VTO : Zero-bias threshold voltage
  - **Default VTO=0V**

```
.param Vdrain=10
.dc Vgate -4 6 0.1     .plot Id(M1)
```



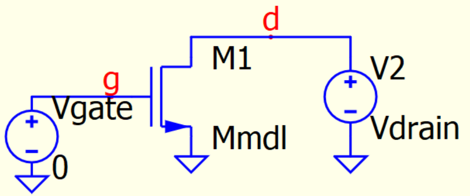

```
.step param vto list -2 0 2
.model Mmdl VDMOS VTO=vto
```



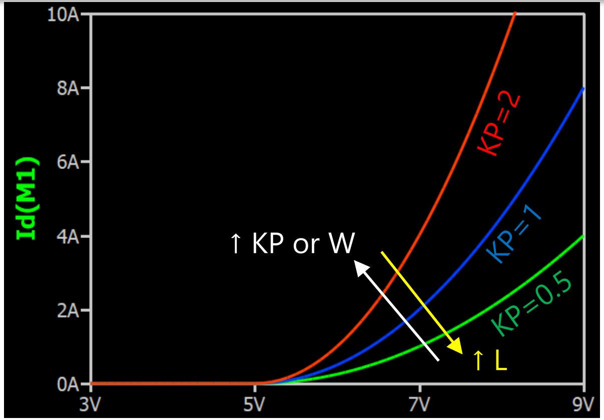
- KP
  - KP : transconductance
  - **Default KP=1 A/V²**

- W and L
  - W : Channel Width (Default 1e-4)
  - L : Channel Length (Default 1e-4)
  - Effect is similar to KP as a gain
    - $\frac{KP}{2}\frac{W}{L-2X_{jl}}$ (for saturation region)

```
.param Vdrain=10
.dc Vgate 3 9 0.1     .plot Id(M1)
```

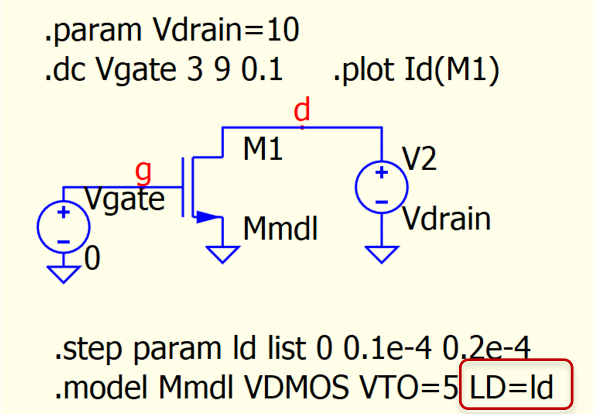


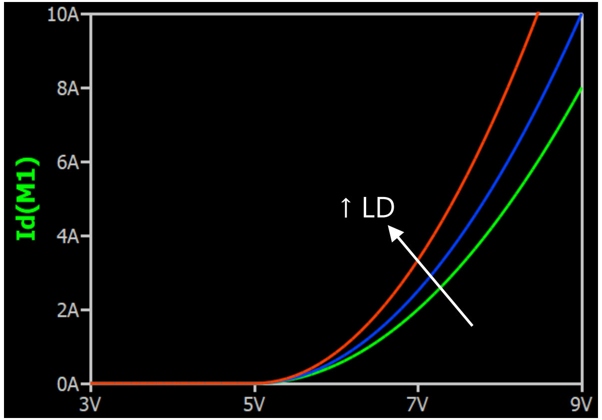

```
.step param kp list 0.5 1 2
.model Mmdl VDMOS VTO=5 KP=kp
```



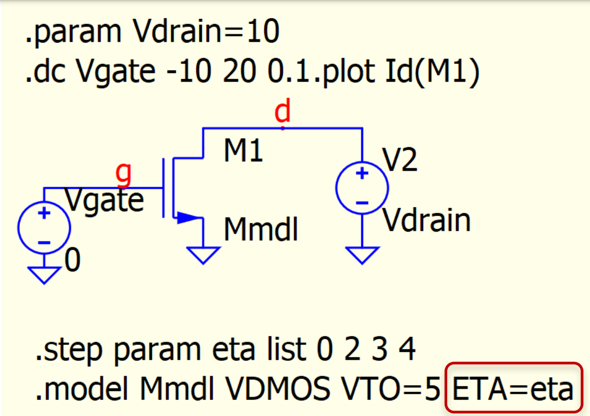
M. MOSFET Params : LD and ETA
Qspice : VDMOS - LD.qsch / VDMOS - ETA.qsch

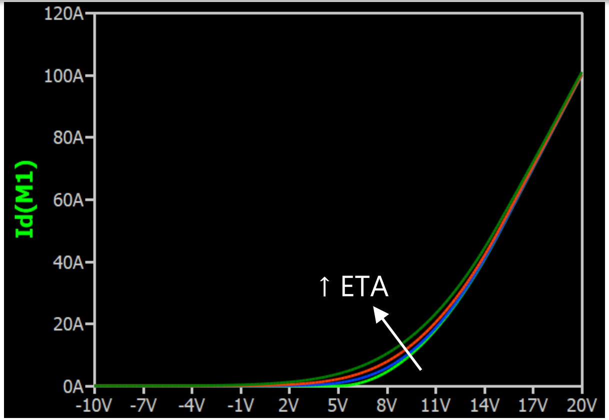
- LD
  - LD : lateral diffusion
  - **Default LD=0 m**
  - $L_{eff} = L - 2LD > 0$
    - Therefore, $0 < LD < \frac{L}{2}$





- ETA (aka ksubthres)
  - ETA : Vds dependence of threshold voltage
  - Static feedback on threshold voltage
  - **Default ETA=0**
  - Qspice accepts parameter name as ETA or ksubthres

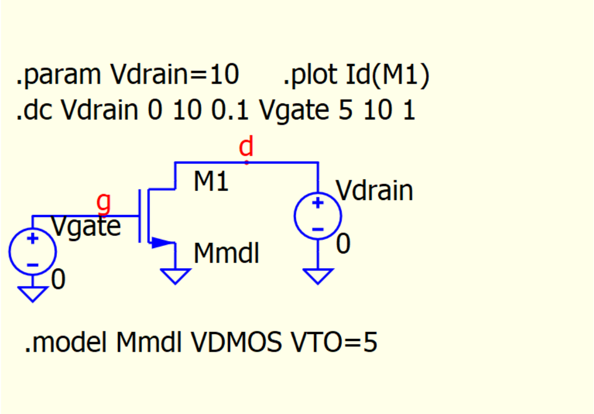


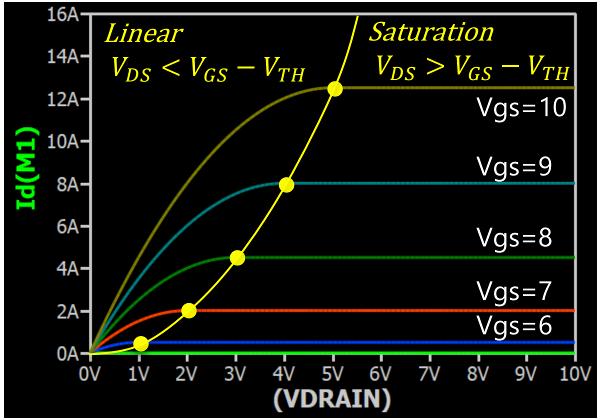


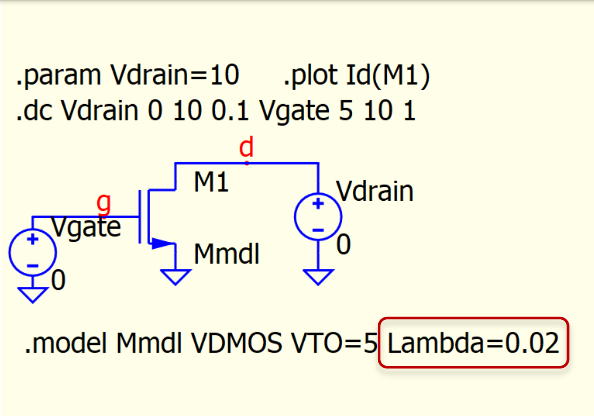
M. MOSFET Params : Lambda

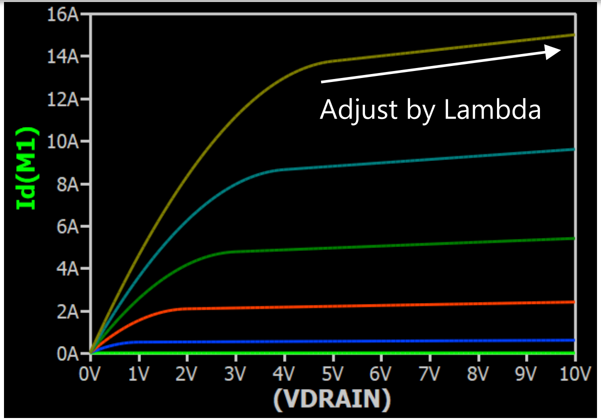
Qspice : VDMOS -LAMBDA.qsch

- LAMBDA
  - Labmda : channel-length modulation
  - **Default LAMBDA=0 V^{-1}**





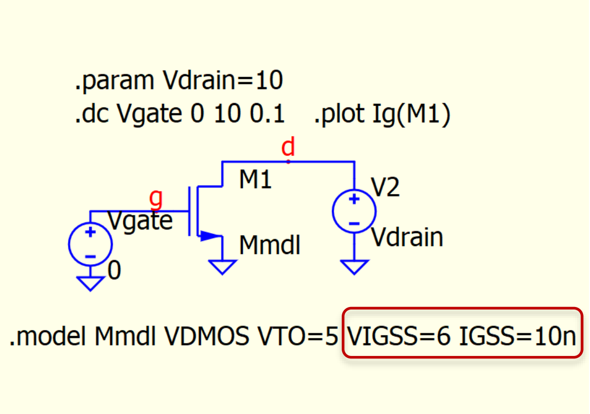


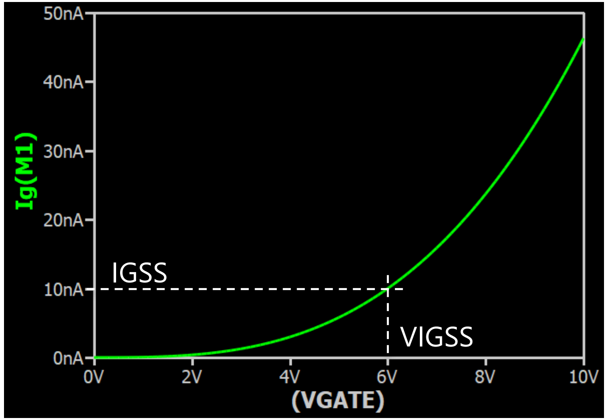


M. MOSFET Params (Gate) : VIGSS and IGSS, RG and CGS

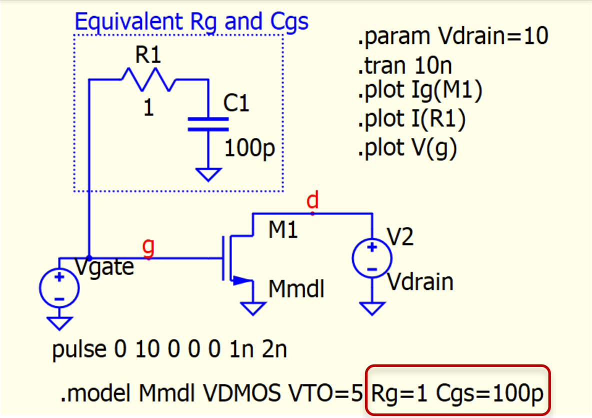
Qspice : VDMOS - VIGSS IGSS.qsch / VDMOS - Rg Cgs.qsch

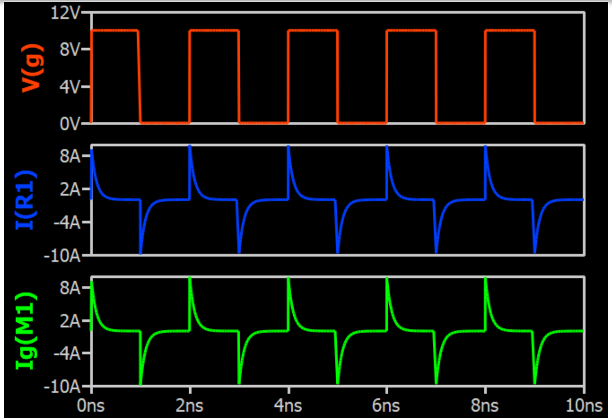
- VIGSS and IGSS
  - Vigss : Voltage at which IGSS was measured
  - Igss : Gate-Source leakage current
  - **Default VIGSS=5V**
  - **Default IGSS=0A**
  - Parameters to determine Igs in relates to Vgs





- RG and CGS
  - Rg : Gate Resistance
  - Cgs : Gate-source capacitance that doesn't scale with width
  - **Default RG=0Ω**
  - **Default CGS=0F**
  - Parameters to determine gate resistance and capacitoance

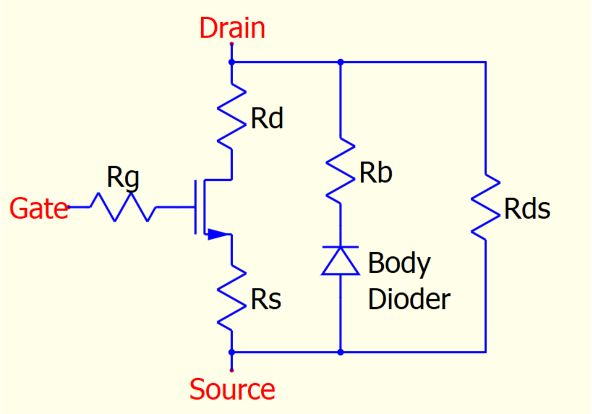




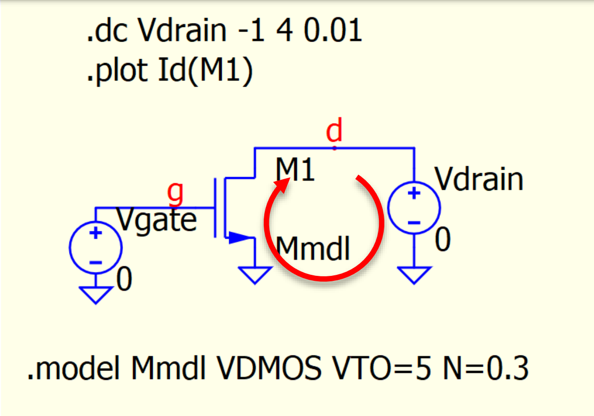
M. MOSFET Params :

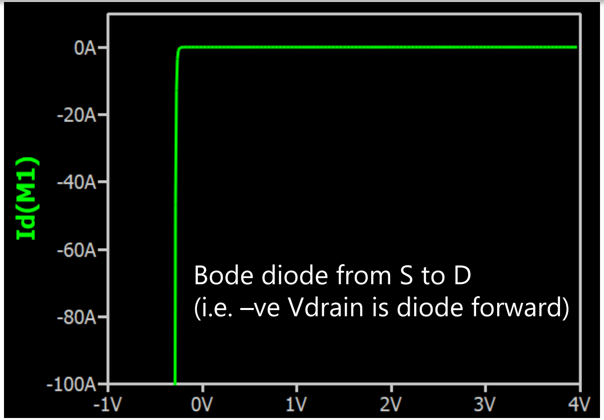
Qspice : VDMOS - BodeDiode.qsch / VDMOS - Rb Rd Rds Rg Rs.qsch

- Resistance
  - Rb : Bulk resistance
  - Rd : Drain resistance
  - Rds : Additional Drain-Source shunt resistance
  - Rg : Gate resistance
  - Rs : Source resistance
  - **Default Rb=Rd=Rg=Rs=0Ω**
  - **Default Rds=Infinite**



- Body Diode
  - Parameters same as diode model parameters
  - Refer to section : D. Diode Diode Model Parameters
  - This idea diode also provide Cds capacitance with its junction capacitance Cj





Drain-Source Turn ON Resistance : Rds,on

- Rds,on
  - This is not a direct parameters, but as to design SMPS, you may want to know what parameters in MOSFET model affect Rds,on
  - In SMPS, Rds,on is generally considered as MOSFET fully turn ON, where
    - $V_{GS} \gg V_{TH}$ and V_{DS} is low, MOSFET in linear region, and $R_{DS,on} = \frac{V_{DS}}{I_{DS}}$
  - Linear region formula : $V_{GS} > V_{TH}$ and $V_{DS} < V_{GS} - V_{TH}$
    - $I_{DS} = KP \frac{W}{L-2X_{jl}}\left(V_{GS} - V_{TH} - \frac{V_{DS}}{2}\right) V_{DS}(1 + \lambda V_{DS})$
  - Therefore
    - $R_{DS,on} = \frac{V_{DS}}{I_{DS}} = \frac{V_{DS}}{KP\frac{W}{L-2X_{jl}}\left(V_{GS}-V_{TH}-\frac{V_{DS}}{2}\right)V_{DS}(1+\lambda V_{DS})} = \frac{1}{KP\frac{W}{L-2X_{jl}}\left(V_{GS}-V_{TH}-\frac{V_{DS}}{2}\right)(1+\lambda V_{DS})}$
    - $\lim_{V_{DS}\to 0} R_{DS,on} = \frac{1}{KP\frac{W}{L-2X_{jl}}\left(V_{GS}-V_{TH}-\frac{0}{2}\right)(1+\lambda\times 0)} = \frac{1}{KP\frac{W}{L-2X_{jl}}(V_{GS}-V_{TH})} = \frac{L-2X_{jl}}{KP\cdot W\cdot(V_{GS}-V_{TH})}$
  - With Qspice model parameters, also consider drain and source resistance in model
    - $@V_{DS} \to 0\mathrm{V}$: $R_{DS,on} = \frac{\mathrm{L}-2\ \mathrm{LD}}{\mathrm{KP}\cdot\mathrm{W}\cdot(V_{GS}-\mathrm{VTO})} + \mathrm{RD} + \mathrm{RS}$
      - Where in default, VTO=0, KP=1, L=1e-4, W=1e-4, LD=0, Rd=0 and Rs=0

Drain-Source Turn ON Resistance : Rds,on

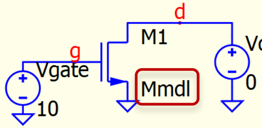
Qspice : VDMOS - (Calculate) Rdson.qsch

- Example #1
  - Mmdl model
  - $@V_{DS} \rightarrow 0\text{V}$
  - $R_{DS,on} = \frac{\text{L}-2\ \text{LD}}{\text{KP}\cdot\text{W}\cdot(V_{GS}-\text{VTO})} + \text{RD} + \text{RS}$
    - RD=0
    - RS=0
  - $R_{DS,on}@V_{DS} \rightarrow 0\text{V} = 141.67\text{m}\Omega$

.dc Vdrain 1p 5 0.01

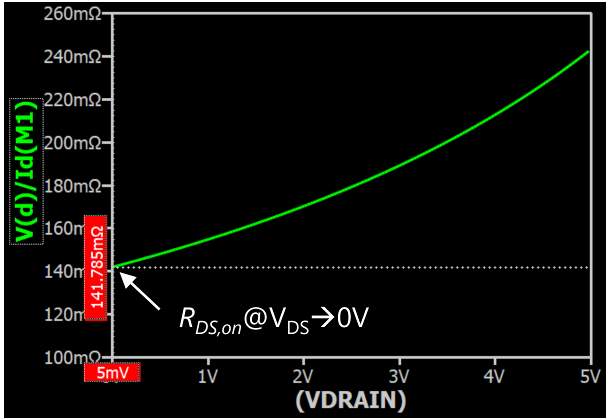
Calculate Rds,on

.plot V(d)/Id(M1)



.model Mmdl VDMOS VTO=4 KP=2 L=4e-4 W=2e-4 LD=3e-5

.model IRF530 VDMOS Rg=3 Vto=4 Rd=50m Rs=12m
+Rb=60m Kp=5 lambda=.01 Cgdmax=1n Cgdmin=.26n
+Cgs=.2n Cjo=.4n Is=52p ksubthres=.1
+mfg=International_Rectifier Vds=100 Ron=160m Qg=26n

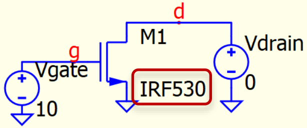


- Example #2
  - Mmdl model
  - $@V_{DS} \rightarrow 0\text{V}$
  - $R_{DS,on} = \frac{\text{L}-2\ \text{LD}}{\text{KP}\cdot\text{W}\cdot(V_{GS}-\text{VTO})} + \text{RD} + \text{RS}$
    - VTO=4, KP=5
    - L=W=1e-4, LD=0
    - RD=50m
    - RS=12m
  - $R_{DS,on}@V_{DS} \rightarrow 0\text{V} = 95.33\text{m}\Omega$

.dc Vdrain 1p 5 0.01

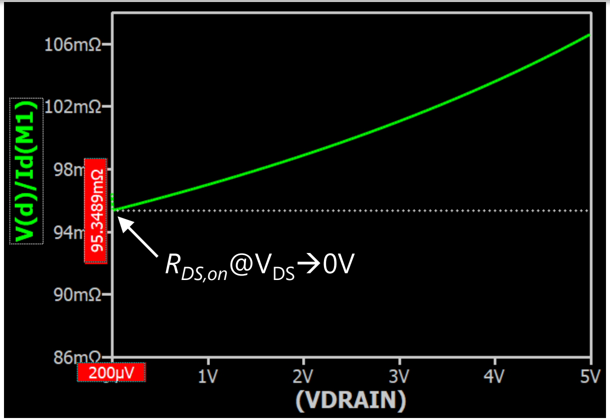
Calculate Rds,on

.plot V(d)/Id(M1)



.model Mmdl VDMOS VTO=4 KP=2 L=4e-4 W=2e-4 LD=3e-5

.model IRF530 VDMOS Rg=3 Vto=4 Rd=50m Rs=12m
+Rb=60m Kp=5 lambda=.01 Cgdmax=1n Cgdmin=.26n
+Cgs=.2n Cjo=.4n Is=52p ksubthres=.1
+mfg=International_Rectifier Vds=100 Ron=160m Qg=26n

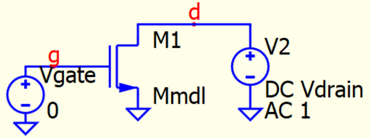


M. MOSFET Params (Cgd) : CGDMAX, CGDMIN and A

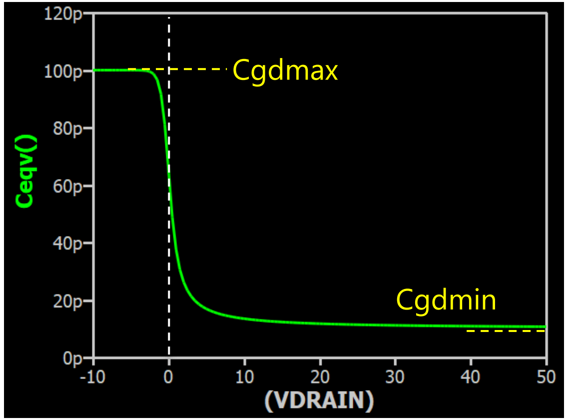
Qspice : VDMOS - CGDMIN CGDMAX.qsch / VDMOS - A.qsch

- CGDMAX and CGDMIN
  - Cgdmax : Maximum additional non-linear Gate-Drain capacitance
  - Cgdmin : Minimum additional non-linear Gate-Drain capacitance
  - **Default Cgdmax=0F**
  - **Default Cgdmin=0F**
  - Model non-linear of Cgd capacitance

```
.param f=10Meg
.ac list f
.step param Vdrain -10 50 0.5
Calculate Capacitance
.func imZ() imag(V(d)/Ig(M1))
.func Ceqv() -1/2/pi/f/imZ()
.plot Ceqv()
```

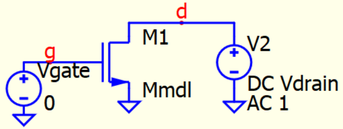



```
.model Mmdl VDMOS VTO=5 Cgdmin=10p Cgdmax=100p
```

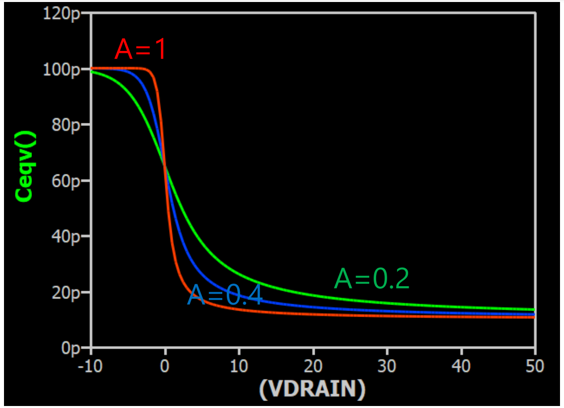


- A
  - A : Additional non-linear Gate-drain capacitance abruptness
  - **Default A=1**
  - Modify Cgd vs drain voltage profile

```
.param f=10Meg
.ac list f
.step param Vdrain -10 50 0.5
.step param a list 0.2 0.4 1
Calculate Capacitance
.func imZ() imag(V(d)/Ig(M1))
.func Ceqv() -1/2/pi/f/imZ()
.plot Ceqv()
```




```
.model Mmdl VDMOS VTO=5 Cgdmin=10p Cgdmax=100p A=a
```



Q. Bipolar Transistor

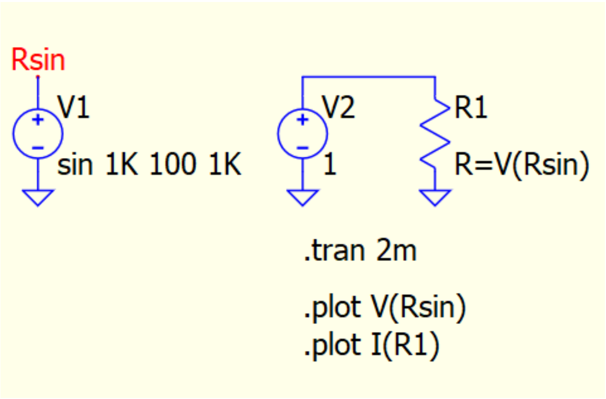
R. Resistor

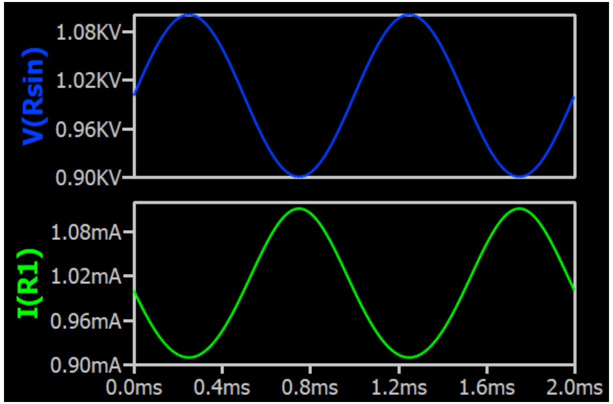
Behavioral Resistor

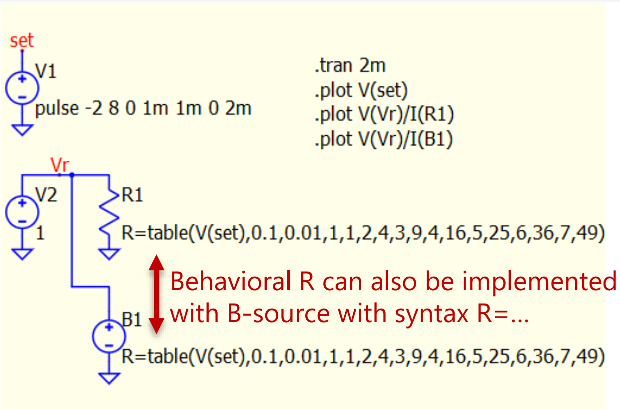
Behavioral Resistor (R)

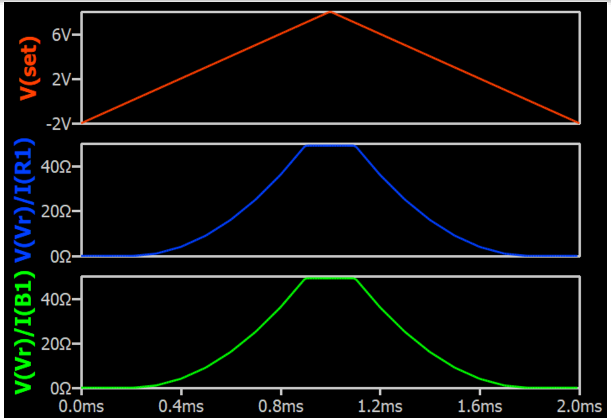
Qspice : Behavioral R Demo 01.qsch ; Behavioral R Demo 02.qsch

- Behavioral Resistor
  - To use formula or voltage/current node for resistance, type R=... in <val> of resistor
  - Also support to use Behavioral source (B) for behavioral resistor
    - Replace V=expression with R=expression









S. Voltage Controlled Switch

S. Voltage Controlled Switch Model Parameters

- S. Voltage Controlled Switch Model Parameters
  - It is common to define Switch Model for usage as multiple switches in a schematic
  - Syntax: Snnn N1 N2 NC+ NC- <model> [instance parameters]
  - .model <model> SW [model parameters]

Voltage Controlled Switch Model Parameters

Name	Description	Units	Default
ETA[1]	Sub-/over-Threshold conduction	V	0.0
ROFF	Off resistance	Ω	1e6
RON	On resistance	Ω	1.0
TTOL	Temporal tolerance	sec	1e308
VH	Hysteresis voltage	V	0.0
VOFF	Voltage when open	V	0.0
VON	Voltage when closed	V	0.0
VT	Threshold voltage	V	0.0

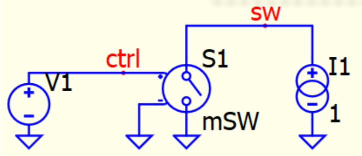
Input Control Voltage

Switch Model Params : Ron, Roff, VT, Von and Voff

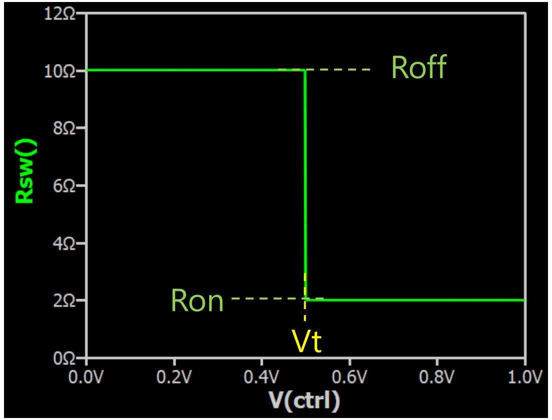
Qspice : Switch - Ron Roff VT.qsch

- RON, ROFF, VT
  - Ron : On resistance
  - Roff : Off resistance
  - VT : Threshold voltage

```
.model mSW SW Ron=2 Roff=10 Vt=0.5 Vh=0
```

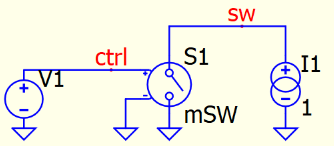



```
pulse 0 1 0 1 1 1 4
.tran 4
.func Rsw() V(sw)/I(I1)
.plot Rsw()
.plot V(ctrl)
```

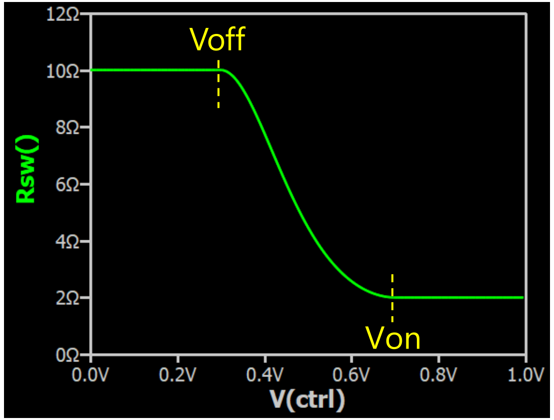


- VON, VOFF
  - Von : Voltage when closed
  - Voff : Voltage when open
  - switch smoothly transitions between on and off
  - If VT and VH are specified, VON and VOFF are ignored

```
.model mSW SW Ron=2 Roff=10 Von=0.7 Voff=0.3
```




```
pulse 0 1 0 1 1 1 4
.tran 4
.func Rsw() V(sw)/I(I1)
.plot Rsw()
.plot V(ctrl)
```



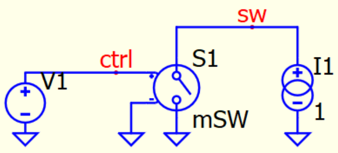
Switch Model Params : VH

Qspice : Switch - VH.qsch

- VH
  - Vh : Hysteresis voltage

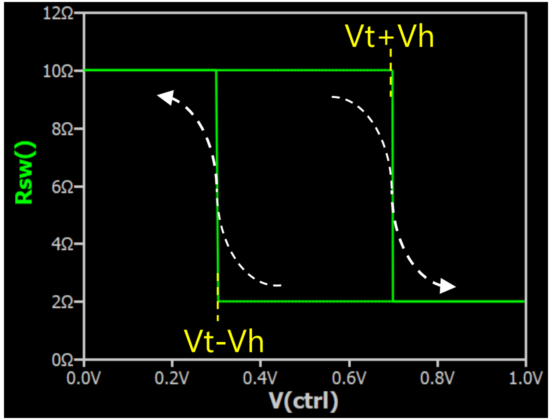
.model mSW SW Ron=2 Roff=10 Vt=0.5 Vh=0.2

+ve Vh



pulse 0 1 0 1 1 4

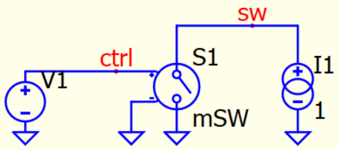
.tran 4
.func Rsw() V(sw)/I(I1)
.plot Rsw()
.plot V(ctrl)



- VH (-vegetive explains)
  - Negative Vh
  - If VH is negative the switch smoothly transitions between on and off

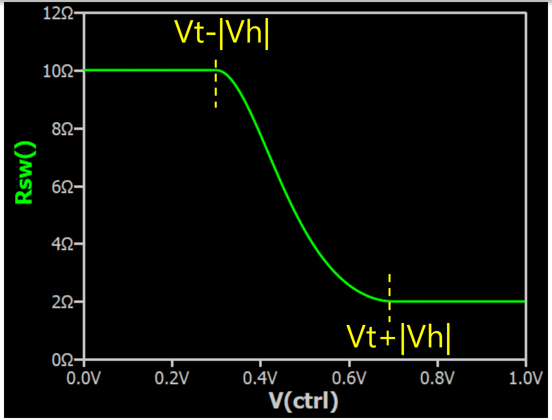
.model mSW SW Ron=2 Roff=10 Vt=0.5 Vh=-0.2

-ve Vh



pulse 0 1 0 1 1 4

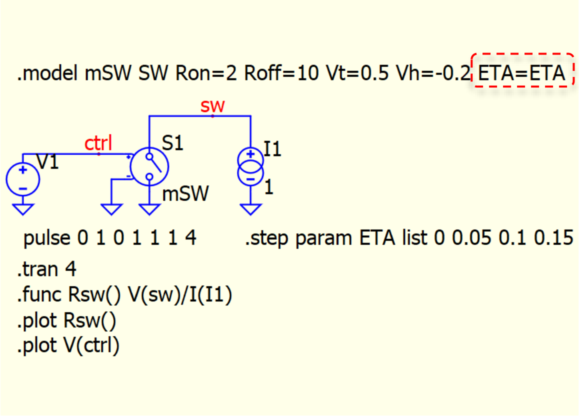
.tran 4
.func Rsw() V(sw)/I(I1)
.plot Rsw()
.plot V(ctrl)

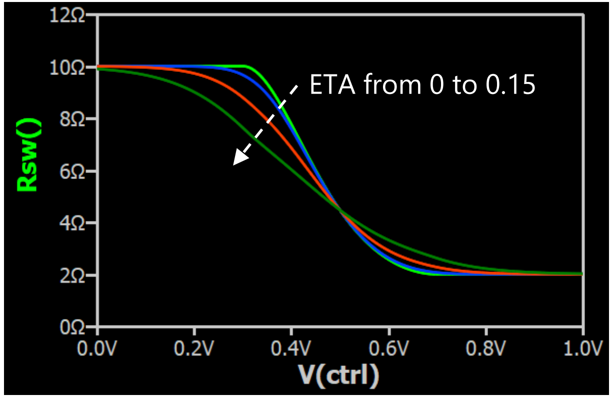


Switch Model Params : ETA

Qspice : Switch - ETA.qsch

- ETA
  - ETA : Sub-/over- Threshold conduction
  - Prevents the control voltage Jacobian from vanishing
  - Only effective in smoothly transitions cases
    - Vt is negative
    - Von / Voff are used without Vt and Vh

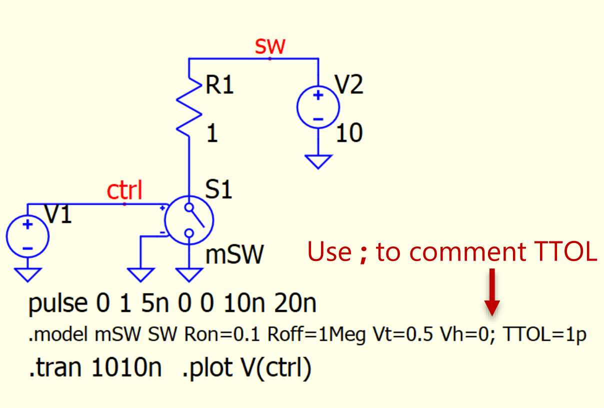


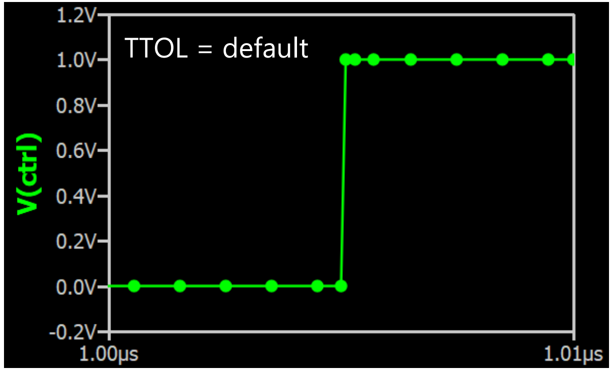


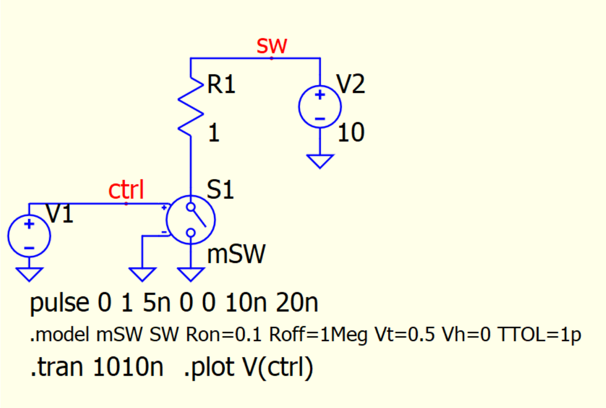
Switch Model Params : TTOL

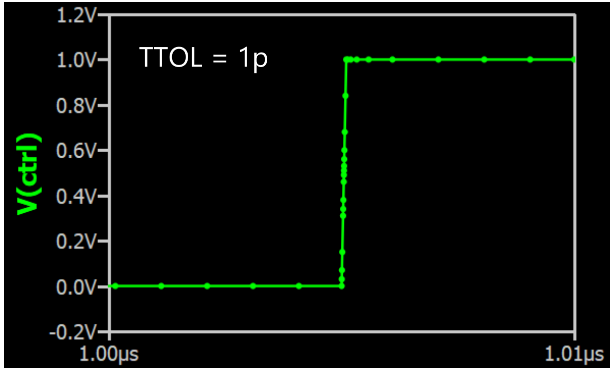
Qspice : Switch - TTOL.qsch

- TTOL
  - Ttol : Temporal tolerance
  - **Default TTOL=1e308s**
- Usage
  - TTOL allows one to determine how accurately the switch time should be found
  - It only affect timestep at switch time, which maintain simulation speed but improve accuracy at switching or logic action









T. Lossless Transmission Line

T. Lossless Transmission Line Instance Parameters

- T. Lossless Transmission Line
  - Syntax: Tnnn L+ L- R+ R- Zo=<value> Td=<value>

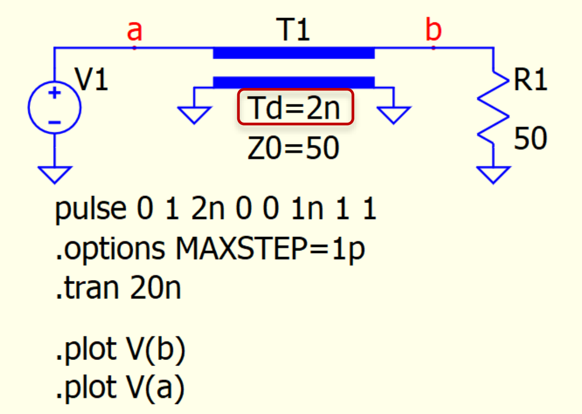
Lossless Transmission Line Instance Parameters

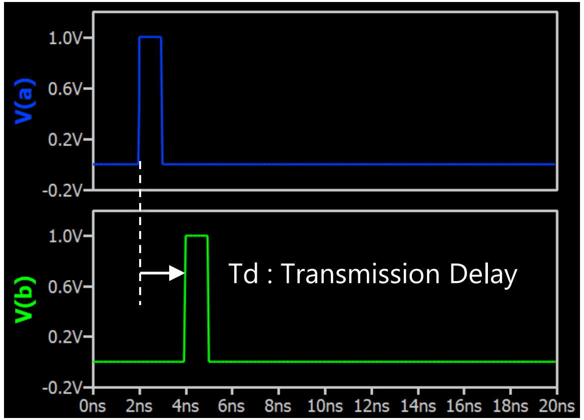
Name	Description	Units	Default
F [1]	Frequency	Hertz	1GHz
NL [1]	Normalized length at frequency given	wavelengths	¼
TD	Transmission delay	sec	
Z0	Characteristic impedance(aka ZO)	Ω	50Ω

T. Instance Params : TD, F and NL

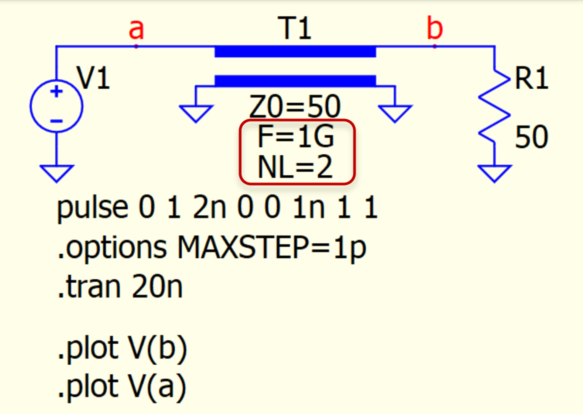
Qspice : Tline - Td.qsch ; Tline - F NL.qsch

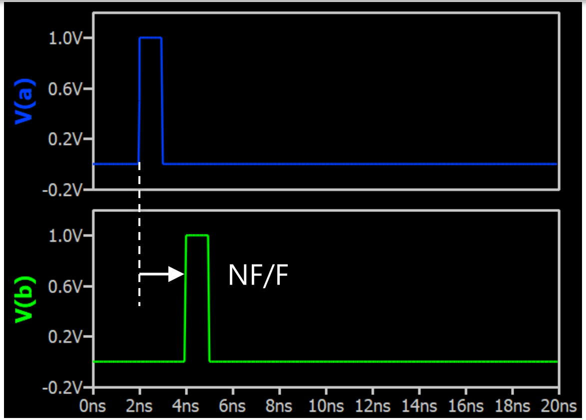
- TD
  - Td : Transmission delay
  - This simulation terminate transmission line with characteristic impedance Zo, no reflection of signal
  - If TD is given, F and NL are ignored





- F and NL
  - F : Frequency
  - NL : Normalized length at frequency given
  - Equation
    - $NL = \frac{Length}{Wavelength} = \frac{Length}{\lambda}$
    - Period per λ : $T = \frac{1}{F}$
    - Delay $T_d = T \times \frac{Length}{\lambda} = \frac{NL}{F}$



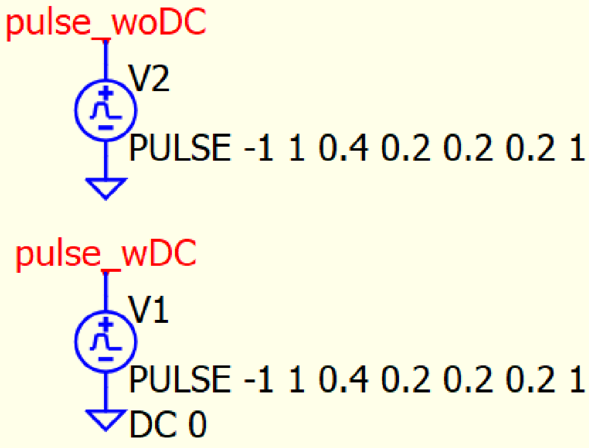


V. Voltage Source

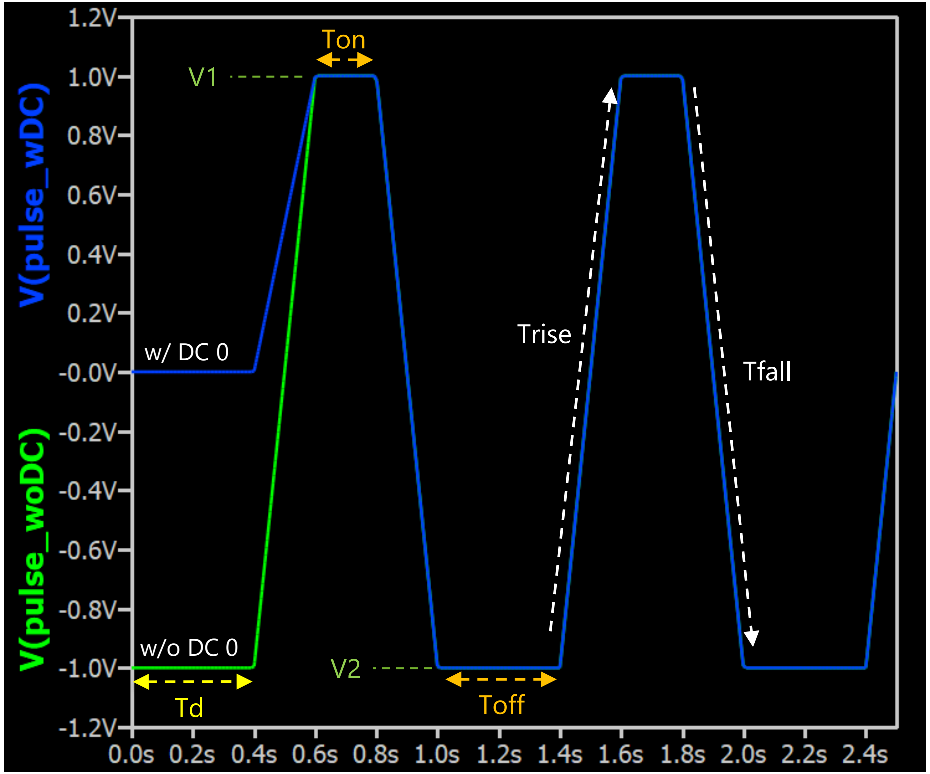
V. Voltage Source : PULSE (Pulse)

Qspice : Vsource PULSE.qsch

Syntax : PULSE V1 V2 Td Trise Tfall Ton Tperiod



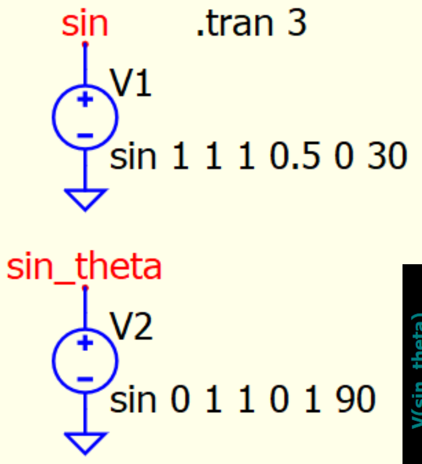
.tran 2.5
.plot V(pulse_woDC) V(pulse_wDC)



V. Voltage Source : SIN (Sine Wave)

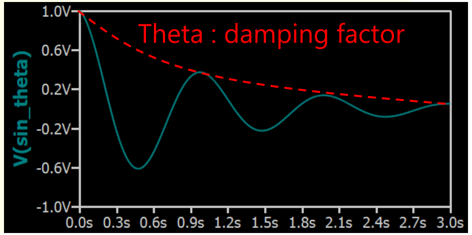
Qspice : Vsource SIN.qsch

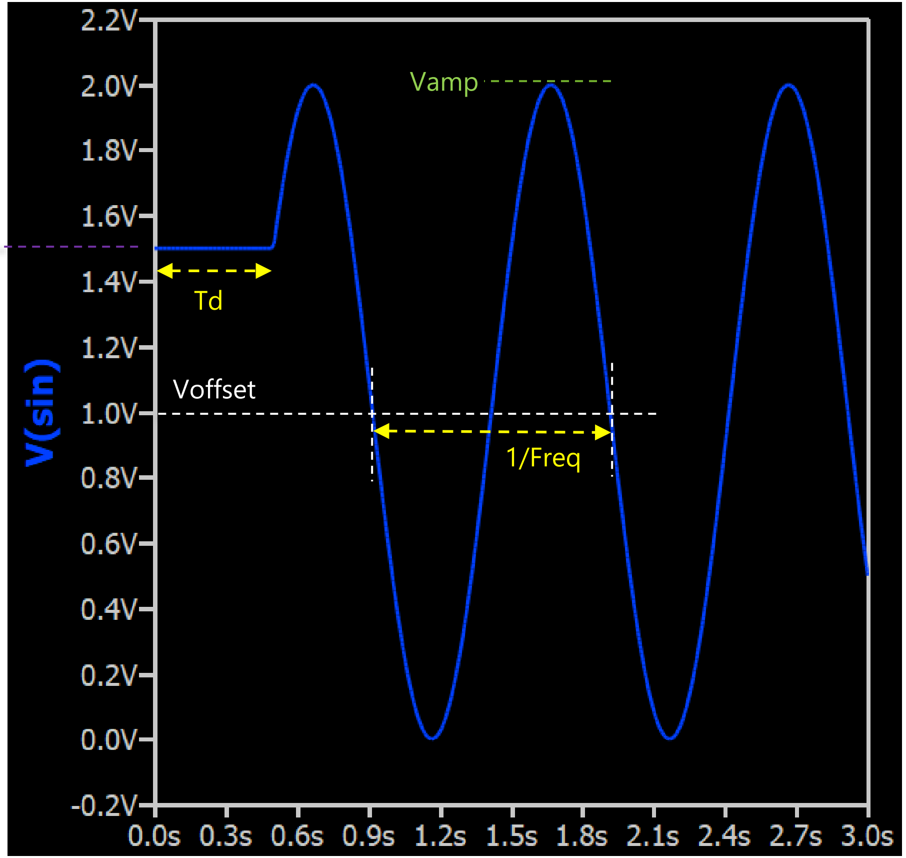
Syntax : SIN Voffset Vamp Freq Td Theta Phi



Phi : level = Voffset + sin(Phi)
e.g.: =1+sin(30º) = 1.5

Amplitude drops by e^{-1}~0.378 in 1/Theta seconds





V. Voltage Source : EXP (Exponential)

Qspice : Vsource EXP.qsch

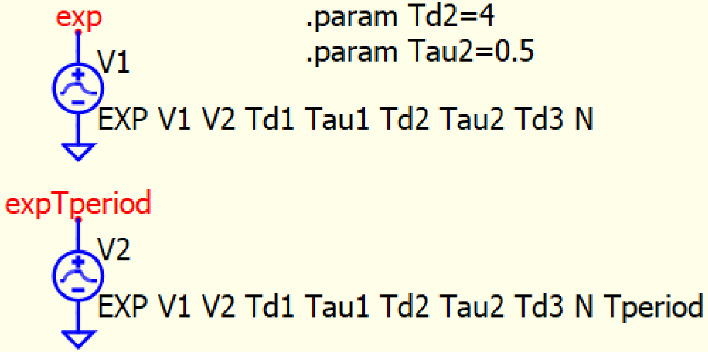
.plot V(expTperiod) V(exp)

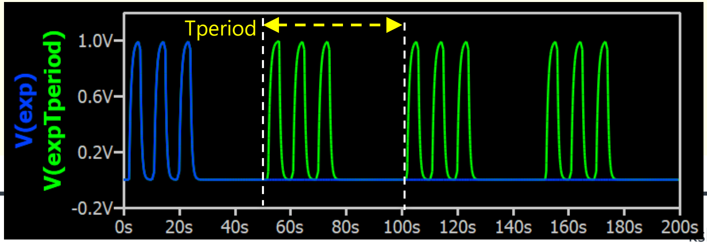
Syntax : EXP V1 V2 Td1 Tau1 Td2 Tau2 Td3 N Tperiod

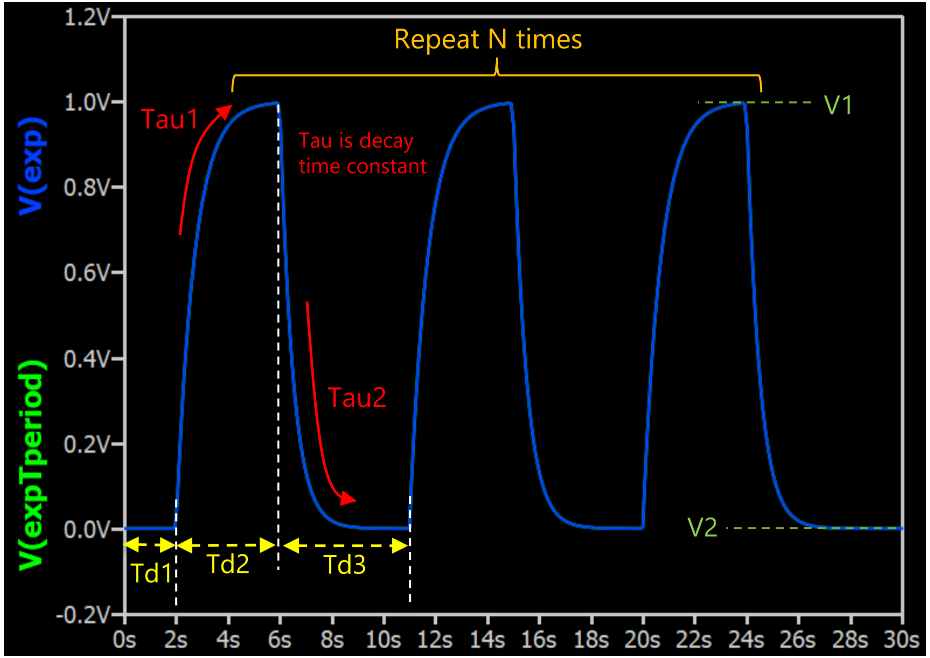
.tran 200

.param V1=0
.param V2=1
.param Td1=2
.param Tau1=0.7
.param Td2=4
.param Tau2=0.5

.param Td3=9
.param N=3
.param Tperiod=50

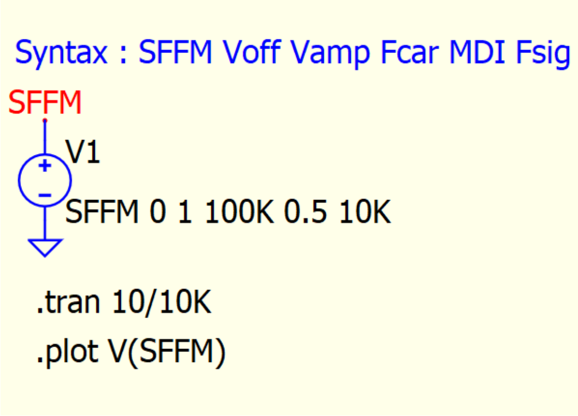




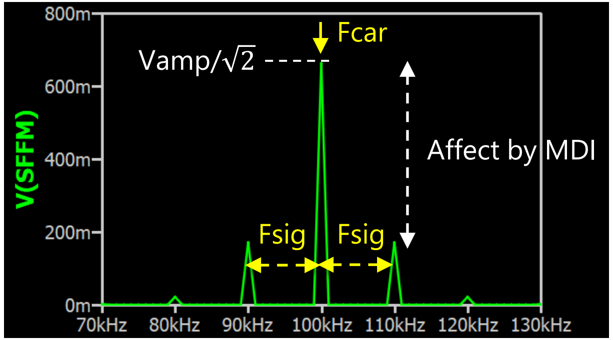


V. Voltage Source : SFFM (Single Frequency FM)
Qspice Vsource SFFM.qsch

- SFFM
  - Single Frequency FM
  - It is hard to observe FM signal in time domain waveform
  - FFT is used to explain its nature



FFT magnitude is RMS

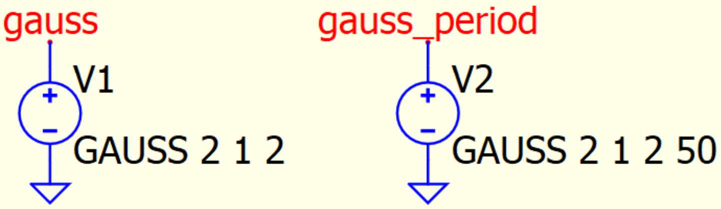


- Transient formula
  - Voff+Vamp*sin((2p*Fcar*time)+MDI*sin(2p*Fsig*time))

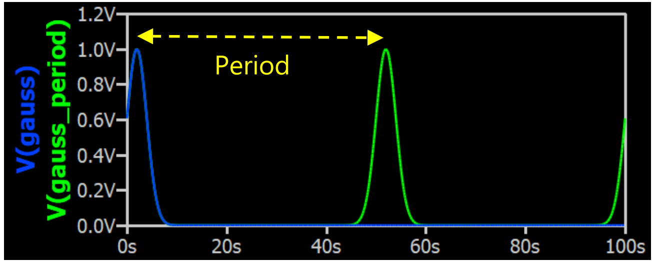
V. Voltage Source : GAUSS (Gaussian Pulse)

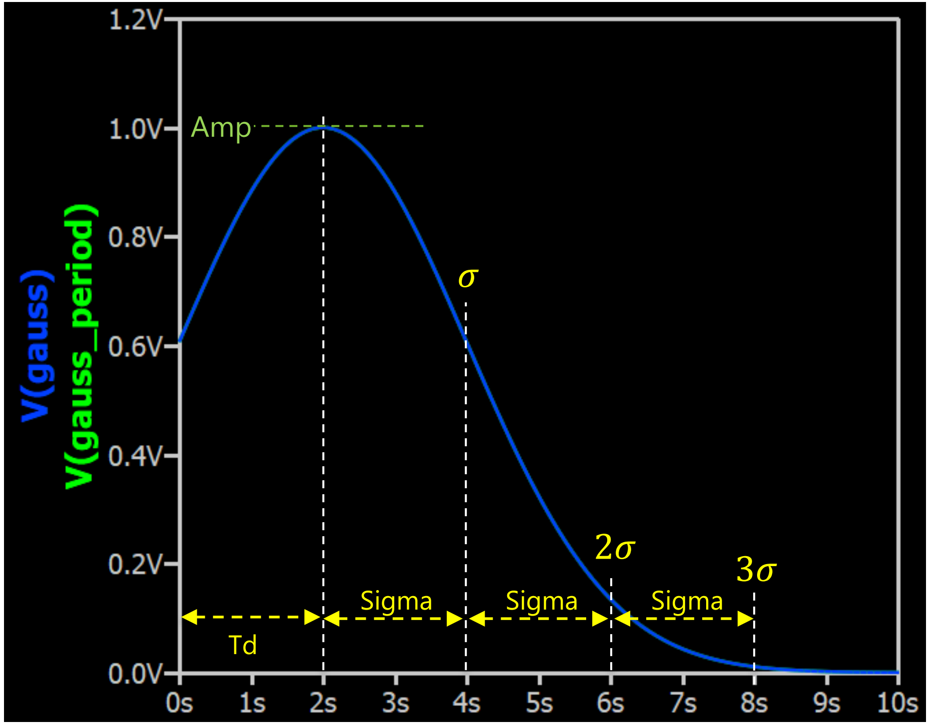
Qspice Vsource GAUSS.qsch

Syntax : GAUSS Td Amp Sigma [Period]




```
.plot V(gauss_period) V(gauss)
.tran 100
```

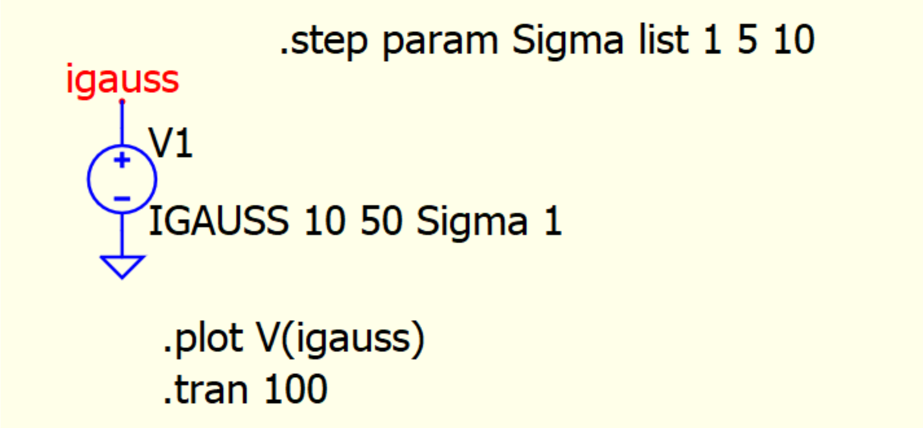


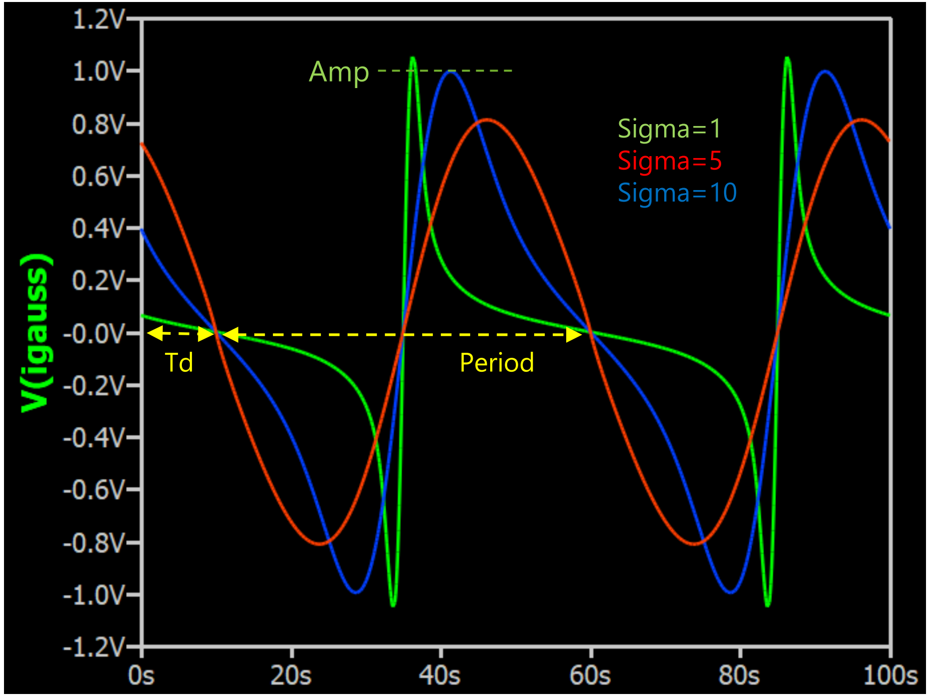


V. Voltage Source : IGAUSS (Imaginary Gaussian Pulse)

Qspice Vsource IGAUSS.qsch

Syntax : IGAUSS Td Period Sigma Amp





V. Voltage Source : CHIRP (Piece-wise Linear Chirp)

Qspice Vsource Chirp.qsch

Syntax : CHIRP(AMP T1 FREQ1 T2 FREQ2 [...]) [LOG] [XTRAP]

```
.param AMP=1
.param T1=5
.param FREQ1=1
.param T2=15
.param FREQ2=2
.param T3=30
.param FREQ3=10
```

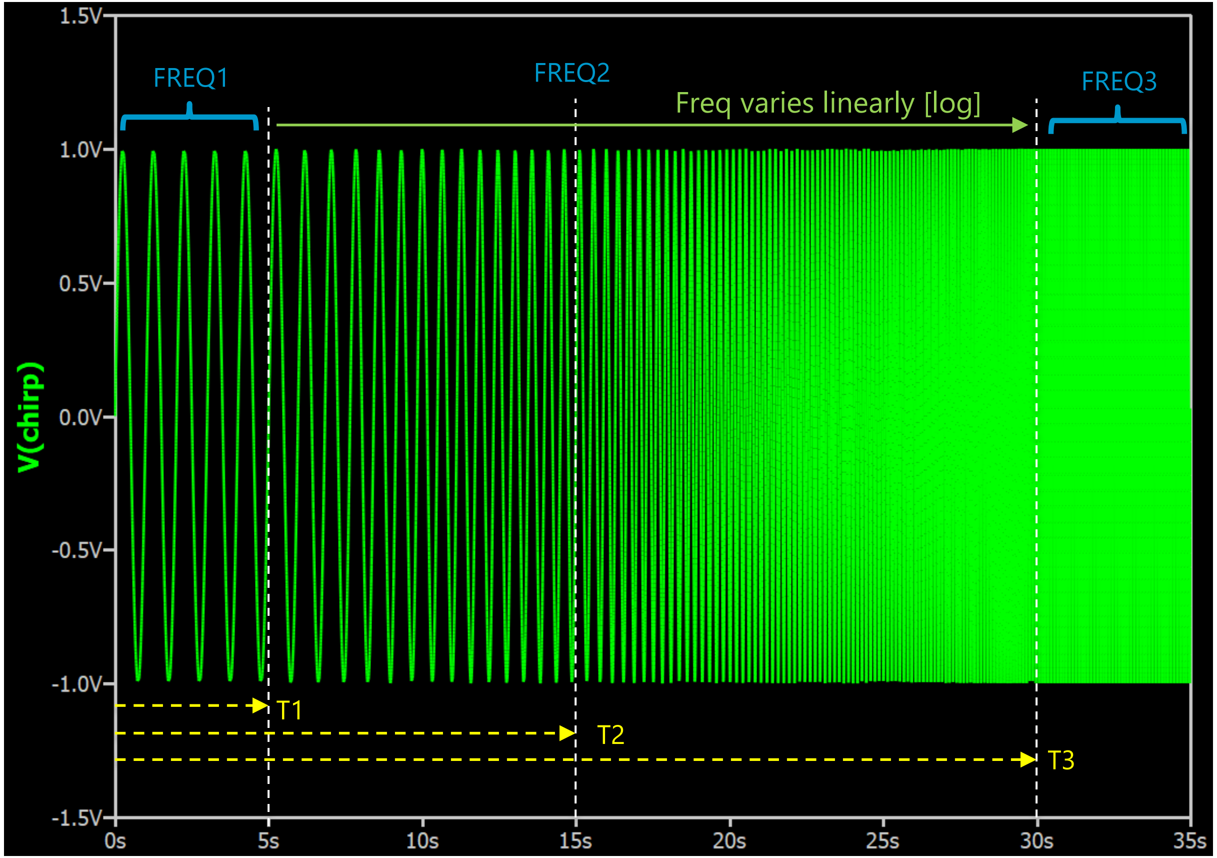
chirp

V1

CHIRP AMP T1 FREQ1 T2 FREQ2 T3 FREQ3

```
.plot V(chirp)
.tran 35
.options MAXSTEP=1/1000
```

XTRAP : extrapolate beyond PWL and CHIRP points

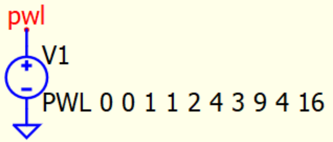


V. Voltage Source : PWL (Piece-wise Linear)

Qspice Vsource PWL.qsch ; Vsource PWL-Log.qsch ; Vsource PWL file.qsch

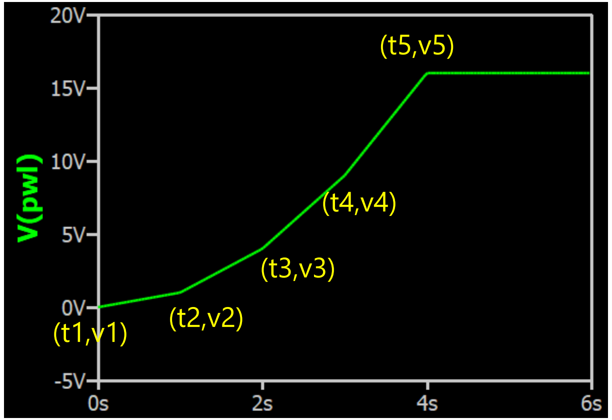
XTRAP : extrapolate beyond PWL and CHIRP points

Syntax : PWL(t1 v1 t2 v2 t3 v3...) [LOG] [XTRAP]

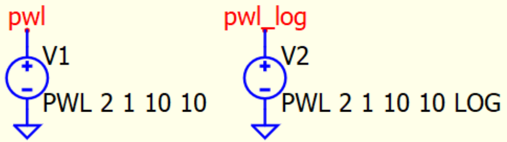


.tran 6
.plot V(pwl)

Vsource PWL.qsch

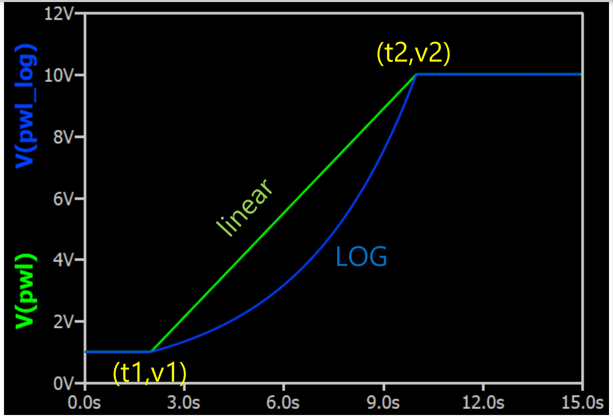


Syntax : PWL(t1 v1 t2 v2 t3 v3...) [LOG] [XTRAP]



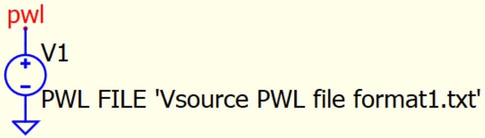
.tran 15
.plot V(pwl) V(pwl_log)

Vsource PWL-Log.qsch



Support load time/value from file.txt

Syntax : PWL FILE file.txt [LOG] [XTRAP]



.tran 12
.plot V(pwl)

Vsource PWL file format1.txt

```
1 1
2 4
3 9
4 16
5 25
6 36
7 49
8 64
9 81
10 100
```

Vsource PWL file format2.txt

```
1,1
2,4
3,9
4,16
5,25
6,36
7,49
8,64
9,81
10,100
```

Ã-Device

Ã-Device

- Ã-Device
  - Syntax

    Ãnnn VDD VSS OUT IN- IN+ MULT+ MULT- IN-- IN++ EN ¥ ¥ ¥ ¥ ¥ ¥ <TYPE> [INSTANCE PARAMETERS]

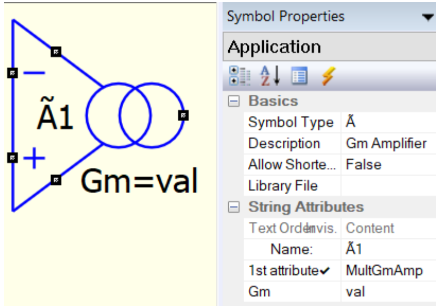
  - Ã-device models a highly configurable Gm block than can mimic the behavior of a complementary MOSFET output, there are two types MULTGMAMP and RROPAMP

Ã-Device Types

TYPE	Behavior
MULTGMAMP	Multiplying Gm Amplifier
RROPAMP	Rail-to-Rail Output OpAmp

To Identify what <TYPE> a symbol is

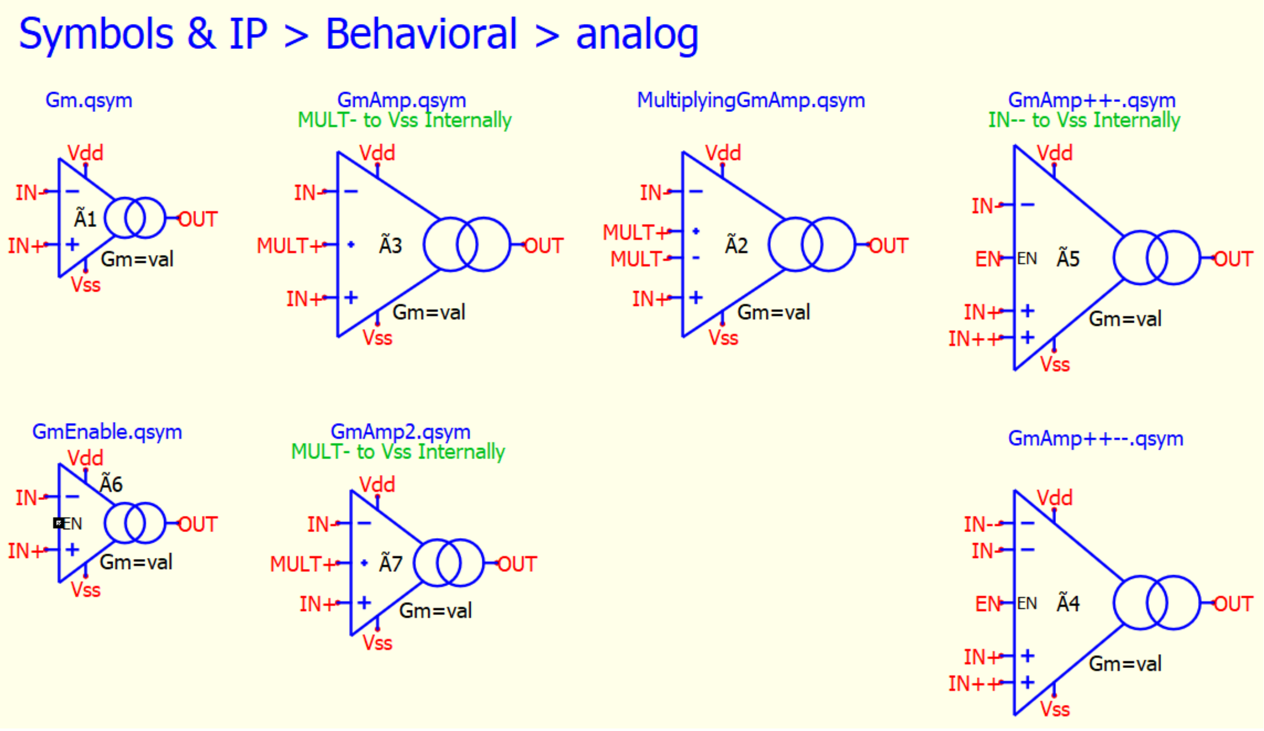
- In Symbol Properties > 1st attribute
- View > Netlist : from device syntax




```
* C:\Users\kelvinleung\Documents\QSPICE\Untitled.qsch
Ã1 ¥0 ¥1 ¥2 ¥3 ¥4 ¥ ¥ ¥ ¥ ¥ ¥ ¥ ¥ ¥ ¥ ¥ MultGmAmp Gm=val
.end
```

Ã-Device [MULTGMAMP]

- Ã-Device
  - Syntax: **Ãnnn VDD VSS OUT IN- IN+ MULT+ MULT- IN-- IN++ EN ¥ ¥ ¥ ¥ ¥ ¥ <TYPE> [INSTANCE PARAMETERS]**
  - Formula in Linear Region : Iout = GM * V(MULT+,MULT-) * V(MIN(IN+,IN++),MAX(IN-,IN--))



Ã-Device Instance Parameters in MULTGMAMP

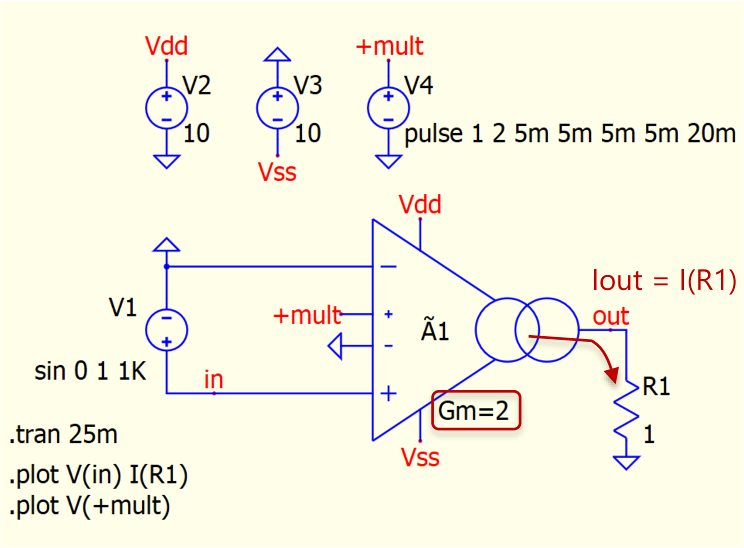
Ã-Device Instance Parameters

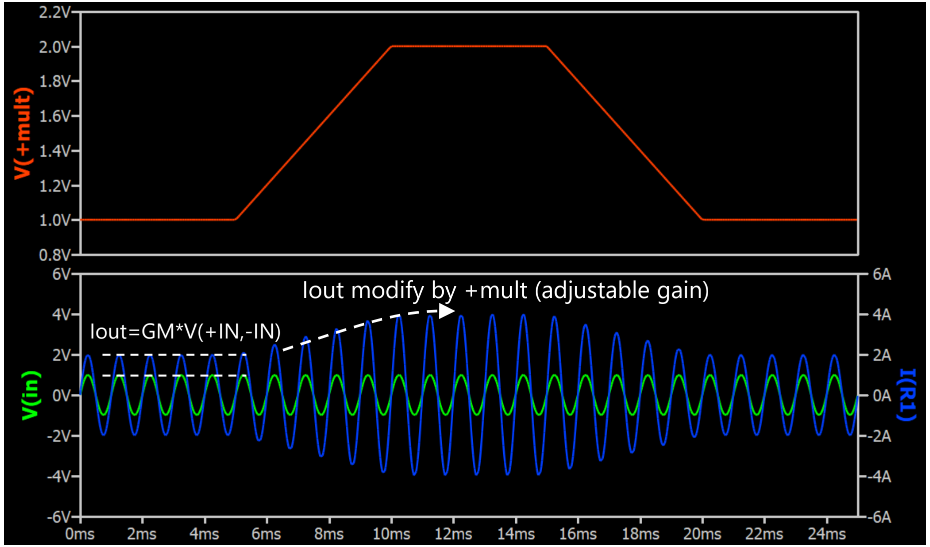
Name	Description
CAPINCM	Common eigenmode input capacitance
CAPINNM	Normal eigenmode input capacitance
CAPVDD	Capacitance from output to Vdd
CAPVSS	Capacitance from output to Vss
EN	Equivalent input voltage noise density
ENK	EN corner frequency
FT	3dB bandwidth of transconductance with no voltages slewing
GM	Ideal transconductance
IC	Initial condition of Vin × Vmult
IN	Equivalent input current noise density
INF	Common mode input current noise density proportional to frequency
INK	IN corner frequency
IOUT	Maximum sourcing current
ISNK	Maximum sinking current
ISNKKNEE	Sharpness of Maximum sinking current limit
ISRC	Maximum sourcing current
ISRCKNEE	Sharpness of max sourcing current limit
M	Number of parallel devices
REF	Logic threshold for enable(from Vss)
ROUT	Additional impedance added to output(2*R to Vdd, 2*R to Vss)
TEMP	Instance temperature
TTOL	Temporal tolerance for enable & UVLO
UVLO	Minimum supply voltage
VCROSS	Cross conduction voltage range
VDSAT	Voltage where gm starts to switch over to a resistance
VDSAT1	Voltage where gm starts to switch over to a resistance(top FET)
VDSAT2	Voltage where gm starts to switch over to a resistance(bottom FET)
VINHIGH	Output range measured from positive rail
VINHIGHKNEE	Sharpness of positive input range limit
VINLOW	Input range measured from negative rail
VINLOWKNEE	Sharpness of negative input range limit
VOS1	Offset voltage for input
VOS2	Offset voltage for multiplying input
VOUTMAX	Maximum output voltage measured from negative rail
VOUTMIN	Minimum output voltage measured from negative rail

MULTGMAMP : Ideal transconductance (GM)

Qspice : Multgmamp - Gm.qsch

- Gm : Ideal transconductance
  - Without IN++ and IN--, formula becomes Iout = **GM** * V(MULT+,MULT-) * V(IN+,IN-)
  - For ideal operation amplifier, GM is infinity
  - In Qspice, *Gm cannot be set to 0*

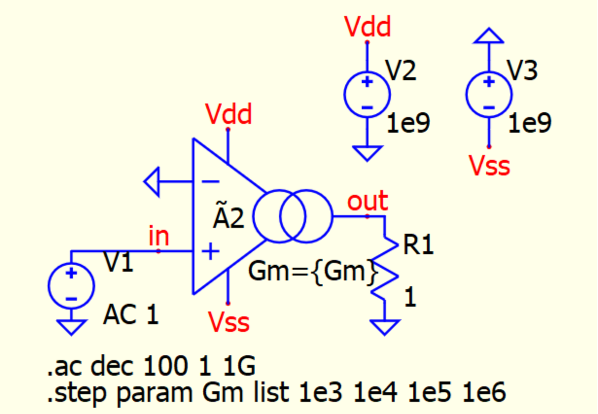


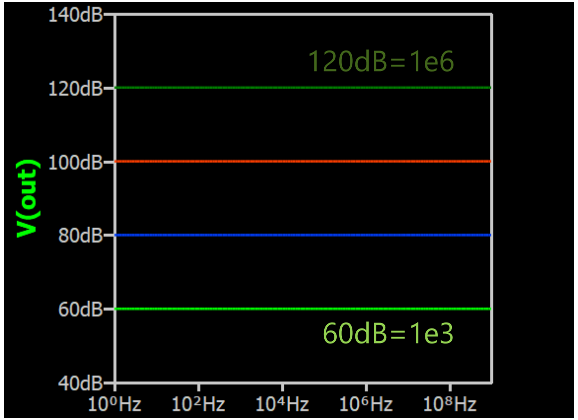


MULTGMAMP : Ideal transconductance (GM)

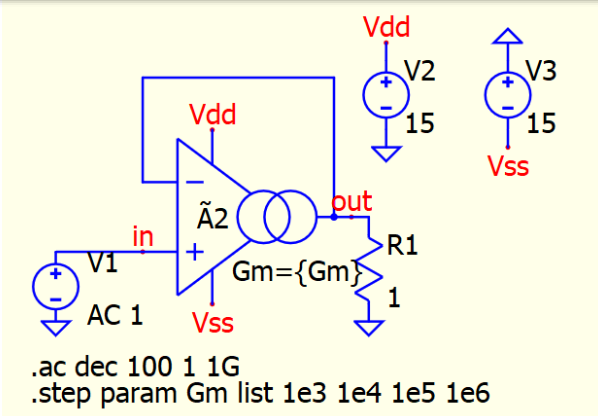
Qspice : Multgmamp - Gm freq response.qsch ; Multgmamp - Buffer.qsch

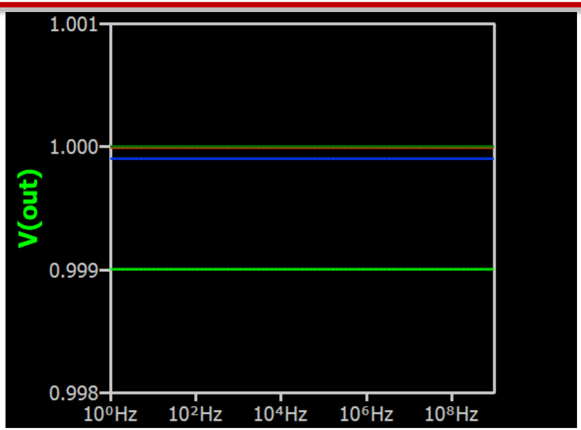
- Gm : Ideal transconductance
  - MULTGMAMP has ideal frequency response if without instance parameters
  - No default value of Gm, must define by user





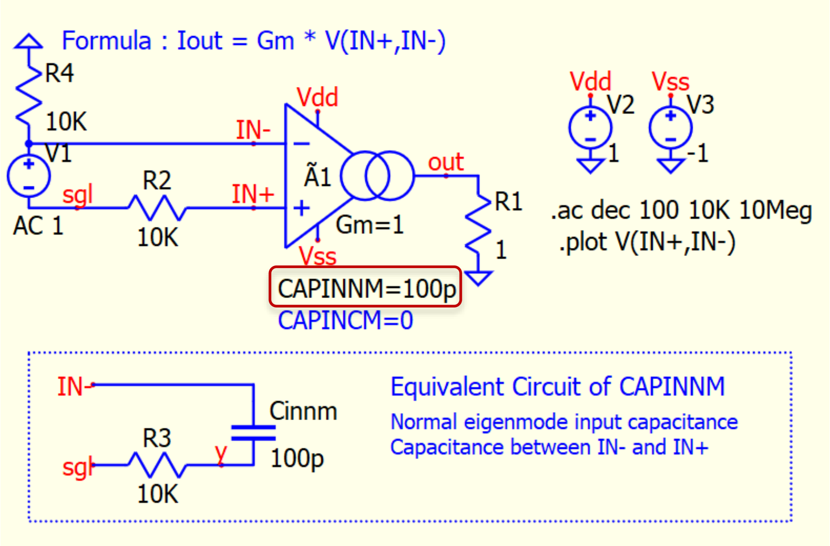
- Demo : Buffer Circuit
  - Demonstrate op-amp close loop ideal characteristic with different Gm value

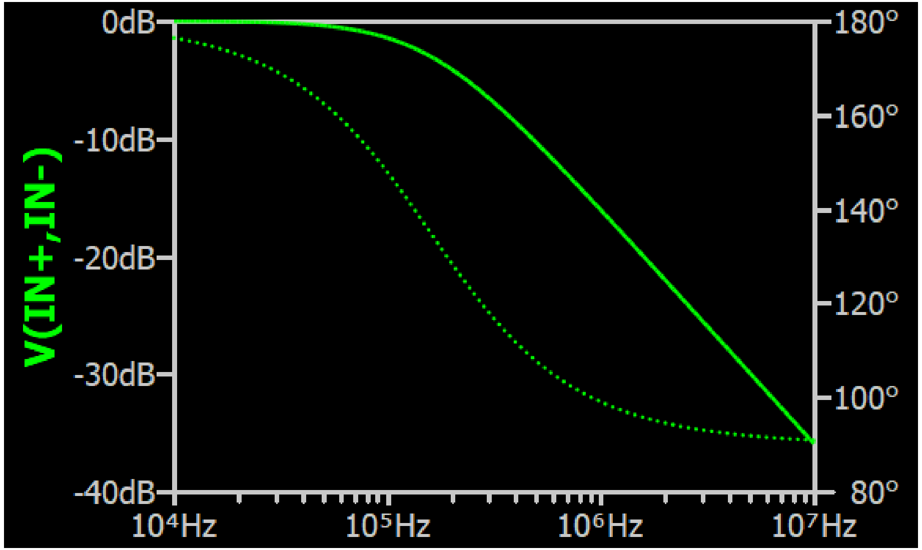




MULTGMAMP : Normal eigenmode input capacitance (CAPINNM)
Qspice : Multgmamp - Capinnm.qsch

- CAPINNM : Normal eigenmode input capacitance
  - **Default CAPINNM=0**
  - This capacitance is equivalent between IN- and IN+

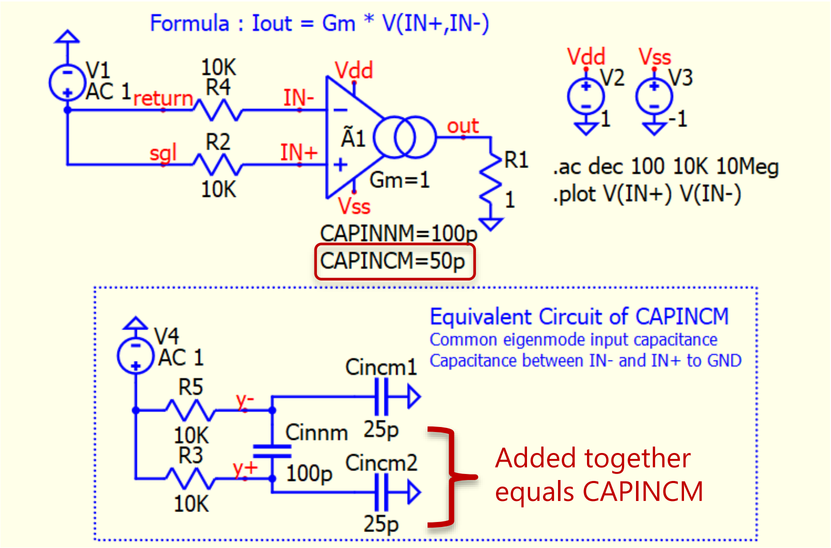


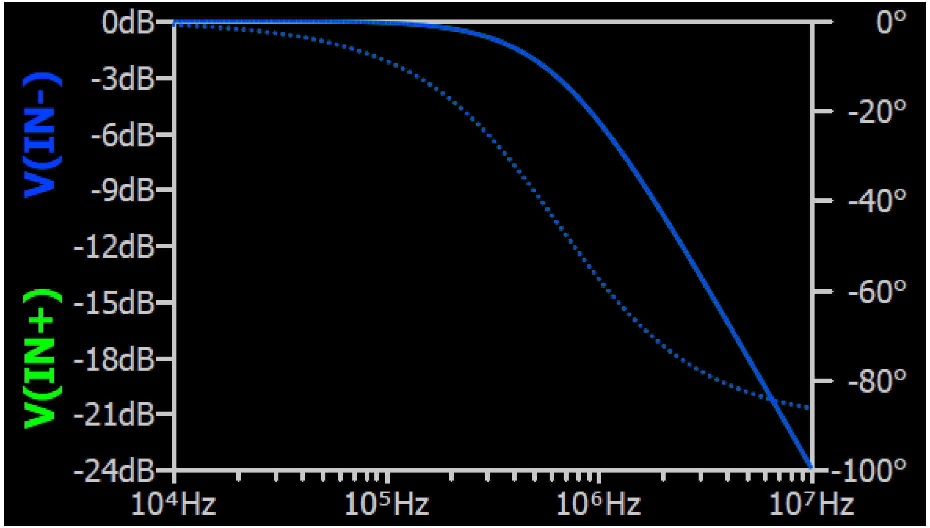


MULTGMAMP : Common eigenmode input capacitance (CAPINCM)

Qspice : Multgmamp - Capincm.qsch

- CAPINCM : Common eigenmode input capacitance
  - **Default CAPINCM=0**
  - This capacitance is between IN- to GND and IN+ to GND

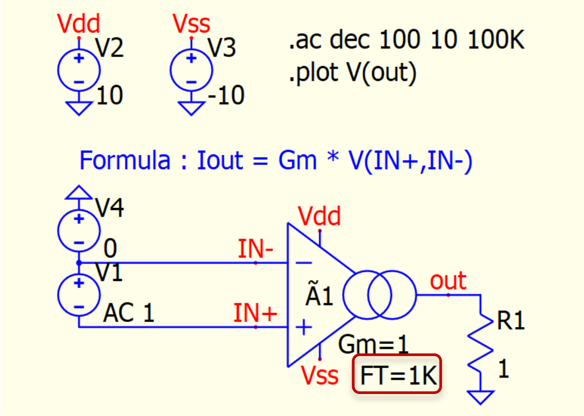


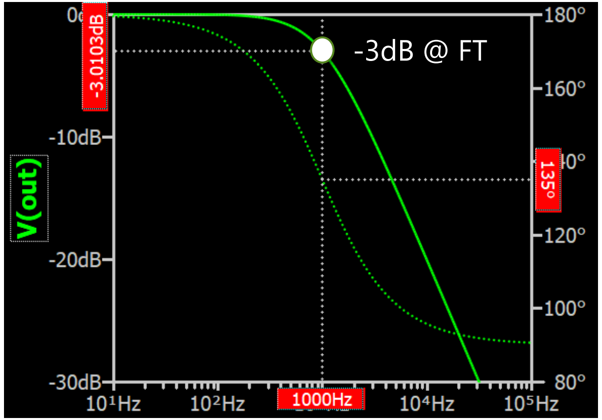


MULTGMAMP : FT 3dB Bandwidth

Qspice : Multgmamp - FT.qsch

- FT (3dB Bandwidth)
  - FT : 3dB bandwidth of transconductance with no voltages slewing
  - **Default FT=0** (i.e. infinite)

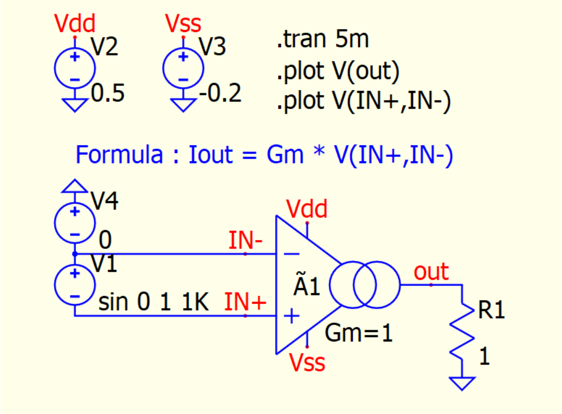


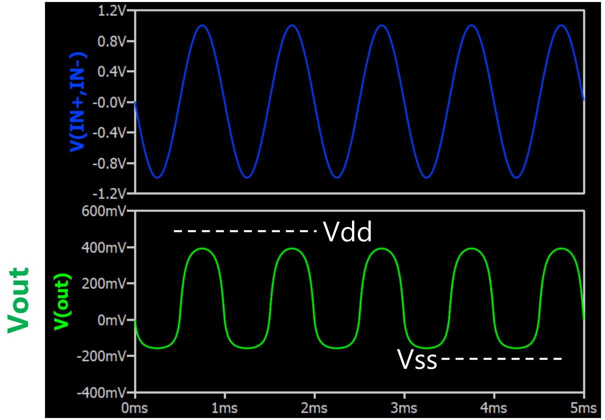


MULTGMAMP : Output Voltage Vdd, Vss and VDSAT

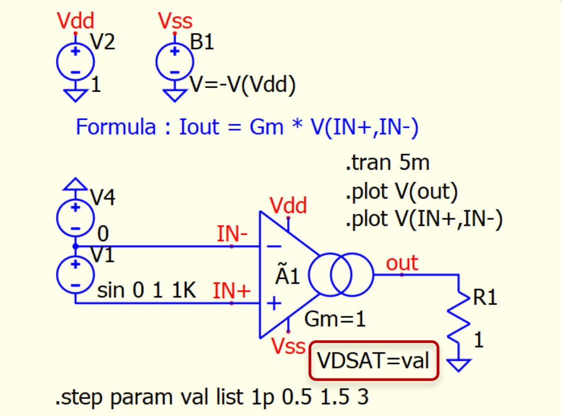
Qspice : Multgmamp - Vdd Vss.qsch ; Multgmamp - VDSAT.qsch

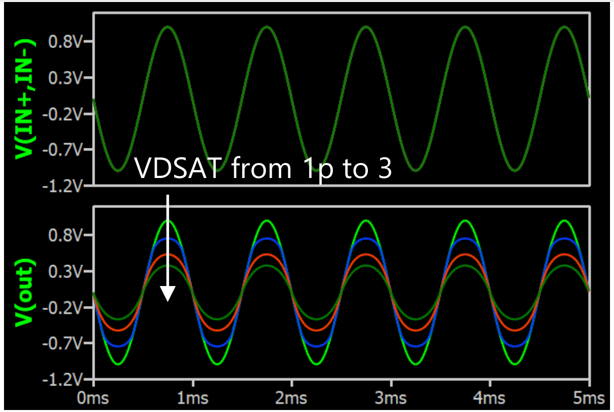
- Vdd and Vss Nets
  - This is not parameters but Net 1 and Net 2 in Ã-Device
  - Output voltage swing is limited by Vdd and Vss
  - ** In this example, Vout cannot reach Vdd and Vss because a default VDSAT is set





- VDSAT
  - Vdsat : Voltage where gm starts to switch over to a resistance
  - **Default VDSAT = 0.5**
  - **VDSAT=0** forced its to default
  - **VDSAT=1p** for no saturation

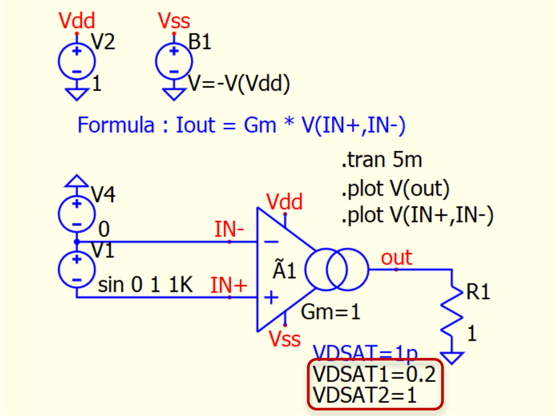


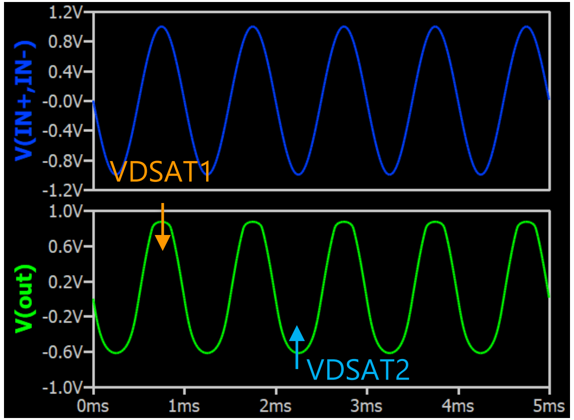


MULTGMAMP : Output Voltage VDSAT1, VDSAT2, VOUTMIN, VOUTMAX

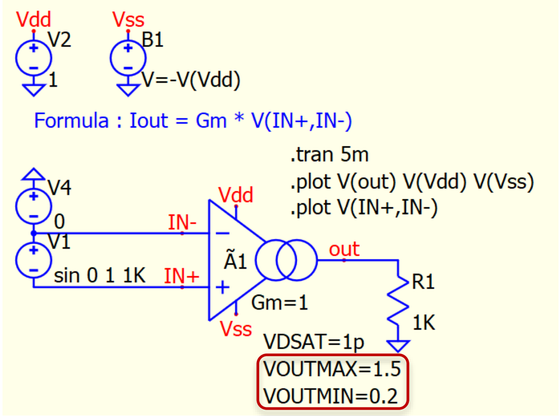
Qspice : Multgmamp - VDSAT1 VDSAT2.qsch ; Multgmamp - VOUTMAX VOUTMIN.qsch

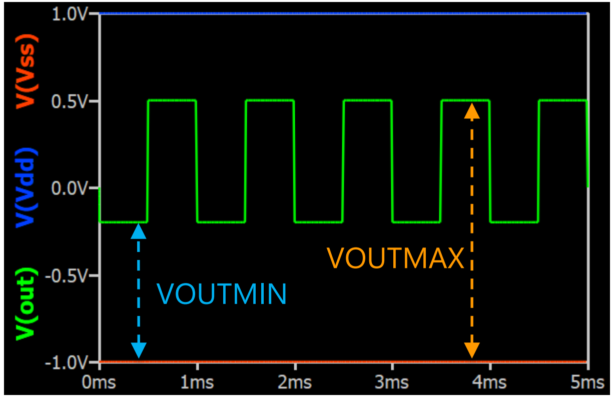
- VDSAT1 and VDSAT2
  - VDSAT1 : Voltage where gm starts to switch over to a resistance(top FET)
  - VDSAT2 : Voltage where gm starts to switch over to a resistance(bottom FET)
  - **Default VDSAT1=VDSAT**
  - **Default VDSAT2=VDSAT1**





- VOUTMIN and VOUTMAX
  - Voutmin : Minimum output voltage measured from negative rail
  - Voutmax : Maximum output voltage measured from negative rail

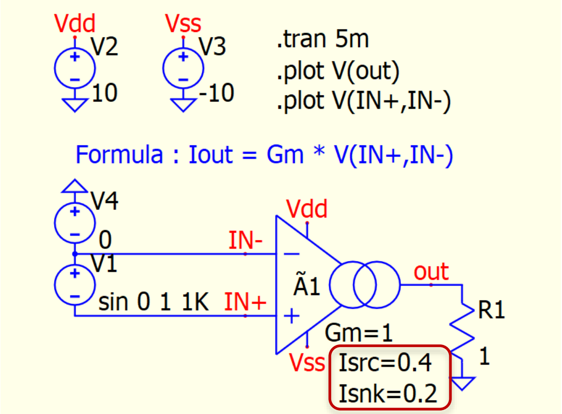


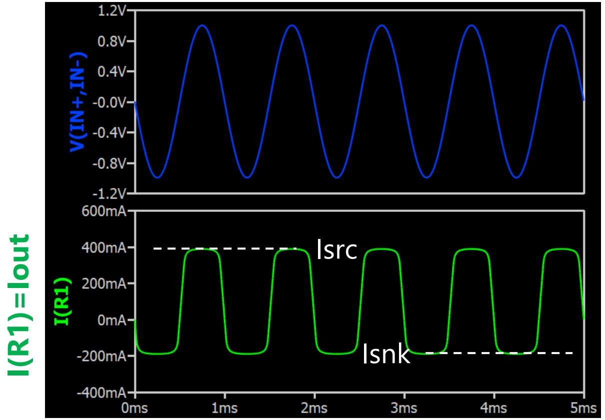


MULTGMAMP : Sink and Src Current (Iout / Isrc, Isnk)

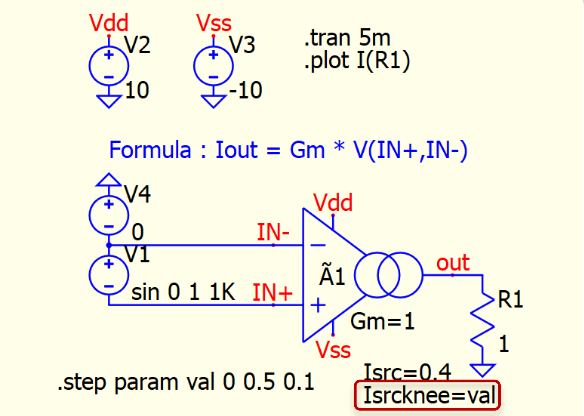
Qspice : Multgmamp - ISRC ISNK.qsch ; Multgmamp - ISRCKNEE ISNKKNEE.qsch

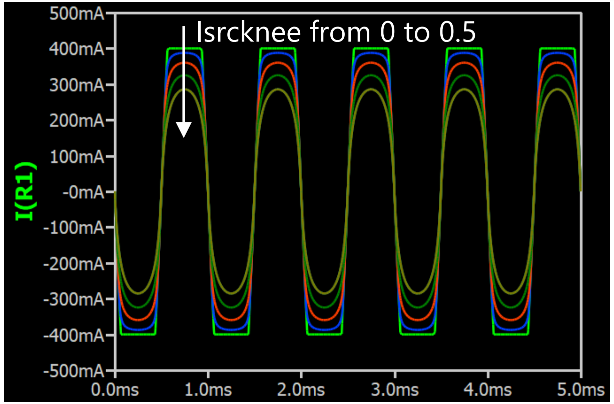
- IOUT/ISRC and ISNK
  - Iout/Isrc : Maximum sourcing current (toward load)
  - Isnk : Maximum sourcing current (toward device)
  - **Default ISRC = Infinite**
  - **Default ISNK = IOUT or ISRC**
    - i.e. if ISNK not specified, ISNK equals IOUT or ISRC





- ISRCKNEE and ISNKKNEE
  - Isrcknee : Sharpness of max sourcing current limit
  - Isnkknee : Sharpness of Maximum sinking current limit
  - **Default Isrckness = 0.1**
  - **Default Isnkkness = Isrcknee**



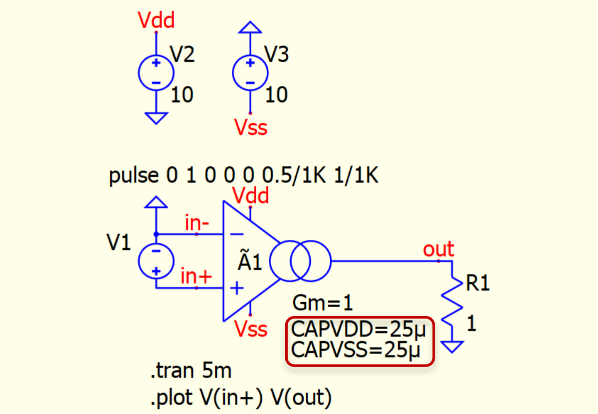


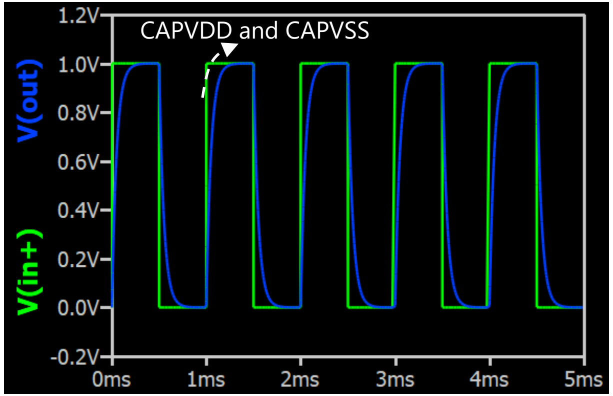
- Important Note
  - To have effect, must defines ISRC or ISNK

MULTGMAMP : Output Capacitance (CAPVDD, CAPVSS) and Resistance (Rout)

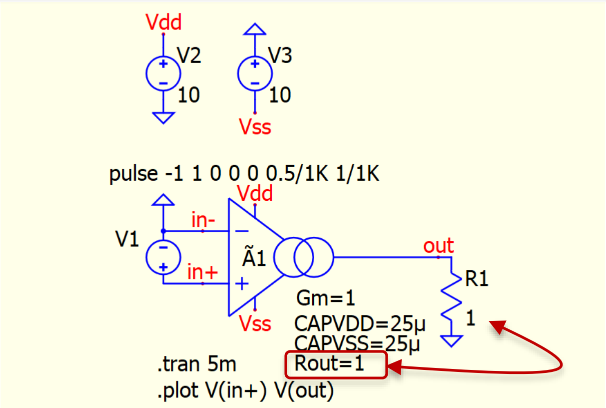
Qspice : Multgmamp - Capvdd Capvss.qsch ; Multgmamp - Rout.qsch

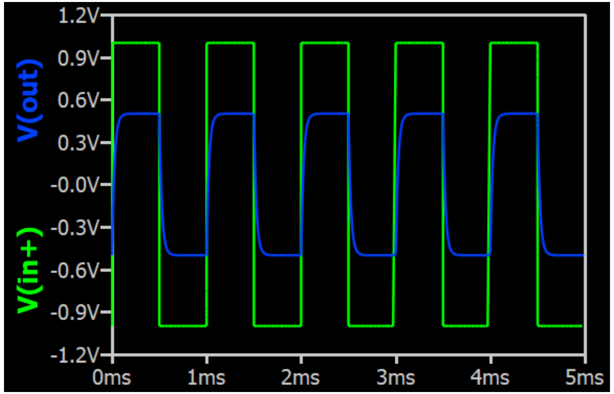
- CAPVDD and CAPVSS
  - CAPVDD : Capacitance from output to Vdd
  - Capvss : Capacitance from output to Vss





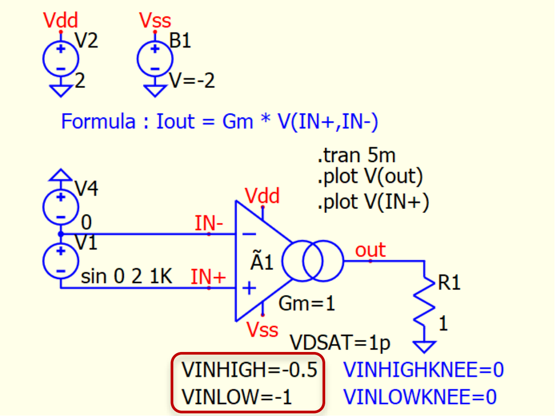
- ROUT
  - Rout : Additional impedance added to output(2*R to Vdd, 2*R to Vss)
  - In this example, Rout equal to amplifier loading, V(out) reduced by halve

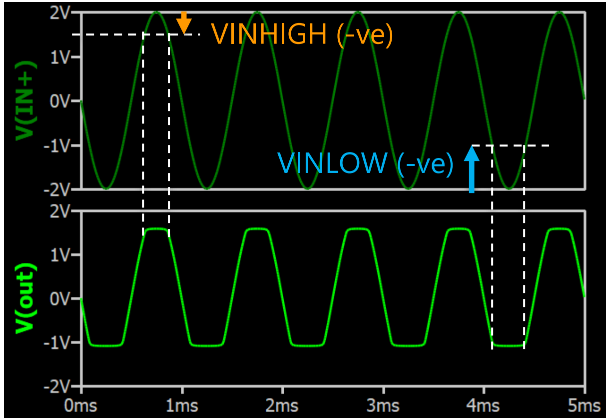




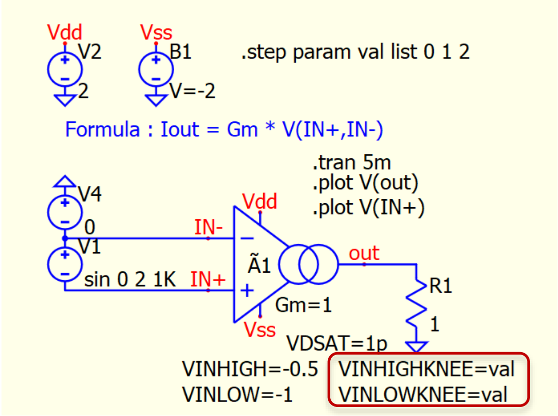
MULTGMAMP : Input Range VINLOW, VINHIGH, VINHIGHKNEE, VINLOWKNEE
Qspice : Multgmamp - VINHIGH VINLOW.qsch ; Multgmamp - VINHIGHKNEE VINLOWKNEE.qsch

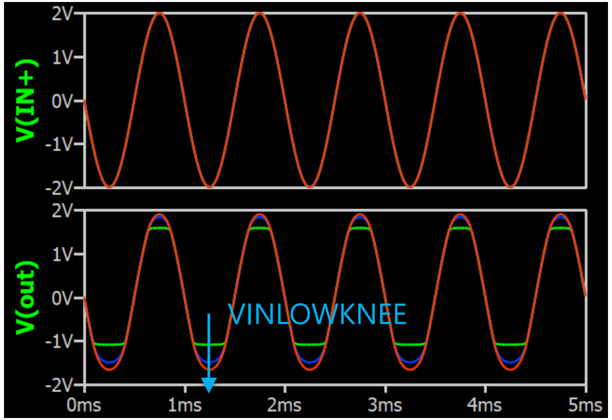
- VINLOW and VINHIGH
  - VINLOW : Input range measured from negative rail
  - VINHIGH : Input range measured from positive rail
  - **Default VINLOW=0**
  - **Default VINHIGH=0**
  - **Value is negative**, which limit input range. For example, VINHIGH=-0.5, Input HIGH is limited to Vdd+VINHIGH = 2-0.5=1.5 in this example





- VINLOWKNEE VINHIGHKNEE
  - Vinlowknee : Sharpness of negative input range limit
  - Vinhighknee : Sharpness of positive input range limit
  - **Default VINHIGHKNEE=0**
  - **Default VINLOWKNEE=0**
  - Increase KNEE soften the sharpness of input range, more output signal to come

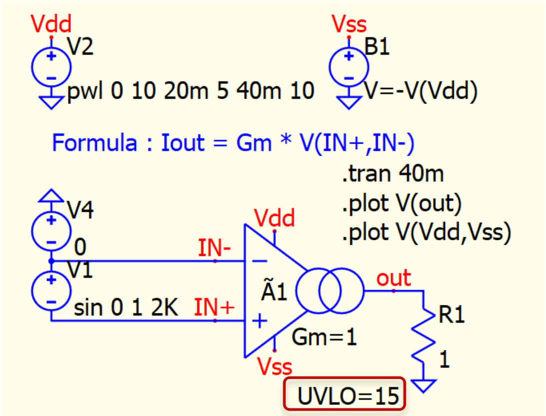


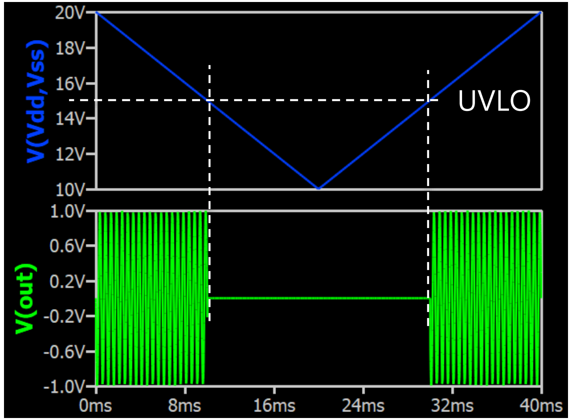


MULTGMAMP : UVLO and VOS1

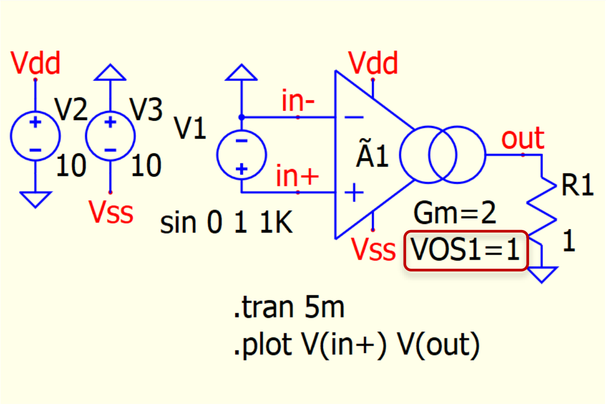
Qspice : Multgmamp - UVLO.qsch ; Multgmamp - VOS1.qsch

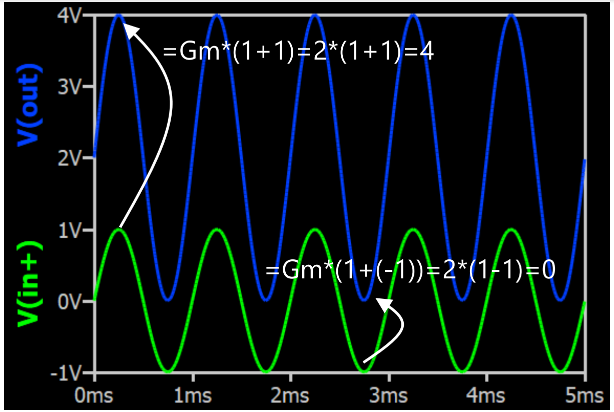
- UVLO
  - UVLO : Under Voltage Lock Out - Minimum supply voltage
  - Default UVLO is Infinite
  - UVLO is compare to supply voltage = Vdd-Vss





- VOS1
  - VOS1 : Offset voltage for input
  - Iout = GM * (*VOS1*+V(IN+,IN-))
    - This parameter is not in HELP formula, but it actually implemented
  - Default VOS1 = 0





¥-Device

¥-Device

- ¥-Device
  - Syntax:

    ¥nnn N1 N2 N3 N4 N5 N6 N7 N8 N9 N10 N11 N12 N13 N14 N15 N16 <TYPE> [INSTANCE PARAMETERS]

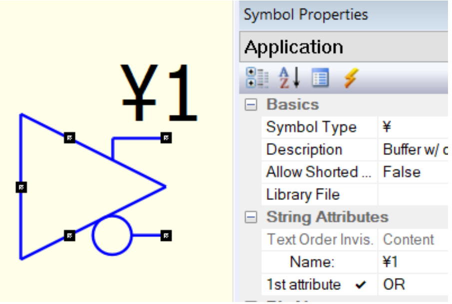
  - The ¥-device supplies gate, flop, and a few other types of functional behaviors. The device expects exactly 16 pins, but not all are used. Unused pins must be specified connected to "¥".

¥-Device Types

TYPE	Behavior
AND	AND gate
CLOCKSYNC	Selects between a Sync and Clock inputs
D-FLOP	D-type flip-flop
EXTOSC	Oscillator programmed with an external resistor
HMITT	Schmitt trigger
JK-FLOP	JK-type flip-flop
MONOSTABLE	Retriggerable monostable
OR	OR gate
PS-FLOP	SMPS flip-flop
RS-FLOP	RS-type flip-flop
T-FLOP	Toggle flip-flop
XOR	XOR gate
Φ-DET	Phase/Frequency detector

To Identify what <TYPE> a symbol is

- In Symbol Properties > 1st attribute
- View > Netlist : from device syntax

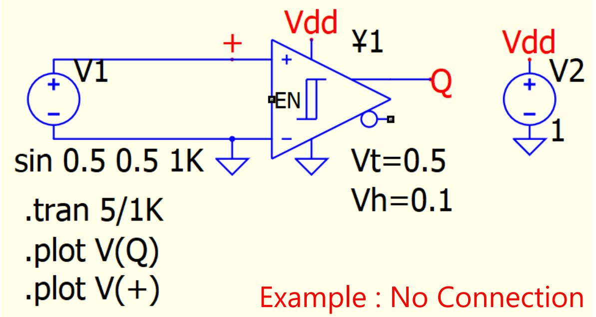


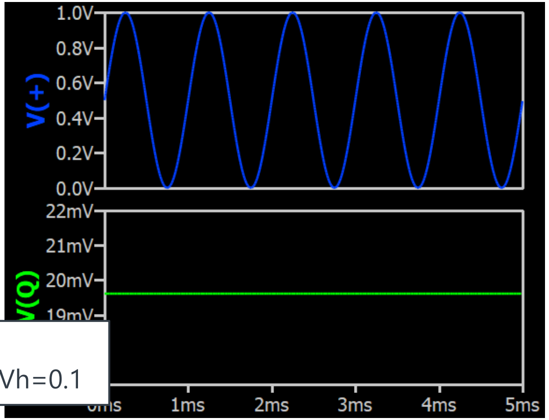

```
* C:\Users\kelvinleung\Documents\QSPICE\Unt
¥1 ¥0 ¥1 ¥2 ¥3 ¥4 ¥ ¥ ¥ ¥ ¥ ¥ ¥ ¥ ¥ ¥ ¥ OR
.end
```

¥-Device : How EN pin works

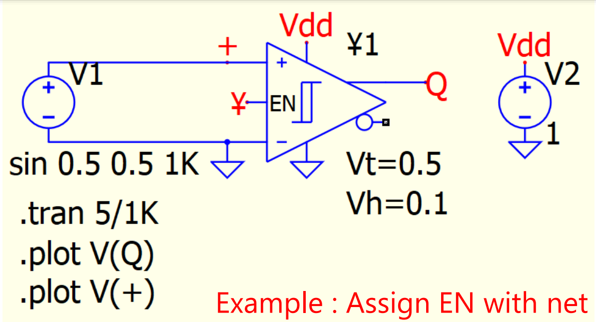
Qspice - Logic - EN.qsch

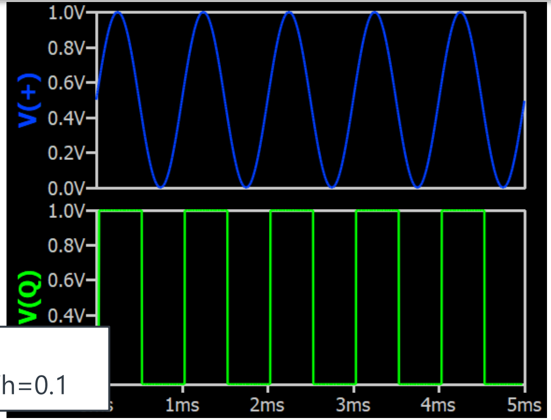
- How EN works
  - If EN is preset in symbol, normally, a signal is used to control its status. Here discuss two situations
  - #1 No connect to EN pin
    - Netlist assign ¥n as net name. EN pin is active to monitor EN signal. In this case, no output will generate
  - #2 Assign EN pin with net ¥
    - ¥ net name is equivalent to unassigned in ¥-device
    - Unassigned EN pin will be considered as Default ENABLE
    - Therefore, a symbol can be created with pin assigned to ¥ for their default





Netlist
¥1 Vdd 0 Q ¥0 + 0 ¥1 ¥ ¥ ¥ ¥ ¥ ¥ ¥ ¥ ¥ HMITT Vt=0.5 Vh=0.1





Netlist
¥1 Vdd 0 Q ¥0 + 0 ¥ ¥ ¥ ¥ ¥ ¥ ¥ ¥ ¥ ¥ HMITT Vt=0.5 Vh=0.1

Common Instance Parameters (example from AND Gate Instance Param)

Name	Description	Units	Default
CAPVDD	Capacitance from an output to Vdd	F	0.
CAPVSS	Capacitance from an output to Vss	F	0.
IC	Initial condition(needed, e.g., for a ring osc)		
M	Number of parallel devices		1.
REF	Logic reference voltage	V	(Vdd + Vss) ÷ 2
RSINK	Resistance to Vss when output high	Ω	RSRC
RSRC	Resistance to Vdd when output low(aka ROUT)	Ω	100.
TD	Delay(aka TD1)	s	0.
TD2	Asymmetrical delay	s	TD
TEMP	Instance temperature	°C	27.
TFALL	Fall time	s	0.
TRISE	Rise time	s	0.
TTOL	Temporal tolerance	s	1µs
UVLO	Minimum Vdd-Vss voltage to operate	V	0.
ZMULT	Impedance multiplier when biased half way		1.

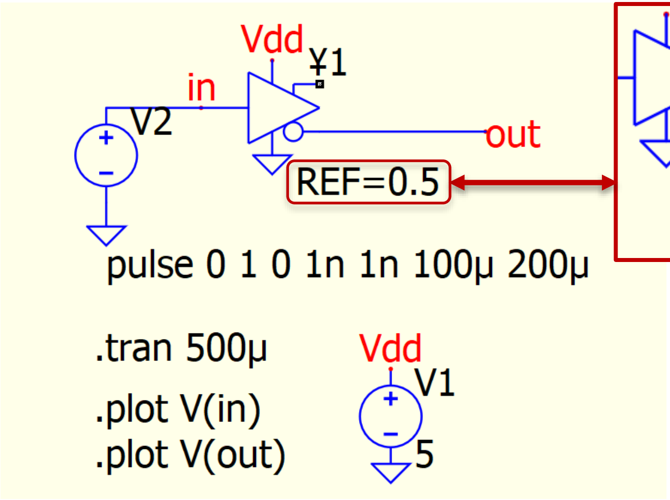
¥ Instance Params : REF Logic Reference Voltage

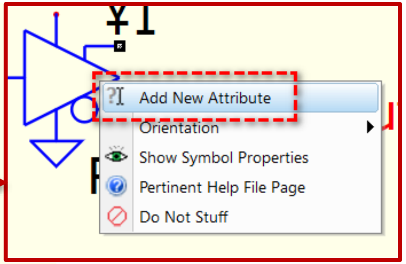
Qspice : Logic - REF.qsch

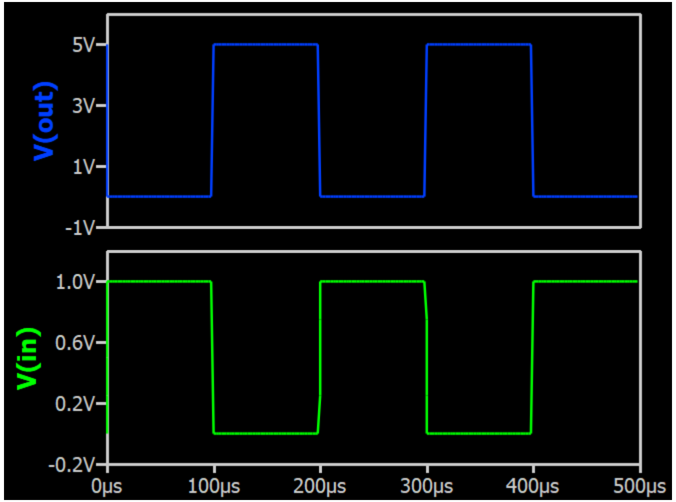
- REF : Logic reference voltage
  - In default, ¥-Device logic threshold is $\frac{\text{Vdd+Vss}}{2}$

REF	Logic reference voltage	V	(Vdd + Vss) ÷ 2

  - User can change logic threshold by [right click device] > [Add New Attribute] to add REF=<value>
    - This example show logic output follows Vdd/0 with logic input threshold equal 0.5V to interface with 1V input logic



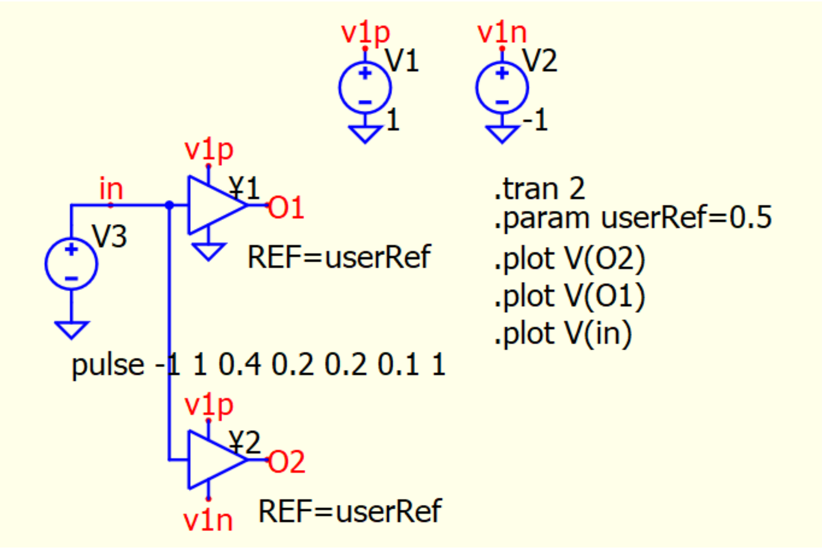


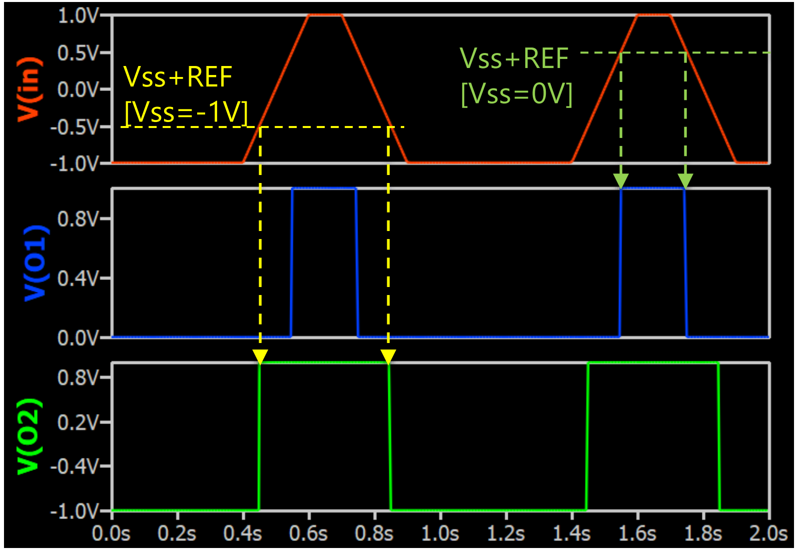


¥ Instance Params : REF Logic Reference Voltage

Qspice : Logic - REF (Dual Supply).qsch

- REF : Logic Reference Voltage
  - REF is not absolute voltage to node 0, but reference to Vss node of ¥-Device
  - In this example, ¥1 and ¥2 are with same REF value, but as ¥1 Vss=0V and ¥2 Vss=-1V, their logic reference is different reference to node 0 (GND). Therefore, even their input is same, their output can be different

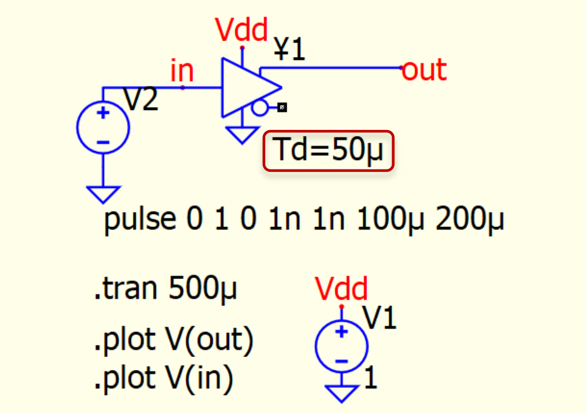


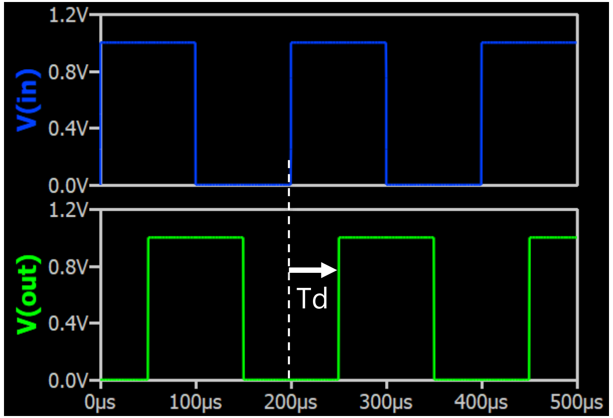


¥ Instance Params : Delay (TD) and Asymmetrical Delay (TD2)

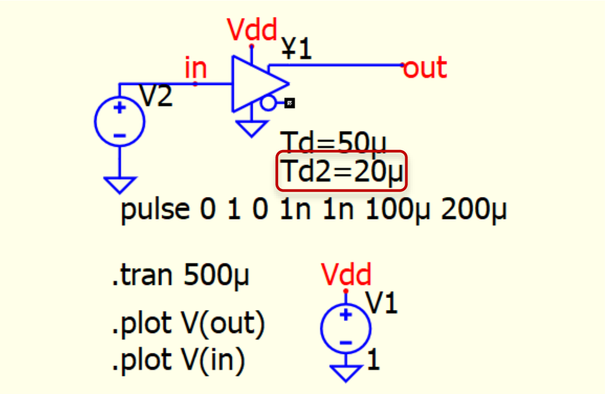
Qspice : Logic - Td.qsch ; Logic - Td Td2.qsch

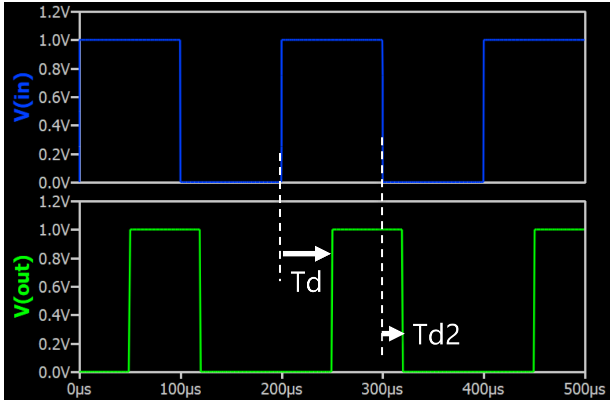
- TD (Delay)
  - Default is 0s
  - ** If TD2 is not set, both rising and falling delay times are same
  - ** If TD > logic H duration or delay TD2 > logic L duration, output always LOW or HIGH





- TD2 (Asymmetrical delay)
  - Default set equal to TD
  - If different delay times for rising and falling edge, set TD2 for falling edge delay time (i.e. TD only control rising edge delay time)

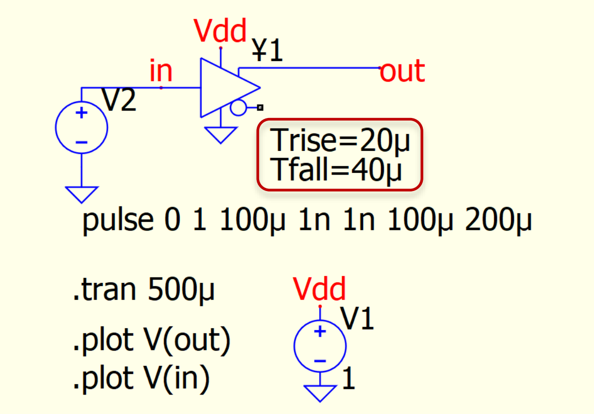


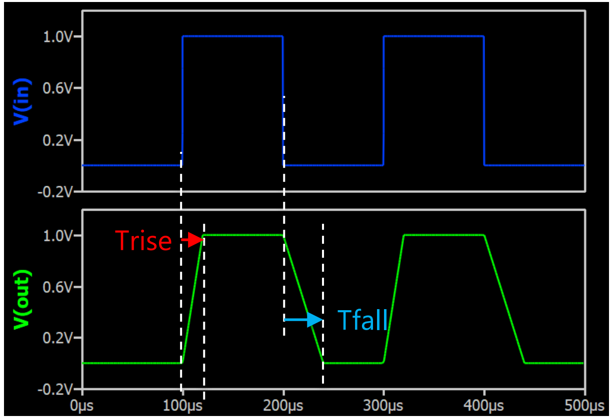


¥ Instance Params : Rise time (Trise), Fail time (Tfall) and UVLO

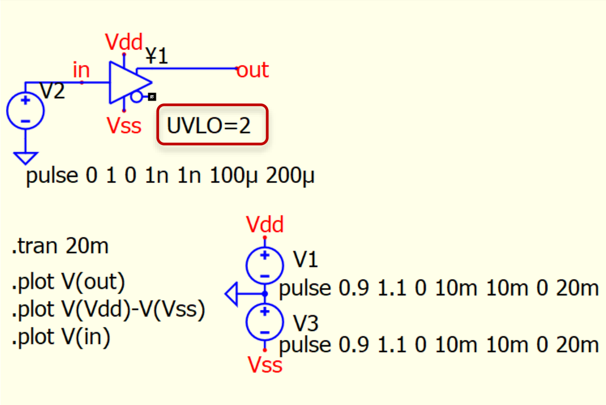
Qspice : Logic - Trise Tfall.qsch

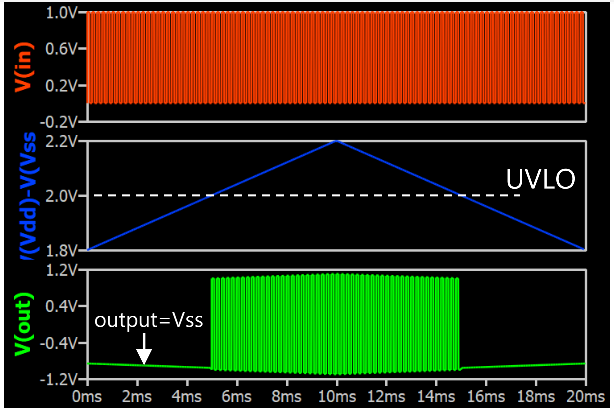
- TRISE and TFALL
  - Trise : Rise time
  - Tfall : Fall time





- UVLO
  - Under Voltage Lock Out UVLO
  - UVLO : Minimum Vdd-Vss voltage to operate
    - Output only enabled when Vdd-Vss > UVLO
    - Output equals Vss when gate disable

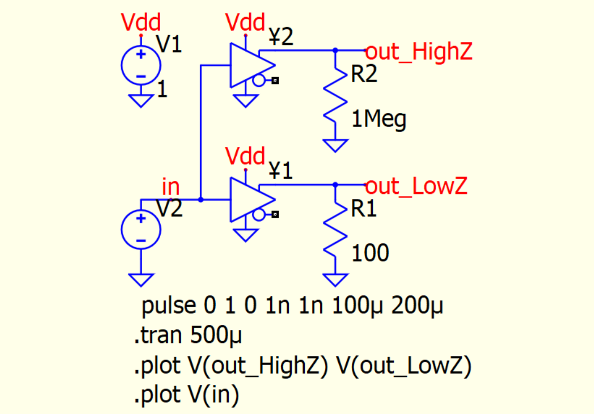


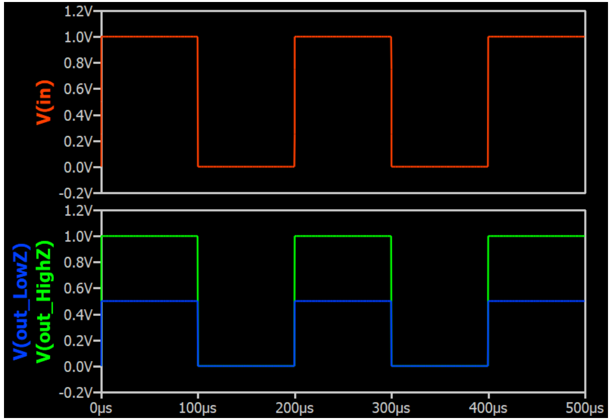


¥ Instance Params : Output R and C (Rsink, Rsrc, Capvdd, CapVss)

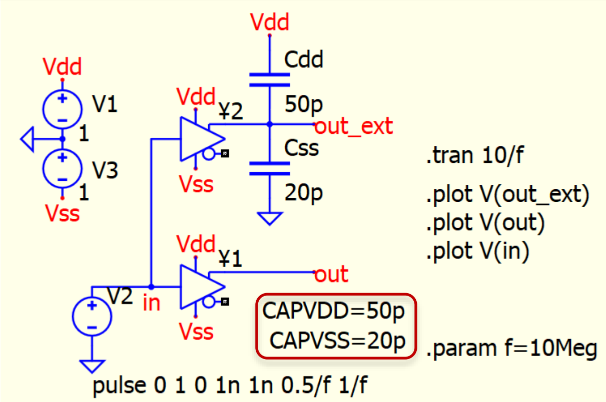
Qspice : Logic - RSINK RSRC.qsch ; Logic - Capvdd Capvss.qsch

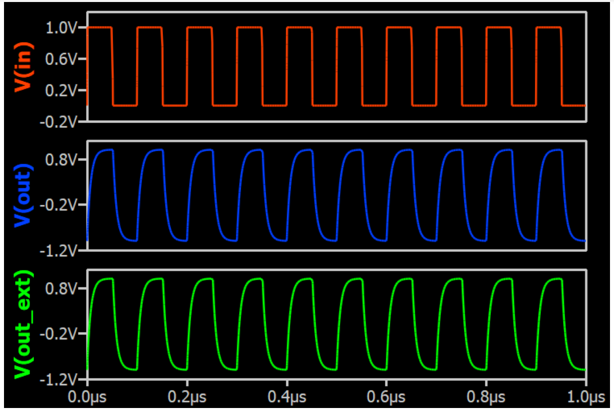
- RSINK and RSRC
  - RSINK : Res to Vss when o/p high
  - RSRC : Res to Vdd when o/p low
  - **Default RSINK=100Ω**
  - **Default RSRC=100Ω**
- Example
  - This simulation shows loading effect when output to a 100 ohms, where o/p level is reduced to half of Vdd





- CAPVDD, CAPVSS
  - Capvdd : Capacitance from an output to Vdd
  - Capvss : Capacitance from an output to Vss
- Explanation
  - Capacitance Capvdd/Capvss equivalent Cdd/Css this example
  - This demo can have frequency response because Rsink=Rsrc=100 internally

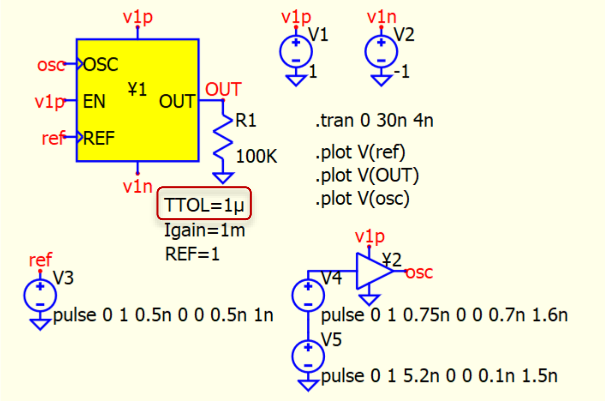


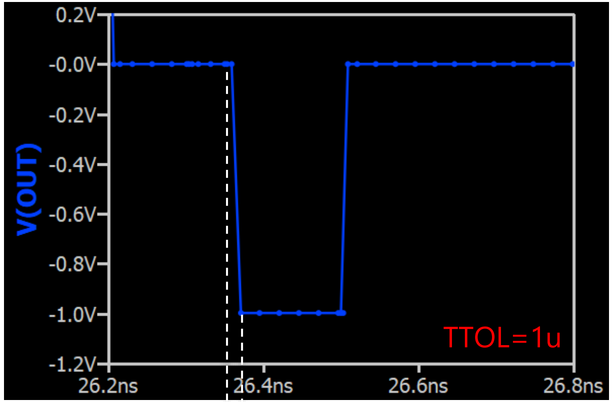


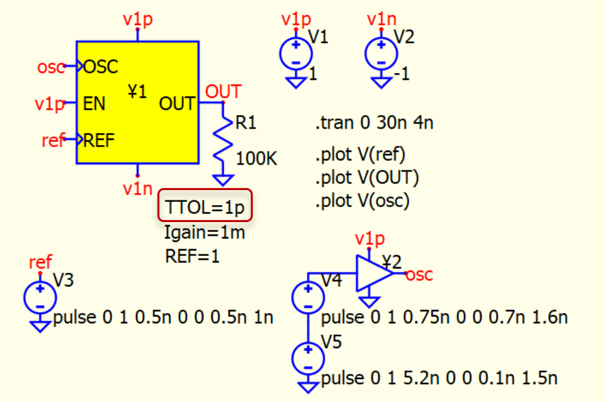
¥ Instance Params : TTOL Temporal Tolerance

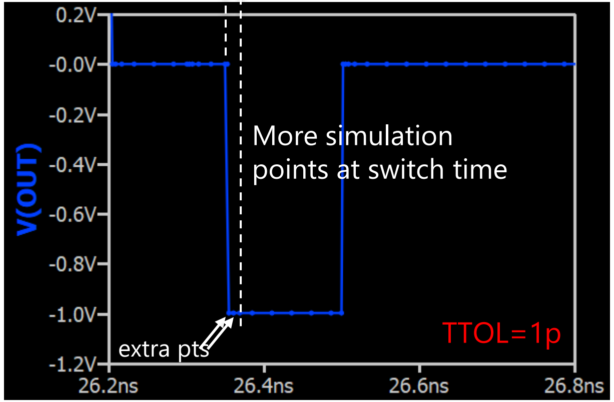
Qspice : Logic - TTOL.qsch

- TTOL
  - Ttol : Temporal tolerance
  - **Default TTOL=1u**
  - TTOL allows one to determine how accurately the switch time should be found





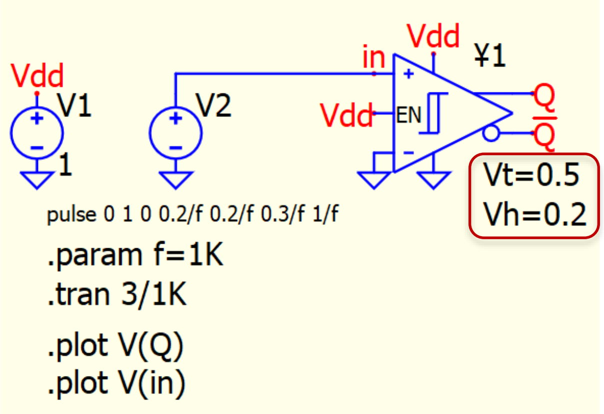


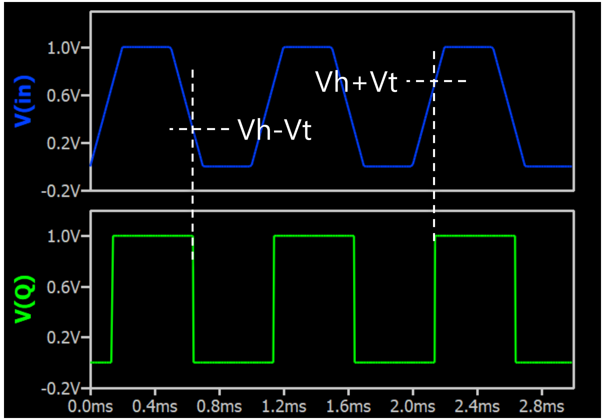


¥ [HMITT] Instance Params : Threshold (VT) and Half Hysteresis (VH)

Qspice : HMITT - Vt Vh.qsch

- VT and VH
  - Vt : Threshold voltage
  - Vh : Half hysteresis voltage
  - HMITT is schmitt trigger logic input
  - low trip point is Vt-Vh and the high trippoint is Vt+Vh





¥ Truth Table : AND, OR, XOR

Qspice : Truth Table of AND OR XOR.qsch

- AND

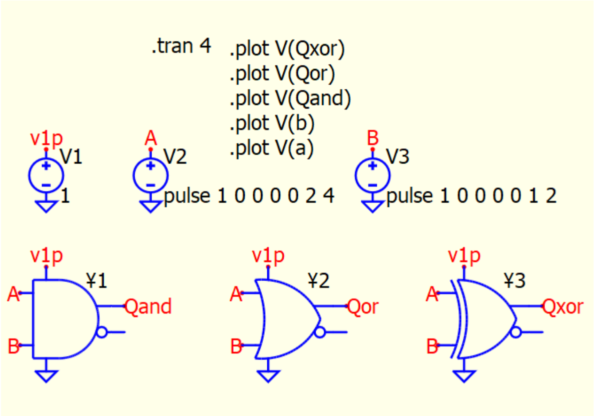
¥-Device AND			
A	**B**	**Q**	**_Q**
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

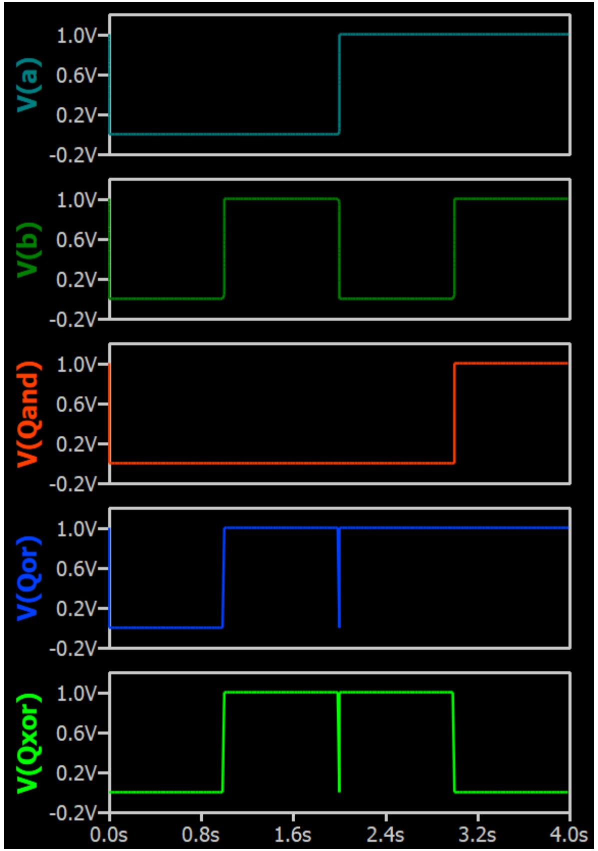
- OR

¥-Device OR			
A	**B**	**Q**	**_Q**
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

- XOR

¥-Device XOR			
A	**B**	**Q**	**_Q**
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1



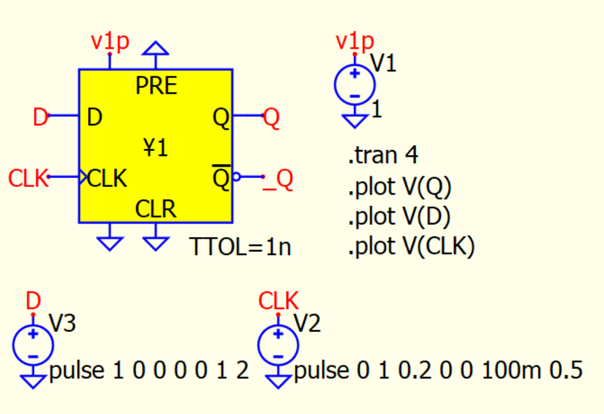


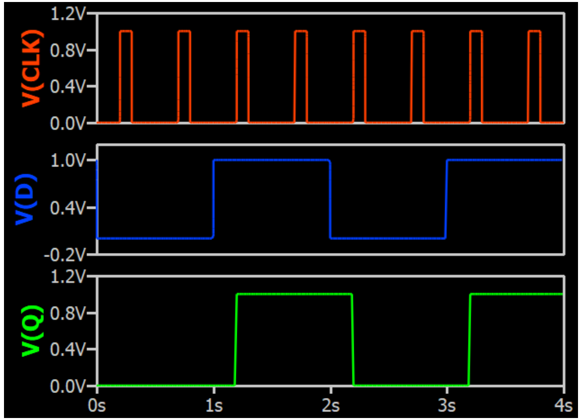
¥ Truth Table : D-FLOP and T-FLOP

Qspice : Truth Table of D-FLOP.qsch ; Truth Table of T-FLOP.qsch

- D-FLOP
  - PRE : Active High (=SET)
  - CLR : Active High (=RESET)

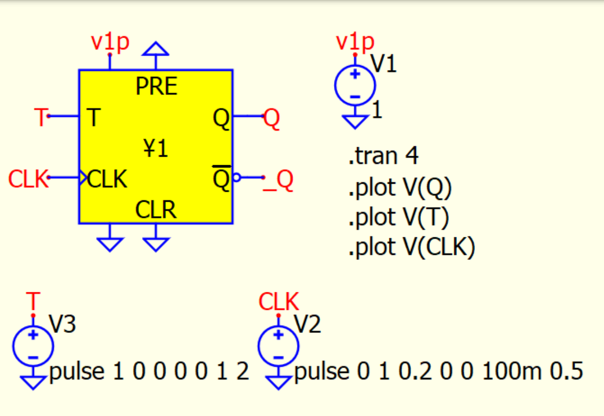
¥-Device D-flop					
CLK	**D**	**PRE**	**CLR**	**Q**	**_Q**
↑	0	0	0	0	1
↑	1	0	0	1	0
x	x	0	0	Q	_Q
x	x	1	0	1	0
x	x	x	1	0	1

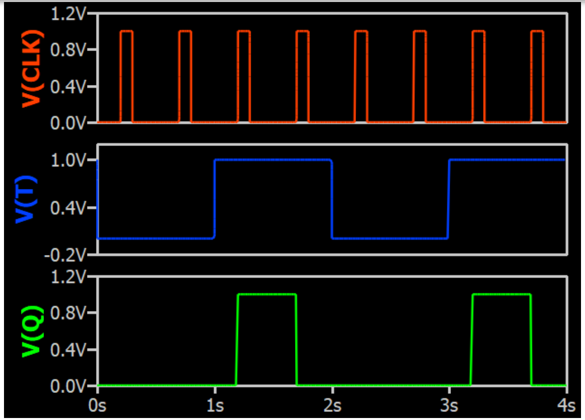




- T-FLOP

¥-Device T-flop				
CLK	**T**	**PRE**	**CLR**	**Qn+1**
↑	0	0	0	0
↑	1	0	0	_Qn
x	x	0	0	Q
x	x	1	0	1
x	x	x	1	0



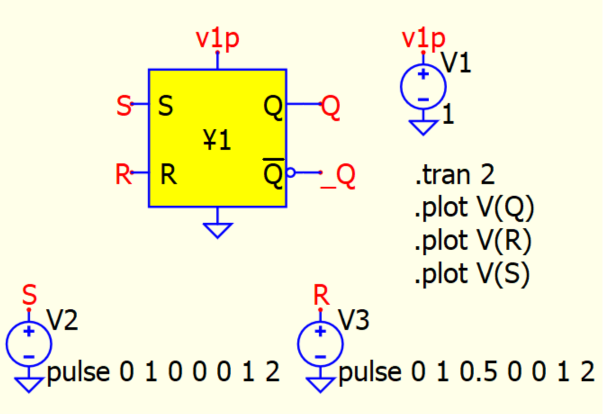


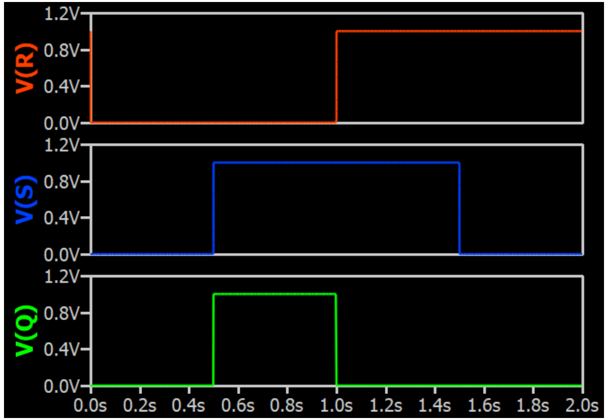
¥ Truth Table : SR-FLOP and JK-FLOP

Qspice : Truth Table of SR-FLOP.qsch ; Truth Table of JK-FLOP.qsch

- SR-FLOP

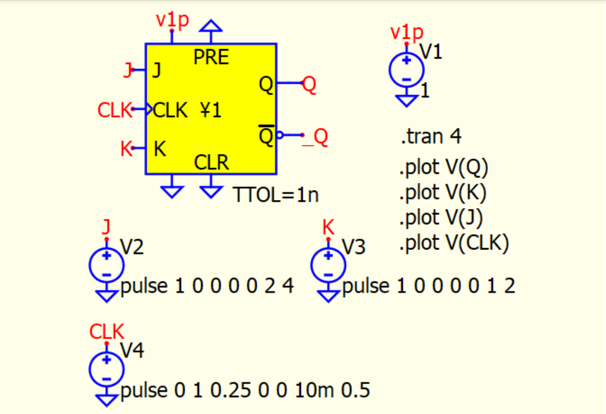
¥-Device SR-flop			
R	S	Q	_Q
0	0	0	1
0	1	1	0
1	x	0	1

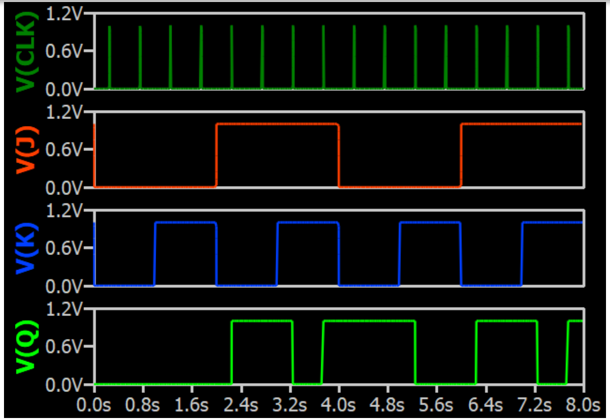




- JK-FLOP

¥-Device JK-flop					
CLK	J	K	PRE	CLR	Qn+1
↑	0	0	0	0	Qn
↑	0	1	0	0	0
↑	1	0	0	0	1
↑	1	1	0	0	_Qn
x	x	x	0	0	Q
x	x	x	1	0	1
x	x	x	x	1	0

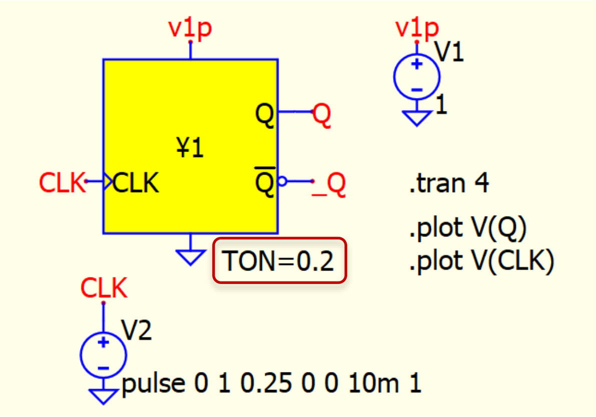


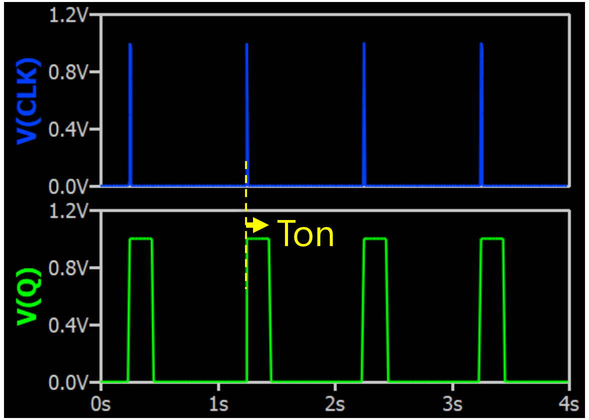


¥-Device Monostable

Qspice : Usage - Monostable.qsch

- Monostable
  - TON must be specified to use Monostable
  - CLK trigger a minimum on-time pulse





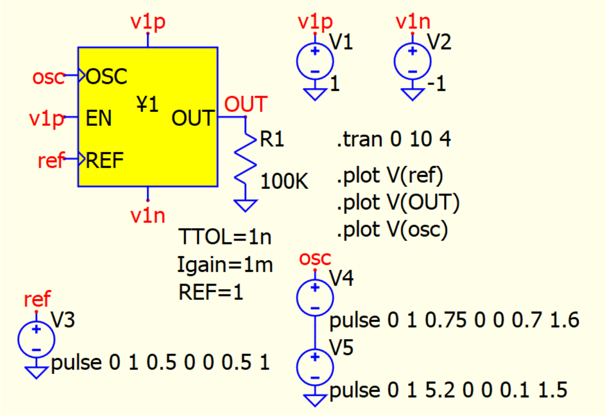
¥ Truth Table : Φ-DET (Phi-Det) [Symbol : PhaseDetector in analog]

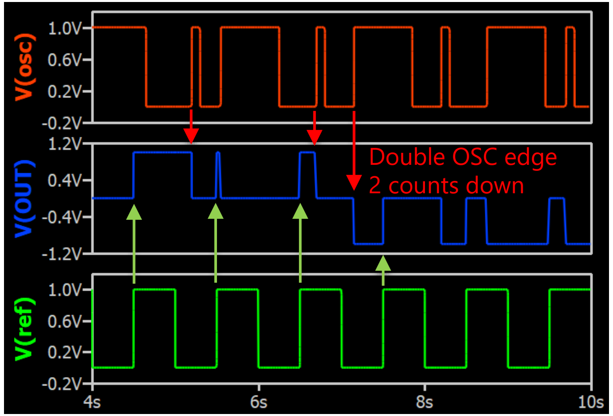
Qspice : Truth Table of Phi-Det.qsch

- Φ-DET (Phi-Det)
  - Phase/Frequency Detector

¥-Device Phi-Det		
REF	**OSC**	**OUT**
↑	x	Up
x	↑	Down
↑	↑	Unchange

- Important
  - Output is current, not voltage
    - Suggest to set a higher Igain for OUT can reach Vdd/Vss with load (Default Igain only 10uA)
  - This device is a [Vdd, 0, Vss] 3-state counter, therefore, must operate with dual supply
    - REF edge counts up
    - OSC edge counts down

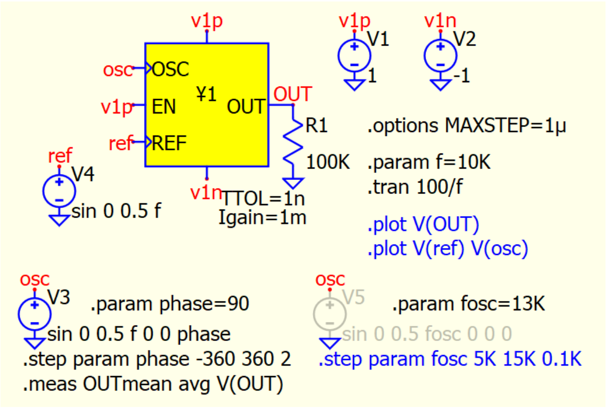


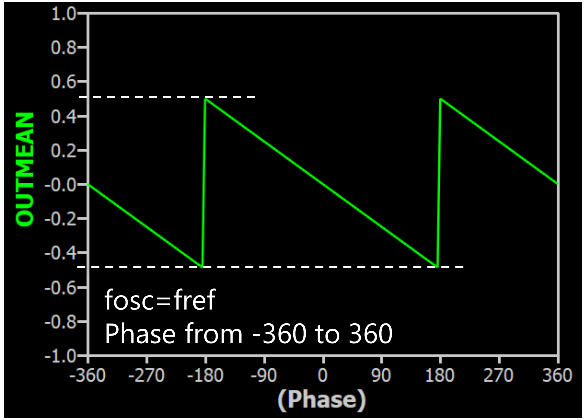


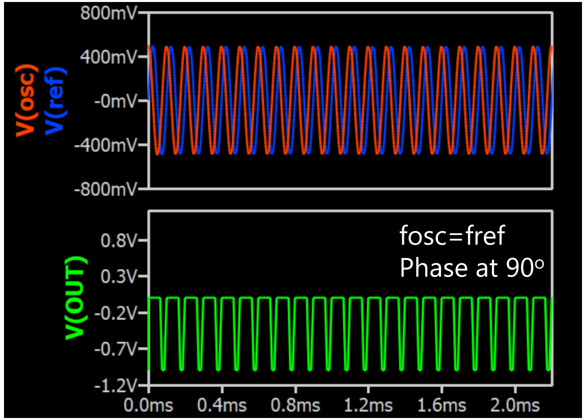
- Phase/Frequency Detection
  - Next slide is simulation results in phase change and frequency change
  - Mean of PWM output pattern can differentiate it is OSC signal phase or frequency deviate from REF signal
  - This is a key component in Phase Lock Loop (PLL)

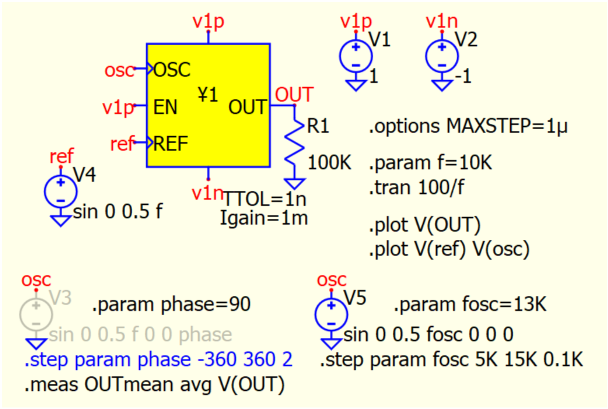
¥-Device Φ-DET (Phi-Det) : OSC and REF Relationship with OUT

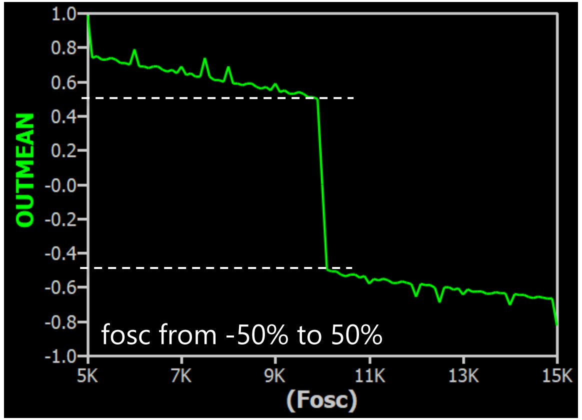
Qspice : Usage - Phi-Det (Freq and Phase).qsch

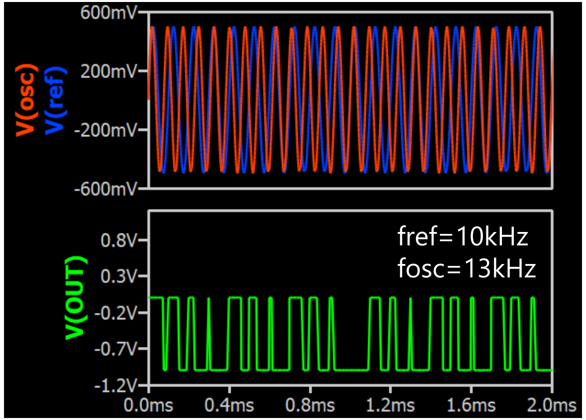










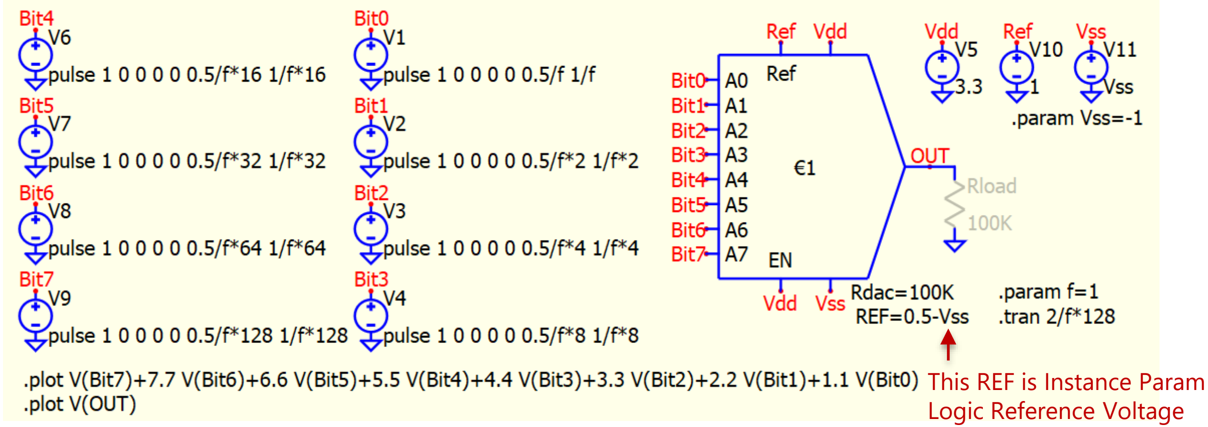


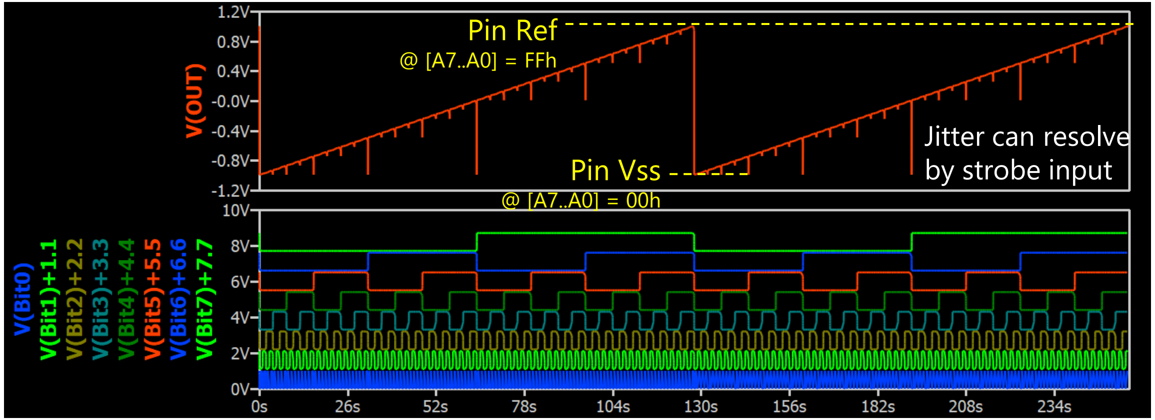
€-Device

€-Device DAC : Build-in Symbol DAC8.qsym

Qspice : DAC - Basic.qsch

- DAC
  - DAC : Digital to Analog Converter
- Important Pins
  - Ref : the maximum voltage value that the DAC can reach
  - A7 : MSB of input word A
  - A0 : LSB of input word A
  - EN : Enable
- Instance Params
  - Common instance params can refer to ¥-Device section (e.g. REF)

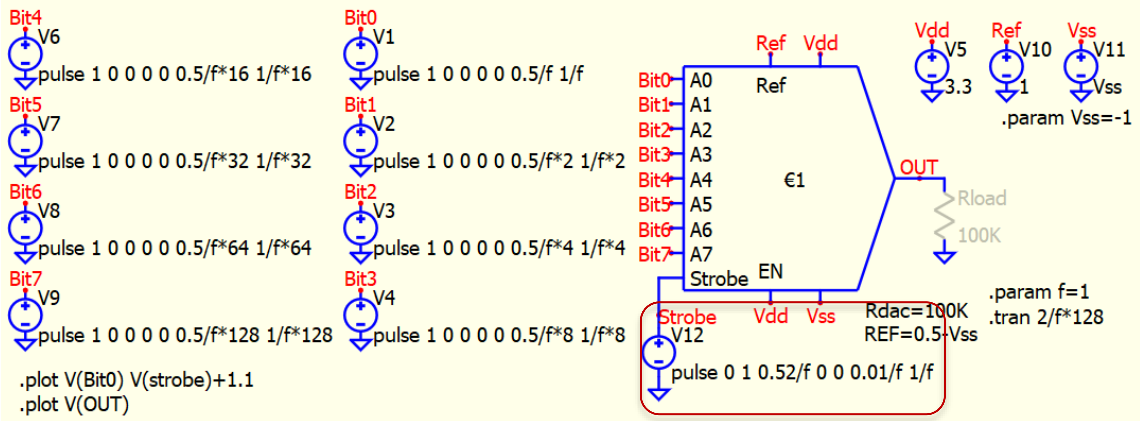


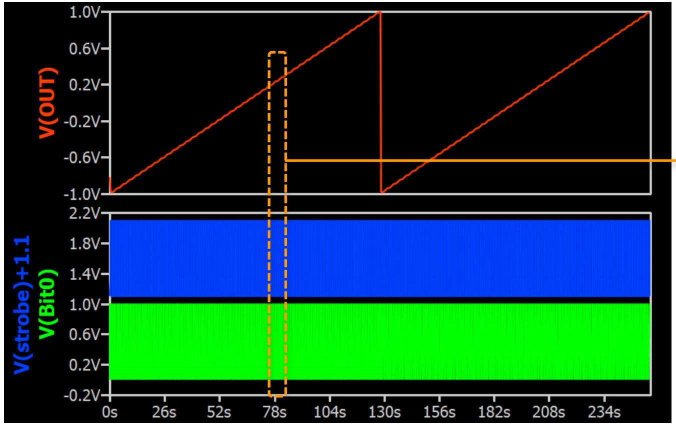


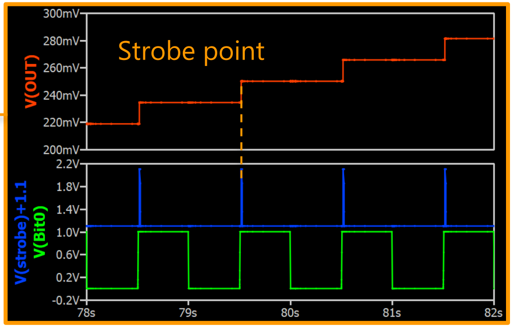
€-Device DAC : Build-in Symbol DAC8strobe.qsym

Qspice : DAC - Strobe.qsch

- Strobe
  - In practice, it named as load DAC strobe (LDAC)
  - This pin transfers all input register data to the DAC registers
  - It resolve jitter in V(out) in previous slide
- Symbol
  - Build-in symbol with strobe is
  - DAC8strobe.qsym



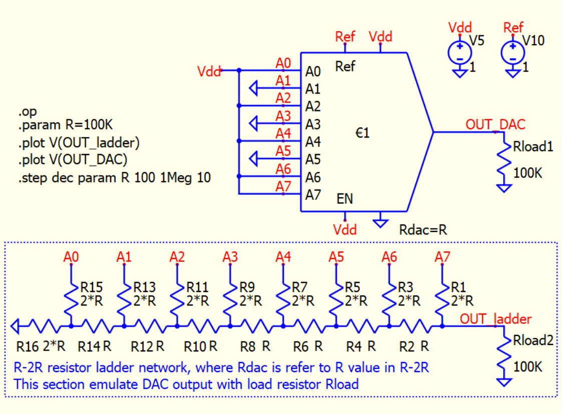


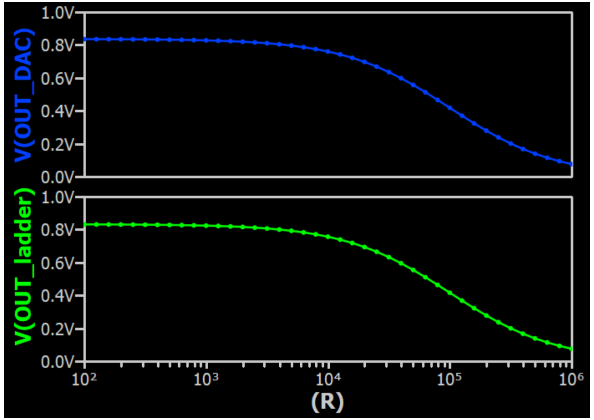


€-Device DAC Instance Params : RDAC

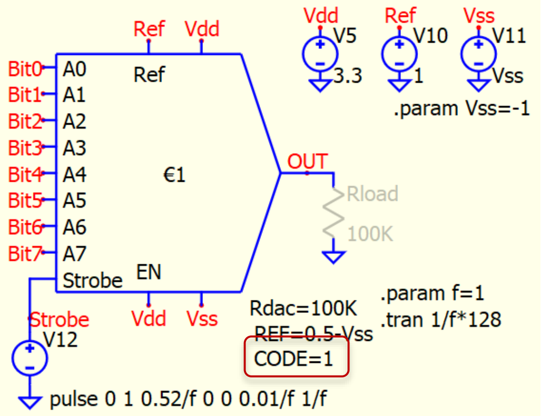
Qspice : DAC - RDAC.qsch ; DAC - CODE.qsch

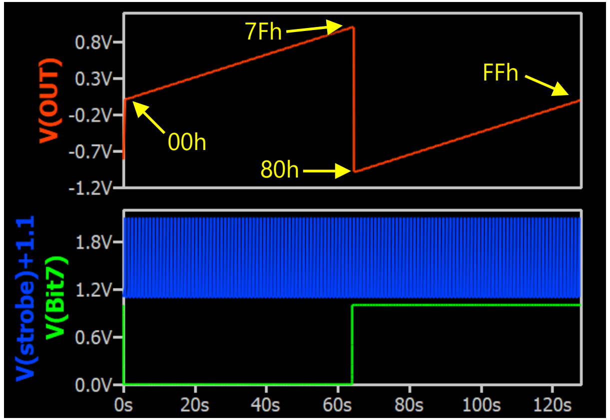
- RDAC
  - Rdac : R of R-2R DAC
  - R-2R resistor ladder network is inexpensive solution for digital to analog conversion
  - Reference
    - https://en.wikipedia.org/wiki/Resistor_ladder
  - Therefore, to prevent loading effect, a voltage buffer should be used in DAC output





- CODE
  - Code : Non-zero maps from -n to n-1 to 0 to 2n-1
  - **Default CODE=0**
  - CODE=0 : Unsigned
  - CODE=1 : Signed - two's complement



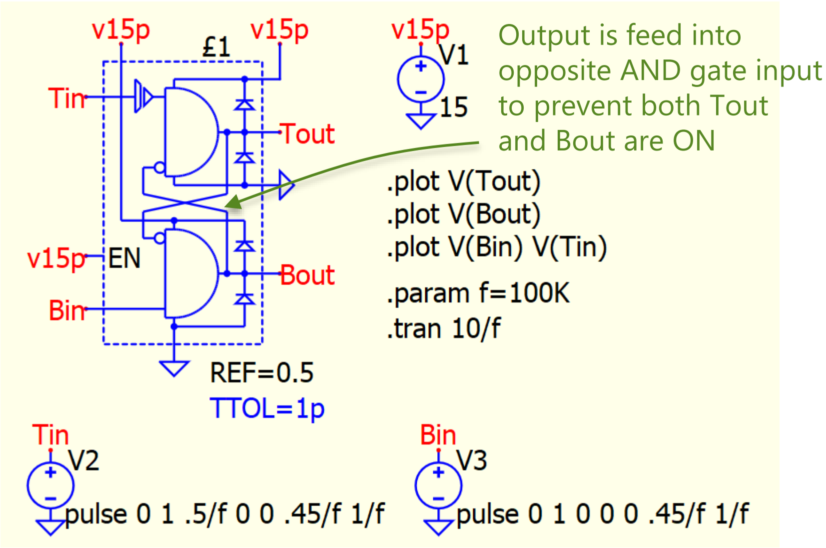


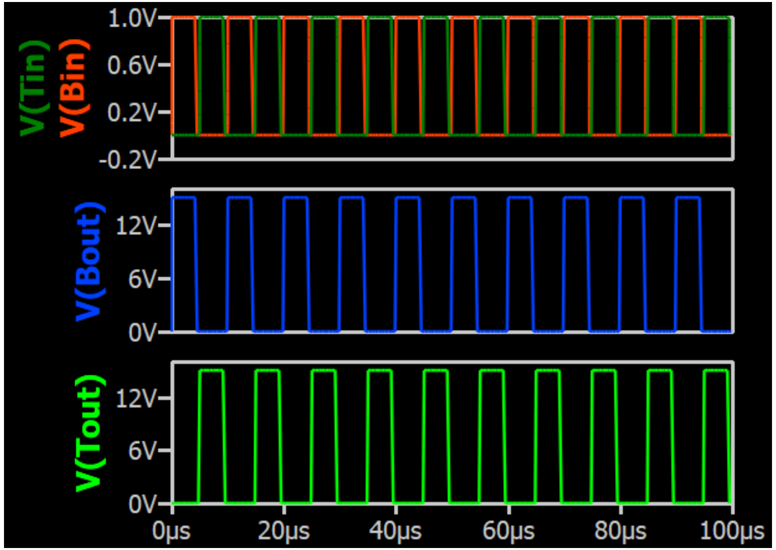
£-Device

£-Device : Dual Gate Driver

Qspice : Dual Gate Driver.qsch

- £-Device Dual Gate Driver
  - Syntax: £nnn Vdd Vss BOOST TOPGATE SW BOTGATE TCTRL BCTRL EN ¥ ¥ ¥ … GATEDRIVER [INSTANCE PARAMETERS]
  - This behavioral device expects Top Input and Bottom Input has deadtime in between





£ [Dual Gate Driver] Instance Params

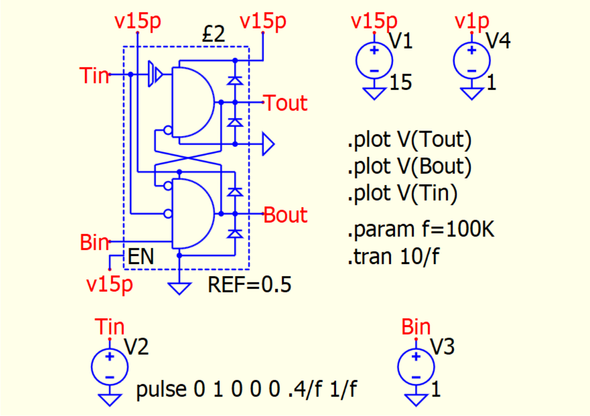
Gate Driver Instance Parameters

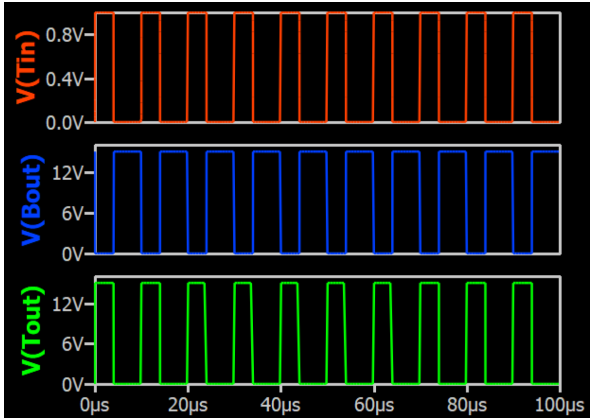
Name	Description	Units	Default
BOOST	Add logic such that the top FET is off if the bottom is controled to be on		(not set)
BUCK	Add logic such that the bottom FET is off if the top is controlled to on		(not set)
CAPVDD	Capacitance from a logic output to Vdd(or BOOST)	F	0.
CAPVSS	Capacitance from a logic output to Vss(or SW)	F	0.
M	Number of parallel devices		1.
REF	Logic reference for enable input	V	(Vdd + Vss) ÷2
ROFF1	Resistance used to pull bottom FET to VSS	Ω	RON1
RON1	Resistance used to pull bottom FET to VDD	Ω	1.
ROFF2	Resistance used to pull top FET to SW	Ω	ROFF
RON2	Resistance used to pull top FET to BOOST	Ω	RON1
RPASSIVE	Resistance used to pull both FETs' gates low when the driver is not enabled	Ω	1Meg
TEMP	Instance temperature	°C	27.
TTOL	Temporal tolerance	s	
UVLO	Minimum Vdd-Vss voltage to operate	V	2.

£ [Dual Gate Driver] Instance Params - Buck and Boost

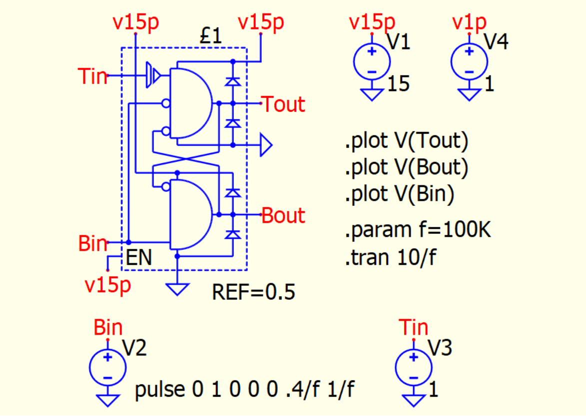
Qspice : Dual Gate Driver (Buck).qsch; Dual Gate Driver (Boost).qsch

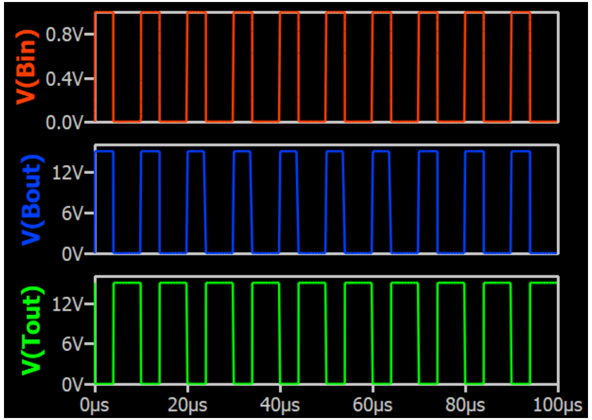
- BUCK
  - Add logic such that the bottom FET is off if the top is controlled to on
  - **Tin** is inverted to drive Bottom AND gate
    - Bin connects to LOW
  - Switch of buck converter is generally at High Side





- BOOST
  - Add logic such that the top FET is off if the bottom is controlled to be on
  - **Bin** is inverted to drive Top AND gate
    - Tin connects to HIGH
  - Switch of boost converter is generally at Low Side



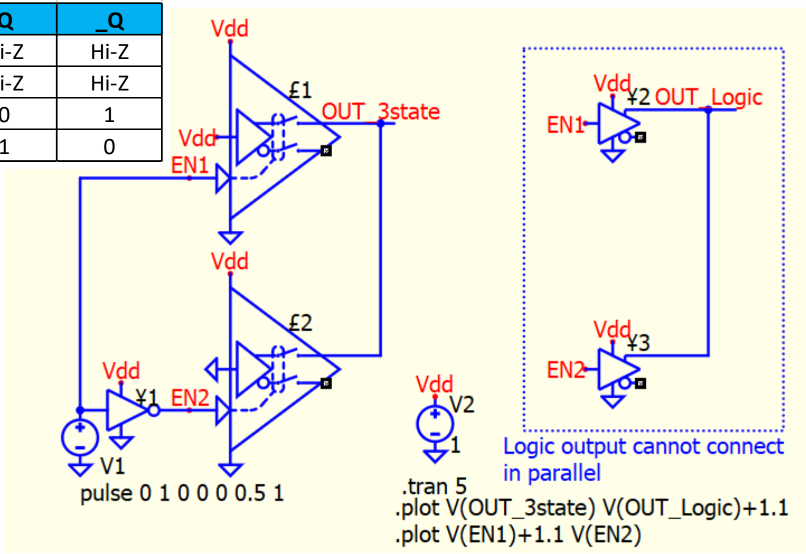


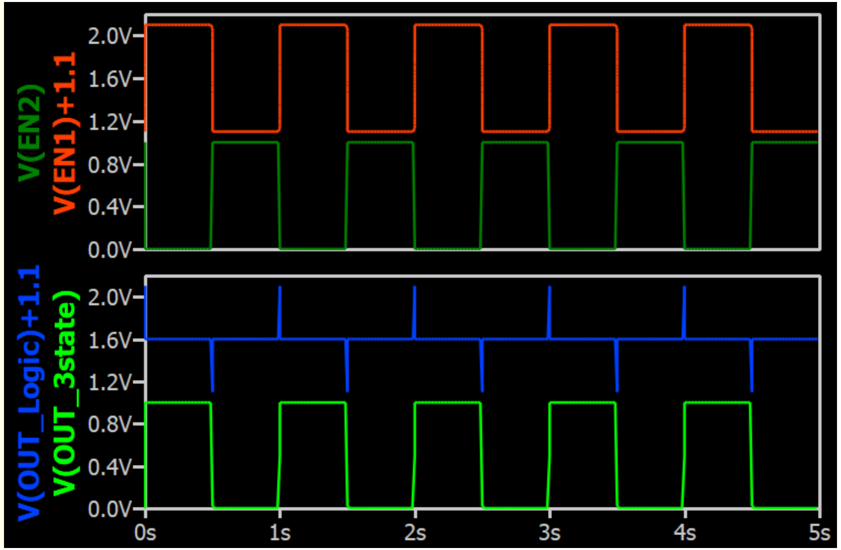
£-Device : Tri-state Buffer

- Tri-state Buffer
  - Syntax: £nnn Vdd Vss Q Q̅ IN EN ¥ ¥ ¥ … 3STATE [INSTANCE PARAMETERS]
  - A tri-state output allows multiple circuits to share the same output line(s)
  - Output into High-Z when disable

£-Device Tri-state Buffer

EN	IN	Q	_Q
0	0	Hi-Z	Hi-Z
0	1	Hi-Z	Hi-Z
1	0	0	1
1	1	1	0



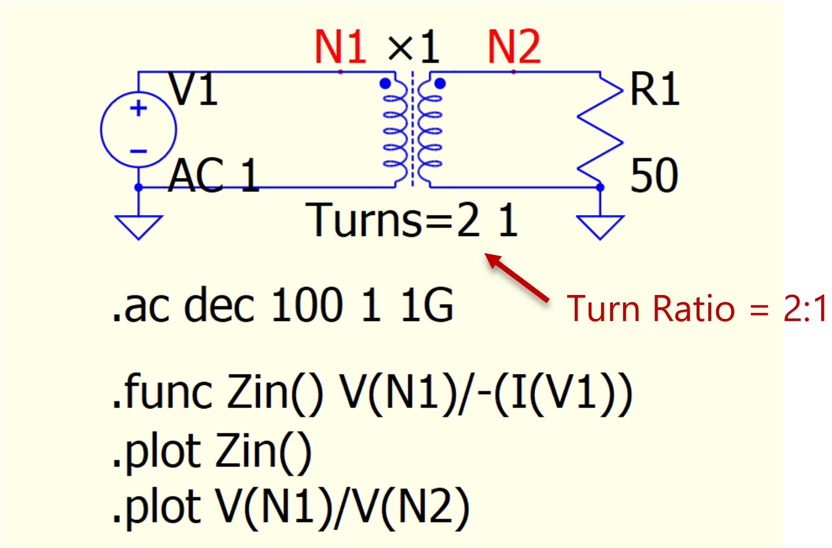


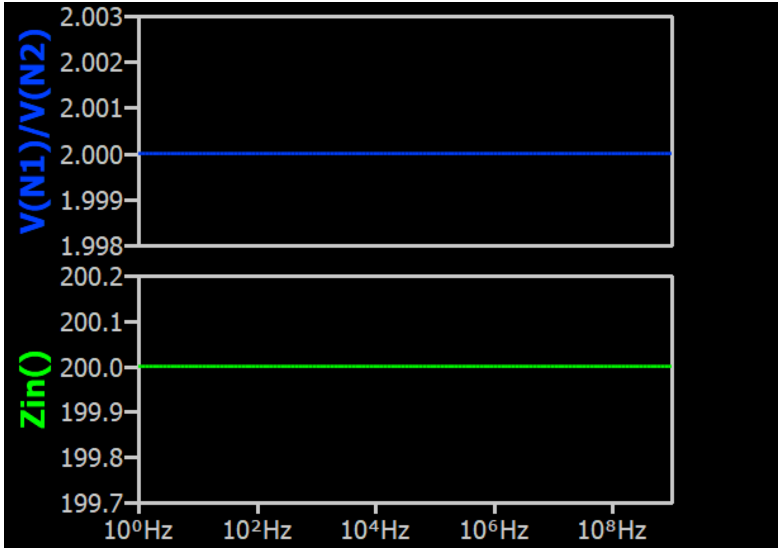
×-Device Transformer

×-Device: Transformer

Qspice : Transformer - Basic.qsch

- ×-Device: Transformer
  - Syntax: ×nnn «PRI+ PRI- SEC1+ SEC1- SEC2+ SEC2 [...]» <TURNS=N1 N2 N3 ...> [Additional Instance Parameters]
  - Ideal Transformer Equation (Inductance → ∞)
    - $n = \frac{N_1}{N_2} = \frac{v_1}{v_2}$ and $Z_{N1} = n^2 Z_{N2}$





×-Device: Transformer Instance Params

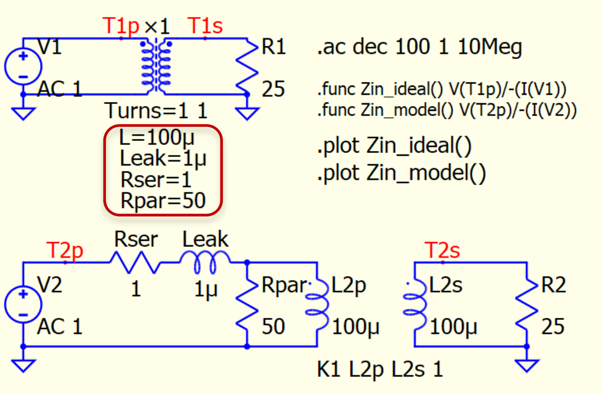
Transformer Instance Parameters

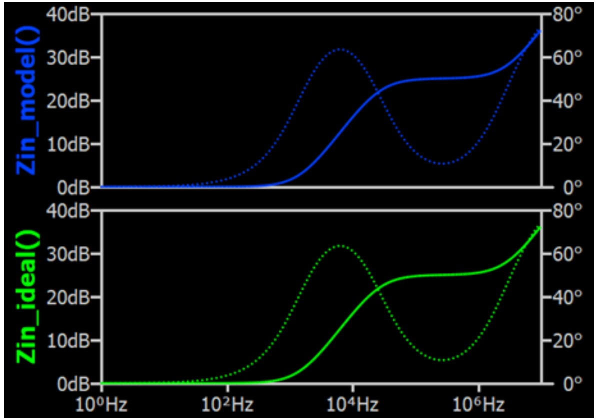
Name	Description	Units	Default
ISAT[1]	Current that drops inductance to SATFRAC of zero-current value	A	Infinite
K[1]	Alternate means of specifying LEAK		1
L	Primary zero-current inductance	H	Infinite
LEAK	Leakage inductance	H	0
LSAT[1]	Inductance asymptotically approached in saturation	H	10% of L
RPAR[1]	Primary parallel resistance	Ω	Infinite
RSER[1]	Primary series resistance	Ω	0.0
SATFRAC[1]	Fractional drop in L at ISAT		0.7
TURNS	List of relative number of turns		

× Instance Params : L, Leak, Rser, Rpar, Isat, Lsat, Satfrac

Qspice : Transformer - L Leak Rser Rpar.qsch ; Transformer - Isat Lsat Satfrac.qsch

- L, Leak, Rser, Rpar
  - L : Primary Inductance
  - Leak : Leakage Inductance
  - Rser : Series Resistance
  - Rpar : Parallel Resistance
  - Equivalent model is shown in this simulation





- ISAT, LSAT, SATFRAC
  - Isat : Current that drops inductance to SATFRAC*L
  - Satfrac : Fractional drop in L at Isat
  - Lsat : Inductance asymptotically approached in saturation
  - These parameters are ignored unless L is given