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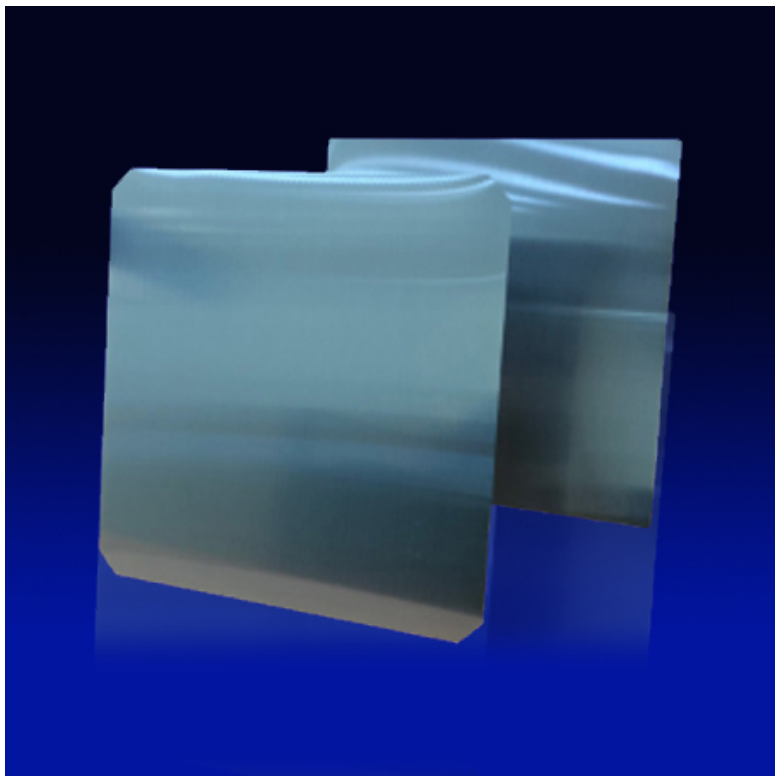

類方形單晶片為高效能太陽能應用裝置提供了最理想方案。 25 年以上的精湛半導體技術使我們能夠確保每一片單晶片都有優秀的晶體結構並且展現一流的成效。

	M2	UNIT
Diameter	210±0.25	
Square Length	156.75±0.25	mm
Angle Length	8.5±0.5	mm
Ingot Growing Method	CZ	
Dopant Type	Boron	

	M2	UNIT
Conductivity	P	
Orientation	‹100›±3°	
Resistivity	0.5-1.5	Ohm.cm
Thickness	180+20/-10 175+20/-10 170+20/-10	um

	G1	UNIT
Diameter	223±0.25	
Square Length	158.75±0.25	mm
Angle Length	1.07±0.5	mm
Ingot Growing Method	CZ	
Dopant Type	Boron	
Conductivity	P	
Orientation	‹100›±3°	
Resistivity	0.5-1.5	Ohm.cm
Thickness	180+20/-10 175+20/-10 170+20/-10	um

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2

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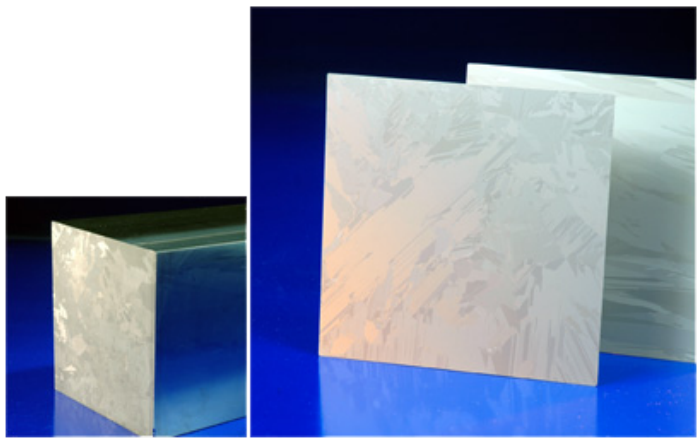
高效能多晶片



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	GENRAL SPEC.	UNIT
Square Length	157.00±0.25	mm
Chord Length	0.5-2	mm
Dopant Type	Boron	
Conductivity	P	
Resistivity	0.5-3	Ohm.cm
Thickness	180+/-20,200+/-20 um	

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3

Development of Heterojunction Back Contact Si Solar Cells

Junichi Nakamura, Naoki Asano, Takeshi Hieda, Chikao Okamoto, Hiroyuki Katayama, and Kyotaro Nakamura

***Abstract*—An energy conversion efficiency of 25.1% was achieved in heterojunction back contact (HBC) structure Si solar cell utilizing back contact technology and an amorphous silicon thin-film technology. A new patterning process was established, and it was applied to the fabrication process of HBC cells. In addition, the unique technology of the surface mount technology concept contributed to the superior performance of HBC cell. A short-circuit current density (J_{sc}) and an open-circuit voltage (V_{oc}) were 41.7 mA/cm^2 and 736 mV, respectively. The high J_{sc} as well as the high V_{oc} indicates the strength of HBC structure cell. Besides, a high fill factor of 0.82 was obtained, which shows that HBC structure cell does not have any fundamental critical losses caused from series resistance or shunt resistance. Such high values of *I–V* parameter means that the patterning process was properly performed.**

***Index Terms*—Back contact (BC), cell efficiency, heterojunction, patterning process, solar cell.**

I. Introduction

In order to achieve the so-called grid parity, it is necessary to reduce the cost of a solar power system including cell and module costs. Actually, the module cost is not necessarily the largest part of the total cost of an electrical power generation system. Therefore, it is important to enhance the energy conversion efficiency in order to decrease a total power generation cost including the costs of power conditioning subsystems, balance of systems, and so on.

For enhancing the conversion efficiency of crystalline Si-based solar cells, several concepts of cell structure designs, such as an interdigitated back contact (IBC) structure or double-faced heterojunction structure [1], have been studied. Fairly high conversion efficiencies of 24.6% [2] and 24.7% [1] were obtained in these structures, but a higher conversion efficiency over 25% is desired for further reduction in the power generation cost toward the "grid parity."

The HBC structure is one of the most likely candidates for higher performance of crystalline Si-based solar cells because it has the advantages of both the BC structure and the heterojunction structure between crystalline silicon (c-Si) and hydrogenated amorphous silicon (a-Si:H). The former has a high J_{sc} since there is no shading effect caused by the presence of front-side electrodes [3]. The latter brings a high V_{oc} because of its high-quality passivation. In fact, Panasonic corporation has reported a high conversion efficiency of 25.6% with the HBC structure [4].

Sharp has developed and commercialized c-Si BC structure cells and silicon-based thin-film solar cells in the history of its solar business. Therefore, we have both technologies of back contact (BC) structure and deposition of a-Si:H.

Thus, we decided to develop HBC structure cells and get a target of 25% cell efficiency by making full use of them.

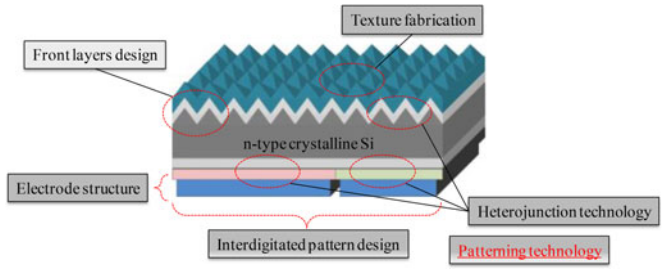

Fig. 1. Development issues of the HBC structure cell.

II. Development

Many issues shown in Fig. 1 are addressed in the HBC cell development. Table I shows affected parameters, targets, and solutions. There are some correlations between the issues; thus, when we tackle an issue, we have to pay a close attention to others.

First of all, we focused on an establishment of heterojunction technology. Although we already had the a-Si:H technology, we had not tried a-Si:H as a passivation layer on c-Si. Therefore, we needed to realize a technology of high-quality passivation at the heterointerface.

In addition, a fabrication process to form the IBC structure is important; especially, a patterning process is considered to be crucial. The precise patterning process is required to form the BC structure. Besides, any degradation in the cell performance induced by the process should be prevented. There had been no precedent for patterning technology of a-Si:H layers on c-Si; therefore, we had to develop a new patterning process.

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TABLE I
DEVELOPMENT ITEMS OF HBC STRUCTURE CELLS

Development issues	Major Affected Parameters	Critical targets	Solutions
Heterojunction Technology.	V_{oc}	• High quality of passivation. (= Long minority carrier lifetime)	• Optimizing cleaning and pretreatment conditions of substrate surface prior to deposition. • Optimizing a-Si:H deposition conditions. • Optimizing posttreatment conditions after a-Si:H deposition.
Patterning Process Technology.	FF, V_{oc}	• Ability of precise pattern formation as designed. • No negative impact on passivation quality. • No negative impact on optical property. • No negative impact on R_s and R_{sh}.	• Developing a new patterning process. • Optimizing any process condition.
Rear Side Pattern Design.	J_{sc}, FF	• Getting the optimum of performance.	• Designing by simulation. • Experimental trials and their feedbacks.
Electrode Structure Design.	FF	• Minimizing both contact resistance and sheet resistance.	• Materials selection. • Optimizing deposition conditions. • Feedbacks from high-precision evaluation of contact resistance.
Front Side Structure Design.	J_{sc}	• Maximizing incident light into substrate.	• Optimizing the structure using optical simulation. • Optimizing the deposition condition of ARC. • Widening the optical bandgap of a-Si:H layers. • Optimized texturing.

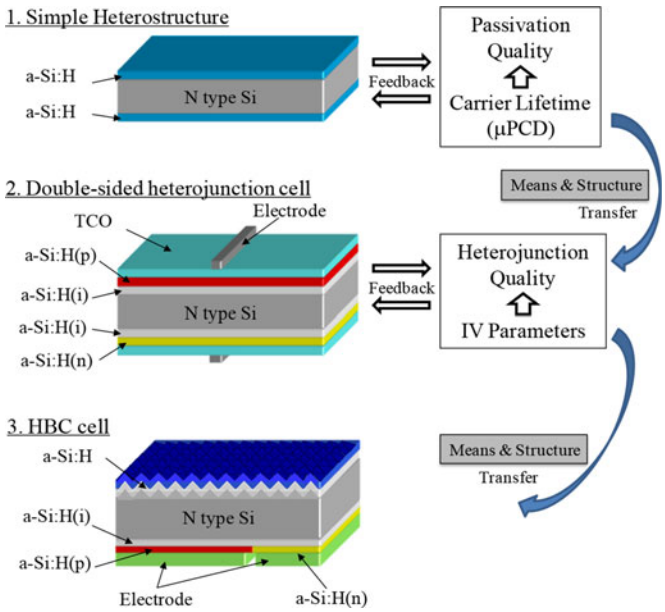

Fig. 2. Development steps of heterojunction technology.

A. Development of Heterojunction

In order to obtain a high V_{oc}, it is necessary to minimize the carrier recombination at heterointerface. In accordance with the prior related literature, following issues were examined:

1) control of crystallization of a-Si:H at the interface;
2) cleaning and pretreatment method of c-Si surface;
3) posttreatment method.

Our study of heterojunction technology was carried out based on the steps as illustrated in Fig. 2. A simple a-Si:H/c-Si heterostructure was fabricated, and we measured its minority carrier lifetime utilizing the microwave photoconductivity decay method to assess the passivation quality. Next, a double-sided heterojunction cell was fabricated, and we measured its *I–V* characteristics such as V_{oc} or fill factor (FF) to evaluate the heterojunction quality. Finally, the above outcome was applied to an HBC fabrication structure and process.

B. Development of the Patterning Process

In order to realize an HBC cell, it is imperative that any patterns are formed into a-Si:H layers. In the development of the HBC structure cells, the development of the patterning method is considered to be one of the most important issues because it strongly affects not only the precise formation of the HBC structure but the passivation quality of the heterointerface as well. Actually, an incomplete process brought about some insufficient performance of cells such as a parasitic resistance or shunting. The patterning issue of the HBC structure is widely recognized; thus, there have been studied various approaches for the development of a new patterning process [5]–[13].

In an HBC cell, a part of its rear face makes an emitter, and the other part makes a collector. In a conventional IBC cell, both emitter and collector are formed by selecting the diffusion doping areas. However, this fabrication process cannot be applied to the HBC process because the dopant diffusion requires a high process temperature. The HBC process, which includes the a-Si:H layers in the structure, should be executed under at a lower temperature than 200 °C. As there was no precedent for a-Si:H patterning process on c-Si, we had to create a new patterning process for HBC cells.

We should take into account the following criteria of the process:

1) ability of precise formation as intended;
2) no negative effect on the passivation quality for each interface;
3) no negative effect on optical property like a reflection or a transmittance at the incident surface;
4) no increase of series resistance;
5) no decrease of shunt resistance.

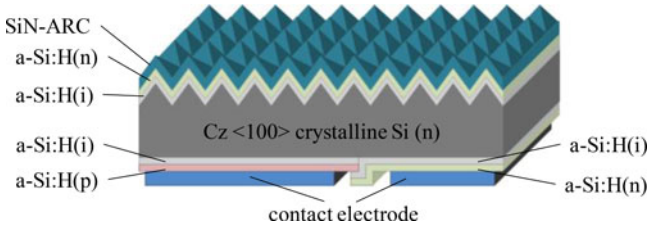

Fig. 3. Structure of HBC structure cells.

After the studies of various processes, the best candidate was chosen, and details of the process conditions were carefully adjusted.

III. Experiment

A. Structure of Heterojunction Back Contact Cells

Fig. 3 shows the schematic structure of HBC cells in this study. Cz-grown, n-type, <1 0 0> oriented single crystal silicon substrates were used. Both an incident surface and a rear surface were covered by a-Si:H layers for high-quality passivation. On the rear surface, both n-type a-Si:H and p-type a-Si:H were located, and then, electrodes were formed on each a-Si:H layers. Interdigitated layout was applied for the rear design of emitter and collector. At the front side, texture was formed, and a SiN antireflection coating (ARC) layer was deposited so as to enhance the light incident into the c-Si substrate. At a boundary area between electrodes, a-Si:H(i/n) layers partly overlapped the a-Si:H(i/p) layers so that c-Si surface was not exposed.

B. Fabrication Process of Heterojunction Back Contact Cells

Fig. 4 shows the flow of an HBC cell fabrication process. As-sliced substrates were prepared, and then, a saw damage was removed. The substrate surface was cleaned and pretreated prior to a-Si:H deposition by plasma-enhanced chemical vapor deposition. Front-side a-Si:H(i)/a-Si:H(n) layers and rear-side a-Si:H(i)/a-Si:H(p) layers were deposited consecutively. After that, rear-side a-Si:H(i)/a-Si:H(p) layers were partially etched off by mixed acid using a conventional photolithographic technology. Then, after the cleaning and pretreatment, a-Si:H(i)/a-Si:H(n) layers were deposited in the same way on all over the rear surface, and these a-Si:H(i)/a-Si:H(n) layers were partially removed by alkaline etchant avoiding damage to a-Si:H(i)/a-Si:H(p) layers.

This step is especially important; here, we used an etch-stop mechanism. In this step, it is necessary that only the a-Si:H(i)/a-Si:H(n) layers are removed, and on the other hand, the a-Si:H(i)/a-Si:H(p) layers should not be etched and damaged. Using the alkaline etchant, we can etch only a-Si:H(i)/a-Si:H(n) layers off because of an extreme difference in etching rates.

Next, ARC of SiN was deposited on the front a-Si:H layers. Finally, electrodes were deposited on the rear side by the vacuum evaporation method and patterned into an interdigitated layout using photolithography.

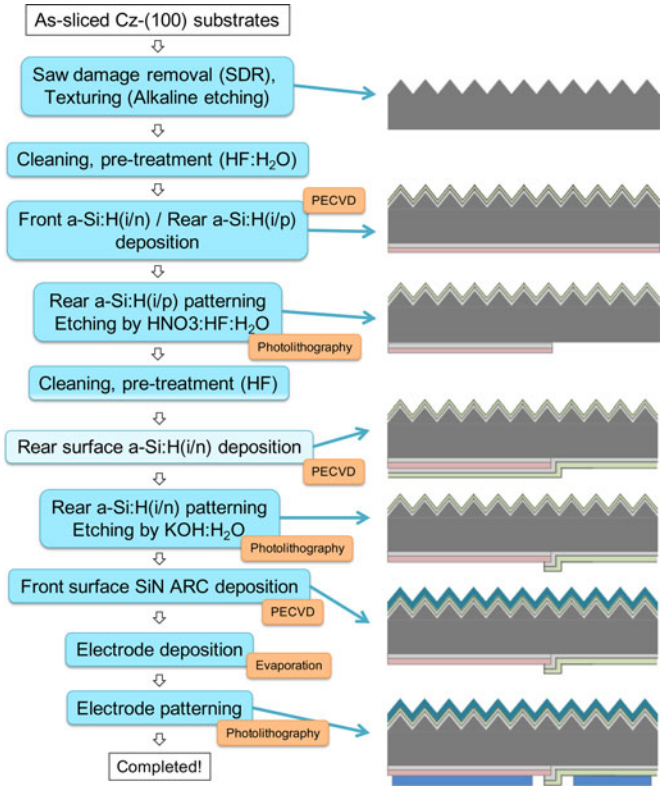

Fig. 4. Fabrication process flow of HBC cells.

During the patterning processes, the front-side a-Si:H(i)/a-Si:H(n) layers and ARC were properly protected from the etchants.

C. I–V Characterization of Heterojunction Back Contact Cells

In Sharp's IBC modules, surface mount technology (SMT) has been applied [14]. We also used it for the *I–V* measurement of HBC cells. The SMT is an excellent and unique approach to realize good electrical contact and wiring to BC cells. During *I–V* measurement, as shown in Fig. 5, HBC cells are temporally mounted on a flexible printed circuit, and thereby, the cell electrodes are directly connected to the wiring lines.

There are the following advantages in SMT.

1) It can reduce the series resistance due to the sheet resistance of the electrodes.
2) It can eliminate the dark space loss caused by the interconnection pads because no interconnection pad is necessary.
3) It can reduce the stress between the cell and the interconnector because all the area of solar cell can be used for the interconnection, and thereby, the stress can be dispersed.

Thus, the SMT can be utilized also for the *I–V* measurements of HBC cells.

I–V characteristics of the HBC cells were independently measured by Japan Electrical Safety & Environment Technology Laboratories (JET) with the aperture area of 3.7196 cm^2 and with expanded combined uncertainty ($U_{95}k = 2$) of 3.30%.

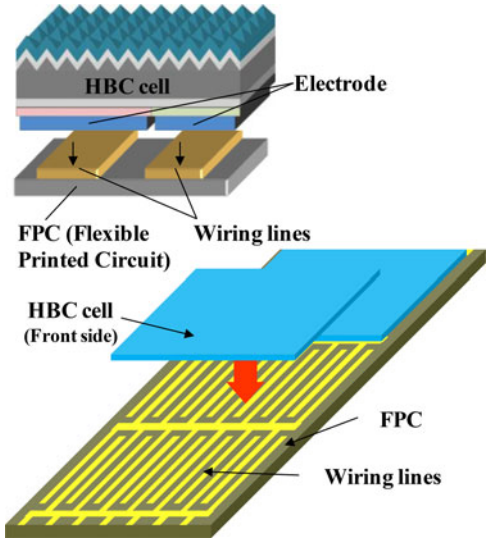

Fig. 5. Schematic view of the SMT concept.

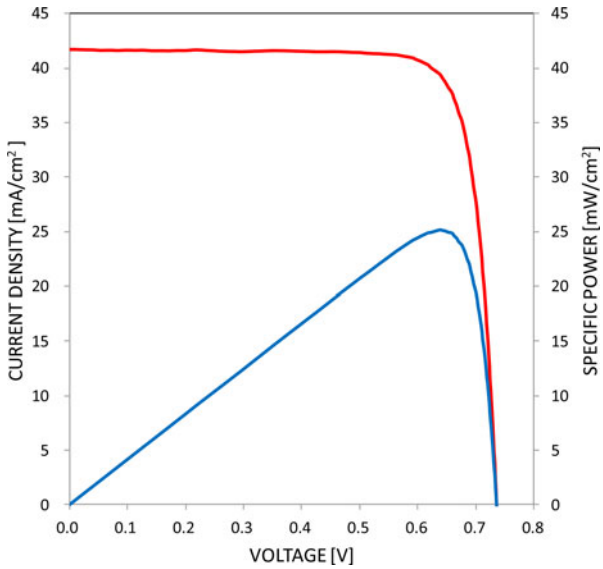

Fig. 6. *I–V* measurement result of an HBC cell. Measurement conditions: an aperture area of ca. 19.3×19.3 mm, AM1.5, 1000 W/m^2, and at 25 °C. Measured by JET.

TABLE II
I–V PARAMETERS OF THE HBC CELL OF 25.1%

J_{sc} (mA/cm^2)	V_{oc} (mV)	FF(%)	η(%)
41.7	736	81.9	25.1

IV. RESULTS AND DISCUSSION

A. *I–V Characteristics*

Fig. 6 shows an *I–V* measurement result for one of the HBC cells. A high cell efficiency of 25.1% was achieved, which exceeded our target.

A high V_{oc} represents that good passivation was realized at each surface, showing the merit of heterojunction. A high J_{sc} represents the advantage of the BC structure, which has no electrode on the incident surface. Furthermore, a high FF suggests that the SMT works well, and besides, there are no fundamental demerits from the viewpoint of series and/or shunt resistance in HBC cells. As a result, high V_{oc}, J_{sc}, and FF were simultaneously realized. Our results imply that the fabrication process including the patterning is successfully executed and show high-performance potential of HBC cell as well.

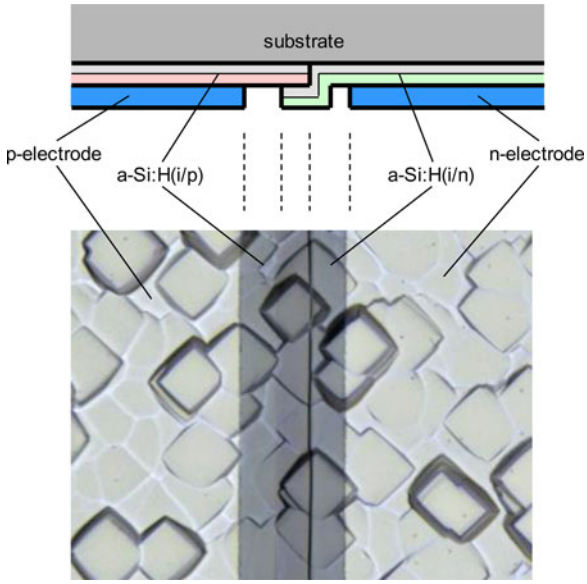

Fig. 7. Microscopic photograph of the rear side of an HBC cell.

B. *Performance of the Patterning Process*

In order to make sure the quality of our patterning process, we observed the rear surface. Fig. 7 shows a microscopic photograph of the rear surface of an HBC cell. This is around the boundary between emitter and collector areas. Right bright area is an n-electrode, and left one is a p-electrode. Between them, a-Si:H(i/p) layers, a-Si:H(i/n) ones, and their stacked area are exposed. As shown in the photograph, emitter, collector, and electrodes are properly formed, and each layer has a clear and straight edge.

In order to investigate the passivation quality, we compared the carrier lifetimes between before and after the patterning process as shown in Fig. 8. Horizontal axis is a normalized carrier lifetime after the a-Si:H(i/p) layer deposition and before the patterning process, and vertical axis is a normalized carrier lifetime after the patterning process and before the ARC deposition. All carrier lifetimes were divided by a certain value for the normalization. The carrier lifetimes after the patterning process were nearly the same or higher than those before the patterning process. Consequently, it was found that the newly developed patterning process worked well as intended.

C. *Progress of Heterojunction Back Contact HBC Cell Efficiency*

Fig. 9 shows the progress of our HBC cell efficiency. Our work started about three and a half years ago. A goal of over

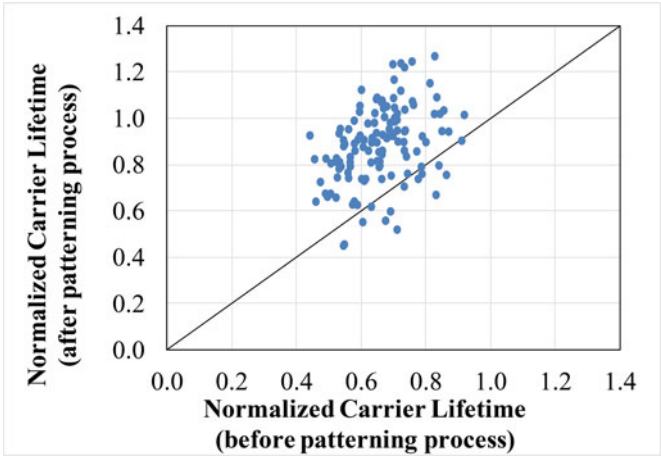

Fig. 8. Comparison between the minority carrier lifetime before and after the patterning process.

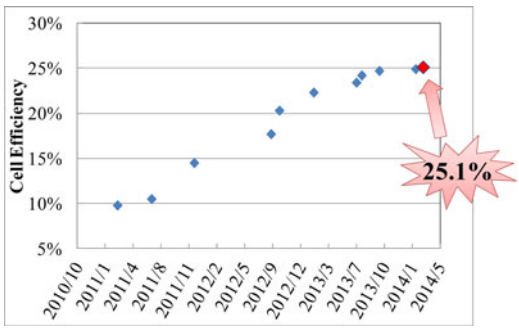

Fig. 9. Our record of HBC cell efficiency progress.

25% efficiency was achieved in such a short time. This is due to the high potential of the HBC concept, and at the same time, we were able to develop efficiently making full use of Sharp's accumulated technological strength.

V. Conclusion

The HBC structure Si solar cell was successfully developed, and a high conversion efficiency of 25.1% was achieved. Sharp's own technologies were effectively applied in the development of HBC cells as follows:

1) technology of a-Si:H film deposition;
2) technology of the IBC structure cell;
3) measurement technology of the SMT concept.

In addition, a new patterning process was established for the HBC cell fabrication, and it was found to work well. Thereby, the high potential of HBC cells was demonstrated in this study, indicating high J_{sc}, V_{sc}, and FF, simultaneously.

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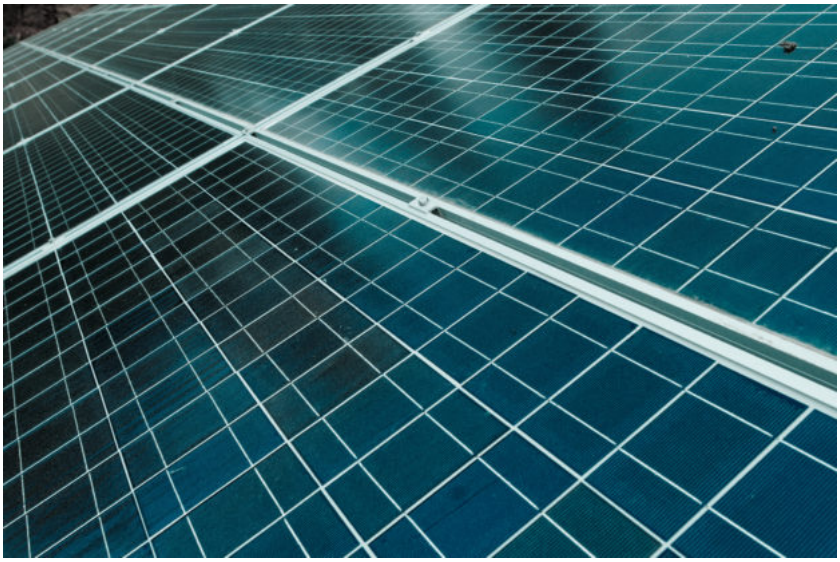
4

TechNews 科技新報

鈣鈦礦─矽太陽能創新紀錄，轉換效率高達 29.2%

作者 Daisy Chuang | 發布日期 2021 年 11 月 02 日 16:04 | 分類 太陽能 , 材料、設備 , 能源科技



歐洲薄膜太陽能電池研究聯盟 Solliance 最近研發出超高效率的串疊型太陽能電池，電池由鈣鈦礦太陽能與矽晶構成，轉換效率高達 29.2%。

Solliance 與荷蘭應用科學研究組織（TNO）、能源研發創新中心 EnergyVille、恩荷芬理工大學看中新型串疊型太陽能的潛力，有助提高轉換池採用四接點（4 Terminal， 4T）結構，也就是上下兩個電池採獨立連結方式，而不像傳統兩接點（2 Terminal， 2T）為上下串聯。

Solliance 研究串疊型電池已久，4 月打造將轉換效率 28.7% 的串疊型模組，但如果要再跨出步伐，還得再試試，TNO 串聯太陽光電計畫經理透明鈣鈦礦電池具有寬能隙優勢，也能允許近紅外光穿透，有助提高轉換效率。

團隊新使用的透明鈣鈦礦太陽能在最大功率點追蹤（Maximum power point tracking）狀態下 5 分鐘，轉換效率測得 17.8% ，隨後團隊將矽池與透明的鈣鈦礦電池相結合，創下 29.2% 新世界紀錄 4T 鈣鈦礦─矽串聯效率。Coletti 認為，這片 4T 電池將來可應用在公用事業大型太陽能電

團隊也有將鈣鈦礦電池與薄膜太陽能串聯，最終成績也頗為理想，將薄膜太陽能 MiaSolé Hi-Tech 製造的柔性銅銦鎵硒（CIGS）串接後，2T 達 27.1%。

- Solliance hits 29.2% efficiency on perovskite/silicon tandem solar cell
- TWO WORLD-RECORDS FOR 4T PEROVSKITE TANDEM

（首圖來源：Flickr/David Goehring CC BY 2.0）

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關鍵字: 串疊型太陽能 , 太陽能電池 , 鈣鈦礦太陽能

0則留言 排序

新增回應……

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TechNews 科技新報

轉換率達 23.5%，工研院 TOPCon 太陽能電池亮相

作者 侯 冠州 | 發布日期 2021 年 10 月 14 日 18:28 | 分類 光電科技 , 太陽能 , 能源科技

2021 年 TIE 台灣創新技術博覽會同步今日以線上加實體展覽的形式亮相，而工研院也在展會中秀出前瞻太陽能技術「穿隧氧化層鈍化接觸（T 前已試量產成功，期能藉此提升台灣於太陽能產業國際競爭力。

根據台灣電力公司今年七月公布的再生能源發電概況顯示，太陽能發電已超越慣常水力發電成為台灣第一大再生能源；而為了更充分利用太陽 TOPCon 太陽能電池。

據悉，此一技術特點是以超薄氧化層及多晶矽層來作為背面鈍化堆疊層，可利用既有 PERC 產線簡單升級，來避免使用成本昂貴的電漿輔助化 反應式電漿沉積（RPD）等設備；同時，鈍化的表層更能有效降低表面陽光反射、充分將太陽光能吸入利用。

工研院進一步說明，TOPCon 太陽能電池可降低光源反射，有效地提升光電轉換效率，在高溫環境下有著更好的穩定性。目前該技術轉換效率 2%，能節省 10% 以上太陽能電廠用地面積，改善在陰雨天等低照度時的發電能力與烈日下的高溫衰減達 3%，適合台灣氣候，能源回收期（Ener 也大幅縮短。

工研院綠能與環境研究所所長王人謙表示，TOPCon 太陽電池具有光電轉換效率高、投報率高、能源回收期短三大優勢。目前已試量產成功，模組功率達 360W，並已於工研院台南六甲院區進行戶外驗證，粗估 20MW 試量產電池及模組每年產值上看台幣 3 億元，為台灣太陽能產業帶來

（首圖來源：工研院）

00:00/00:00 technews

關鍵字: TOPCon 太陽能電池 , 再生能源 , 工研院 , 永續發展

1 則留言 排序

新增回應……

陳懷祖
看起來很不錯，已經達23.5~~
有機會買來自家自己裝!!
讚 · 回覆 · 3週

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