Department of Electrical & Electronic Engineering
Bangladesh University of Engineering & Technology

EEE458 VLSI II Laboratory
Laboratory Module 4:
Layout design with Cadence Virtuoso Layout Suite L Editor

Objectives:

- To create a layout view of the basic inverter circuit from scratch.
- To perform the design rule check of the inverter

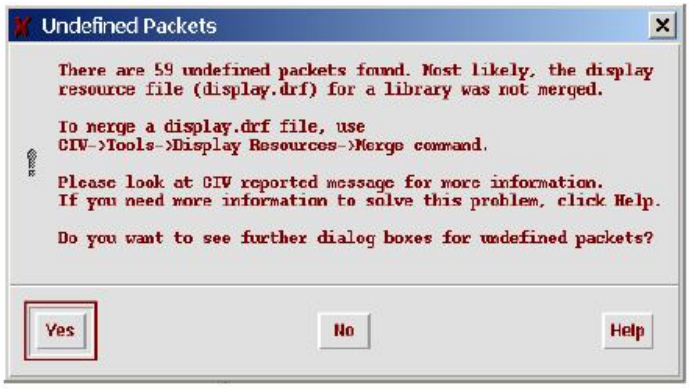
Lab 4-1 To setup the Virtuoso Layout Suite L Editor

The VLSI design process goes through the following steps:
Schematic Design → Schematic level Simulation → layout → Design Rule Check (DRC) → Layout vs. Schematic (LVS) Check→ active device and parasitic Extraction → Layout level Simulation.

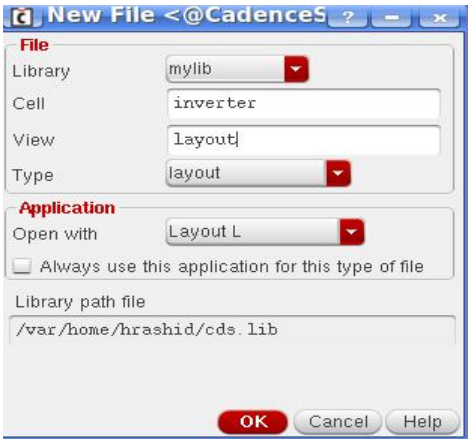
The tool for layout creation is called Virtuoso Layout Suite L. Before working with Layout editor you need to set the design layers. These information are stored in the *display.drf* file of the PDK.

If the dsplay.drf file is not auto loaded and you do not manually load it, you will get error message about missing packets when you try to open a schematic or layout view and you will not be able to see any process specific layers.

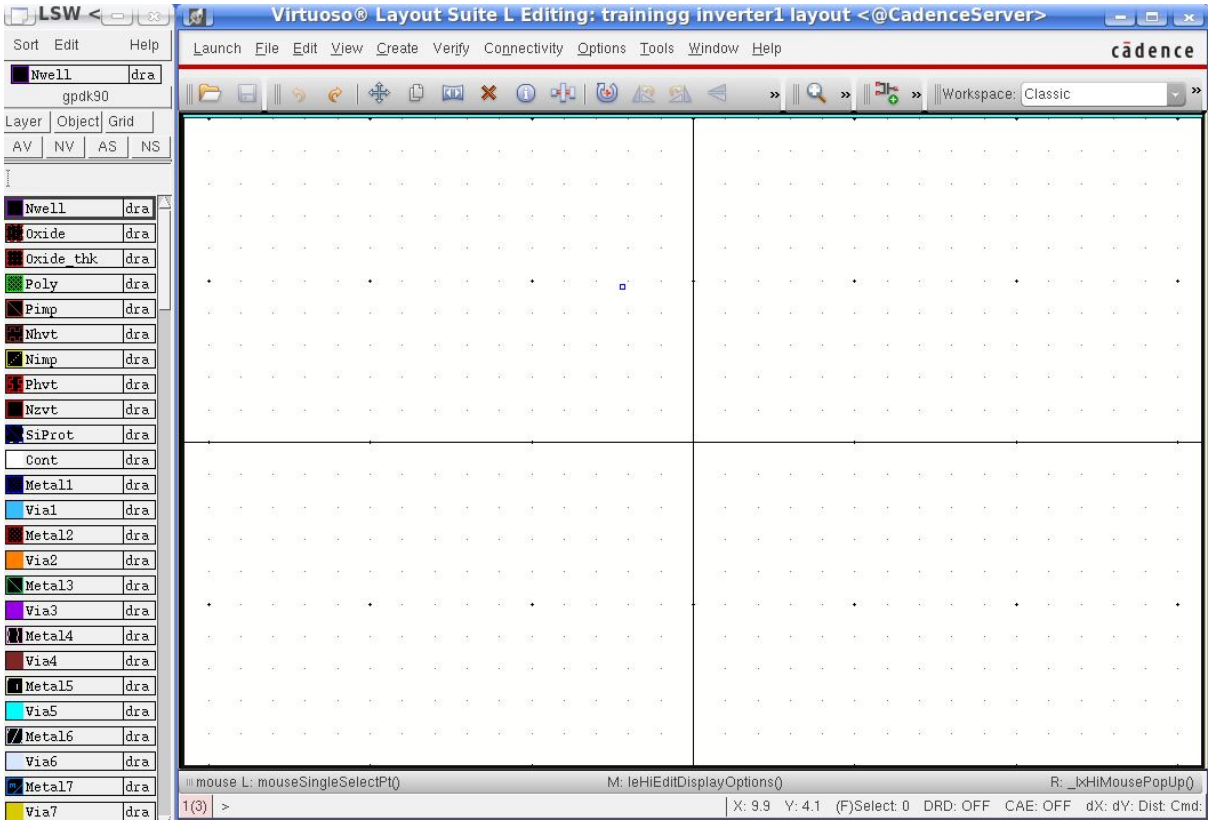
NOTE: *If the layout-drawing tools are not correctly shown in the LSW window, an error information shows up as follows.*



After the preparation is done invoke the Layout Suite L Editor from the CIW by executing ***File → New → Cell View***. The new file form appears and fill it as shown in the figure below.



Two windows should have appeared. The Virtuoso Layout Editing window and the LSW (Layer Select Window) window. The LSW window is the one you will use to choose the different layers of the IC design.

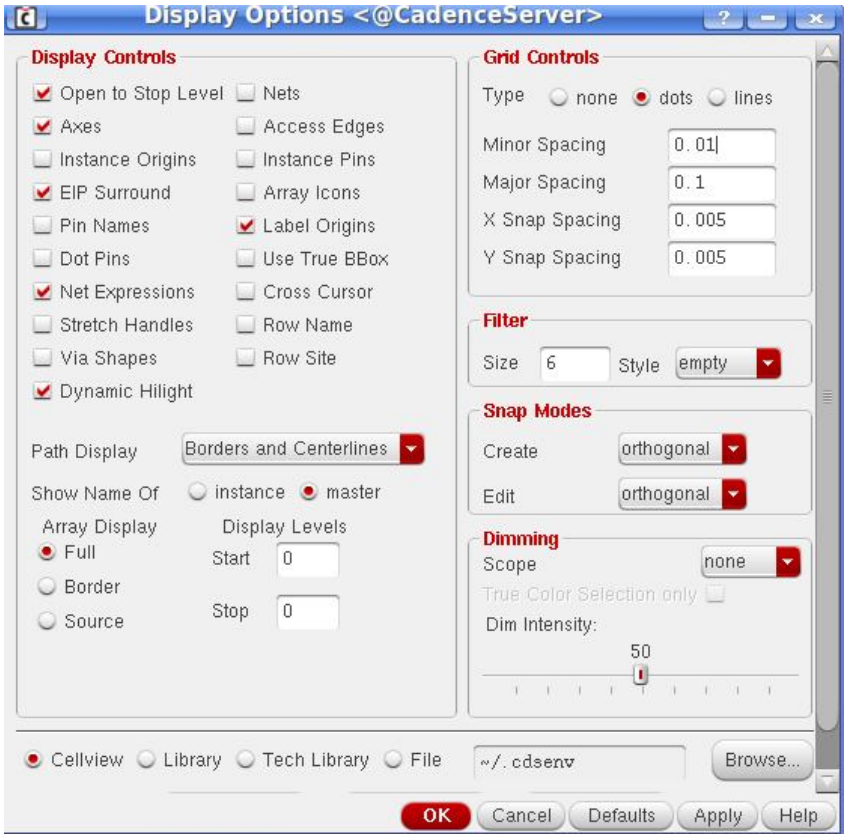


The LSW window is divided in three main categories which are : layer color, layer name and layer purpose. The detailed is described in the table below:

Color	Matches the color in the Editing window. Each layer has its own color and pattern. Each layer has two colors associated with it; a fill color and an outline color. These colors can be changed to fit your taste by editing the technology file.
Name	What is the type of layer (Newll, Oxide, poly, metal1, etc)
Purpose	In gpdk090 the only purpose classification is dra=drawing slo=slot Drawing is used in layout, slot is used to create a whole for metal stress relief

Verify that the layers display corresponds to the gpdk090 layers shown in the GPDK 90 nm Mixed Signal Process Spec manual.

Before starting the layout, you need to setting the layout configuration. Execute the following in the Virtuoso Layout Editor***: Options → Display***. Configure the form as shown in the figure below:



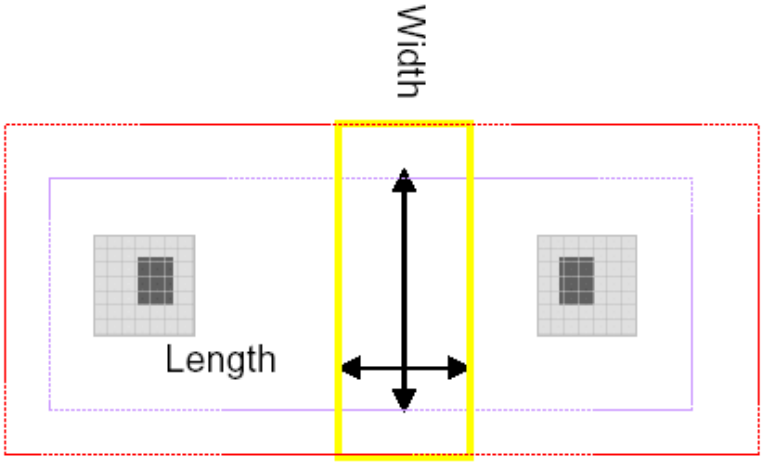
Also in the option → edit window deselect the gravity, which will enable you to draw layout between the grid points.

Lab 4-2 Building the layout of the CMOS inverter

Now we are going to build the layout of the inverter. An inverter has an NMOS and a PMOS transistor. First we will build an NMOS transistor.

Study the device layout examples shown in page 12 of the GPDK 90nm Mixed Signal Process Specifications. As seen from the layer diagram the NMOS inverter consists of oxide, Nimp, Cont

and poly layers. Study the rules of these layers and calculate the minimum size of the poly, cont, oxide and Nimp layer to create a minimum size NMOS transistor.



nmos1v – 1.2 volt nominal VT NMOS transistor

Device Layers	
Layer	**Color and Fill**
Oxide	
Nimp	
Poly	
Cont	
Metal1	

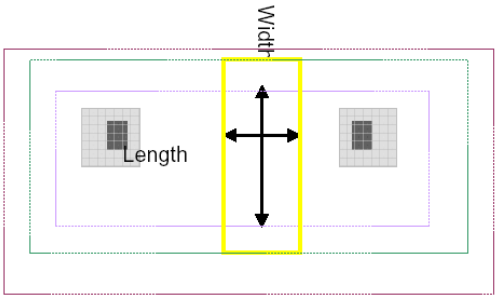
Fig: NMOS inverter layout levels

The rules related to the NMOS transistor can be summarised as follows :
Contact size : 0.12 umX 0.12 um (Fixed)
Poly width Minimum : 0.1 um (Fixed MOS gate length)
Contact to poly spacing (Minimum) : 0.1 um
Contact to oxide spacing (Minimum) : 0.06 um
Poly extending to oxide (Minimum) : 0.18 um
Nimp overlapping oxide (Minimum) : 0.18 um
Minimum Metal 1 width : 0.12 um
Maximum Metal 1 width : 12.0 um
Minimum Metal 1 to Contact enclosure : 0.06 um

Now we start building the NMOS transistor layout. Look at the LSW and find the current drawing layer and follow the procedure described below:

1. To create the active area of the NMOS, left click the oxide layer and make it the current drawing layer. In the Layout editor window execute ***Create → Shape → Rectangle***.
2. Draw the shape of the oxide layer after calculating its size.
3. In the LSW window select the Nimp layer and draw the Nimp rectangle.
4. In the LSW window select the poly layer and draw the poly gate rectangle.
5. In the LSW window select the Cont layer and draw the contact on both side of the poly gate

Now study the PMOS transistor structure in the GPDK 90 nm Mixed Signal Process Spec. The PMOS transistor consists of Oxide, Poly, Pimp, Cont and Nwell layer. Study the rules of these layers and calculate the minimum size of Poly, Cont, Oxide, Pimp and Nwell layer to create a minimum size PMOS transistor.



pmos1v – 1.2 volt nominal VT PMOS transistor

Device Layers	
Layer	**Color and Fill**
Nwell	
Oxide	
Pimp	
Poly	
Cont	
Metal1	

The rules related to PMOS are same as NMOS except the there is an additional layer the Nwell, whose rules are as follows :

Minimum Nwell width : 0.6 um

Minimum Nwell spacing to Newell (same potential) 0.6 um

Minimum Nwell spacing to Newell (different potential) 1.2 um

Minimum Nwell spacing to N+ active area : 0.3 um

Minimum Nwell spacing to P+ active area : 0.3 um

Minimum Nwell enclosure to P+ active area 0.12 um

Minimum Nwell enclousere to N+ active area 0.12 um

Minimum N+ Active Area to P+ Active Area Spacing 0.15 um

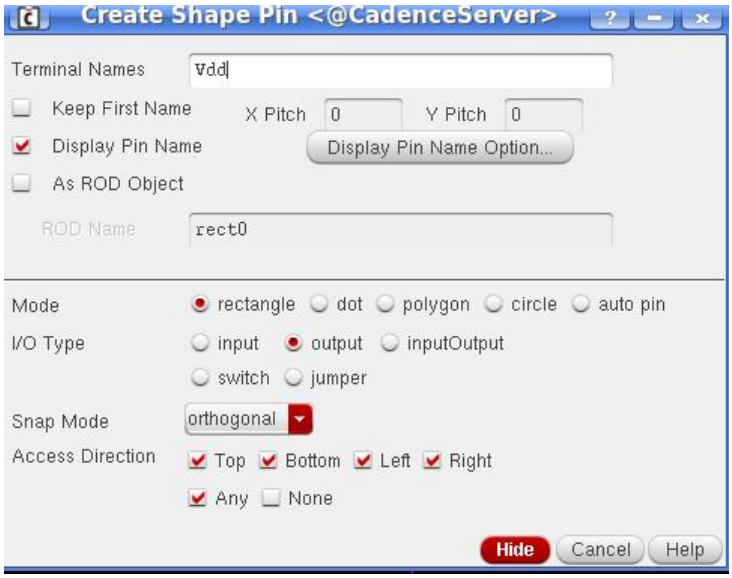
Minimum Contact to Contact spacing 0.14um

Now we start building the PMOS transistor layout. Look at the LSW and find the current drawing layer.

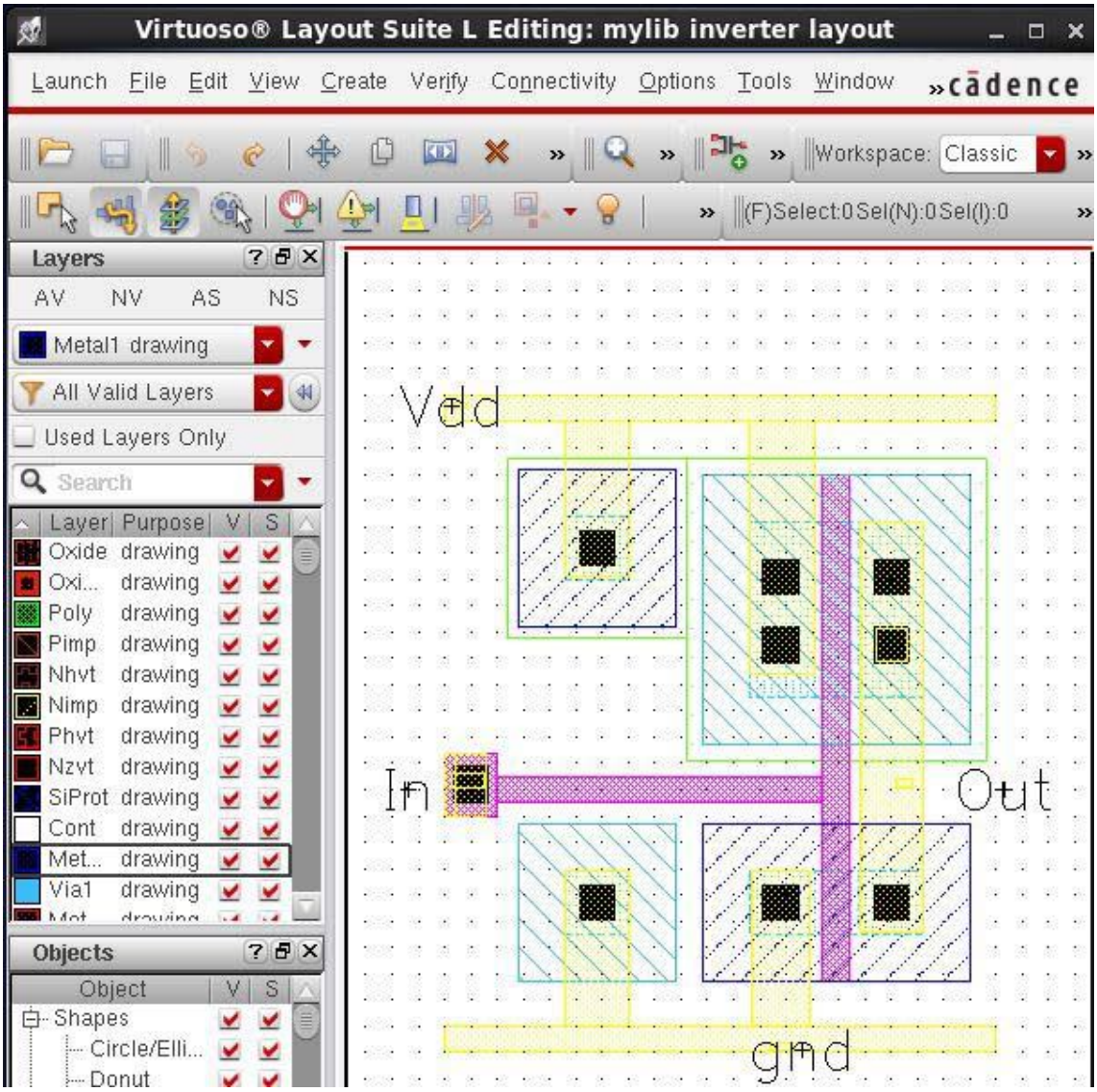
6. To create the active area of the PMOS, left click the oxide layer and make it the current drawing layer. In the Layout editor window execute ***Create → Shape → Rectangle***.
7. Draw the shape of the oxide layer after calculating its size.
8. In the LSW window select the Pimp layer and draw the Pimp rectangle.
9. In the LSW window select the poly layer and draw the poly gate rectangle.
10. In the LSW window select the Cont layer and draw the contact on both side of the poly gate.
11. In the LSW window select the NWELL layer and draw the NWELL rectangle.

Now create the input output pin in the layout as below

11. In the layout editor window execute the following : ***Create → Pin***. Make sure that you are selecting the **Metal1** in LSW.
12. To create the Vdd pin fill in **Create shape pin** Form as shown below and place the rectangle beside the Vdd bus.
13. In a similar way create the gnd pin
14. Now select the poly layer and create the In pin
15. Now select the Metal1 layer and create the Out pin.



Your layout would look some thing like below:

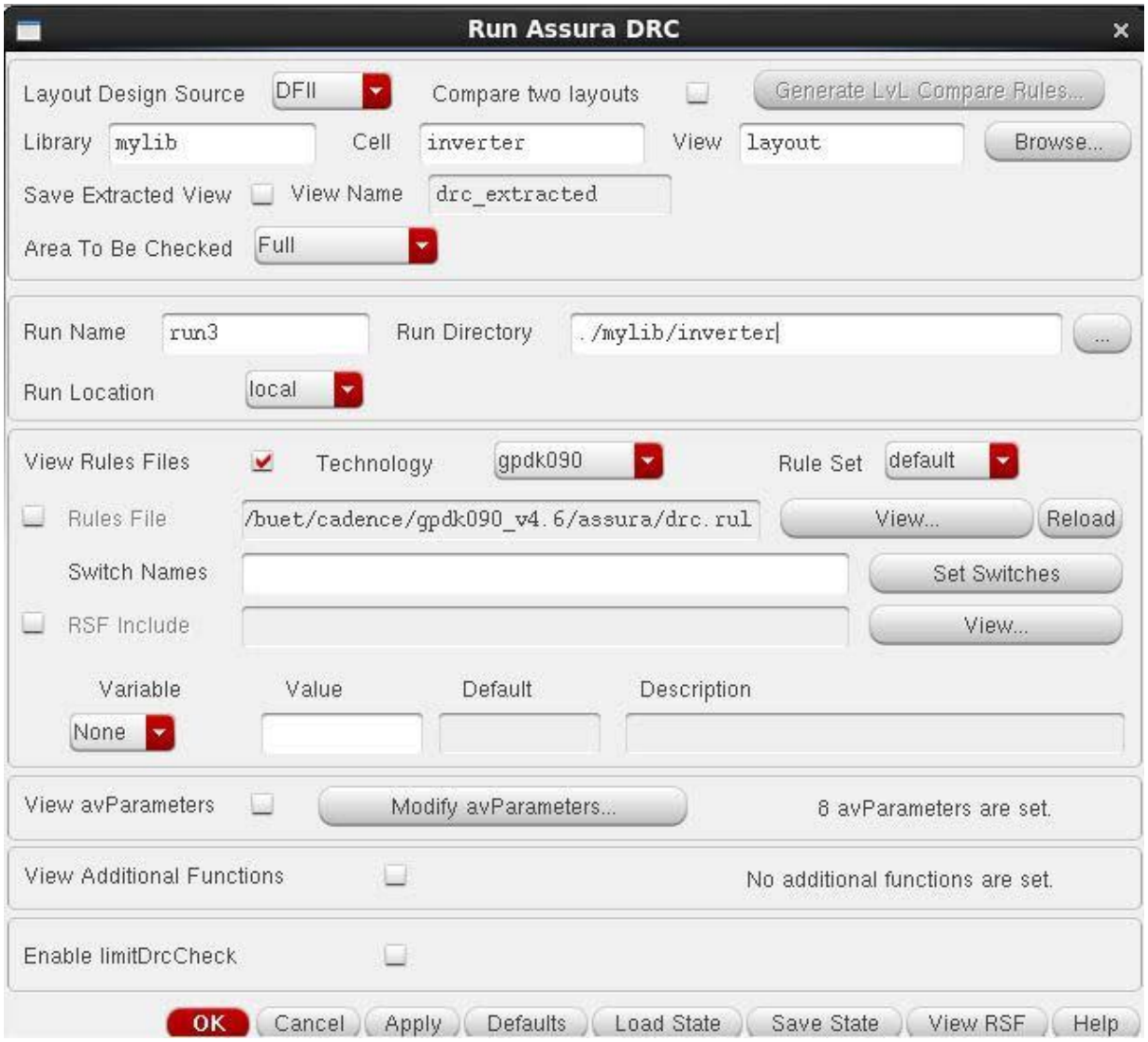


Lab 4-3 DRC Rules check by Cadence's ASUURA

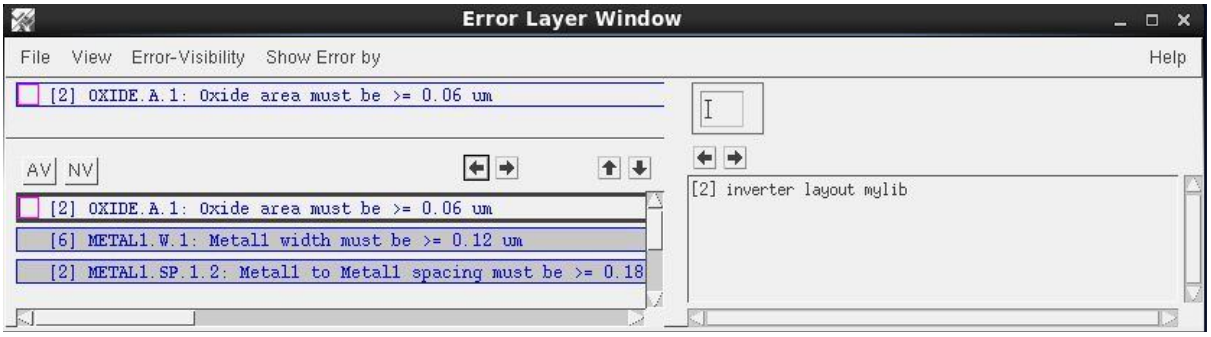
Now we would like to check whether our design have cleared all the DRC rules. We will use the program ASSURA for this purpose.

Running DRC

1. In the Layout Editor select Assura → Run DRC from layout window. The DRC form appears. The Library and cell name are taken from the current design window, but rule file may be missing. Click view Rule file and Select the technology as gpdk090. This automatically load the rule file.



2. Click OK to start DRC.
3. A progress form will appears. You can click on the watch log file to see the log file.
4. When DRC finishes, a dialog box appears asking you if you want to view your DRC results, and then click YES to view the results of this run.
5. If any DRC error exists in the design, View layer Window (VLW) and Error Layer Window (ELW) appears.



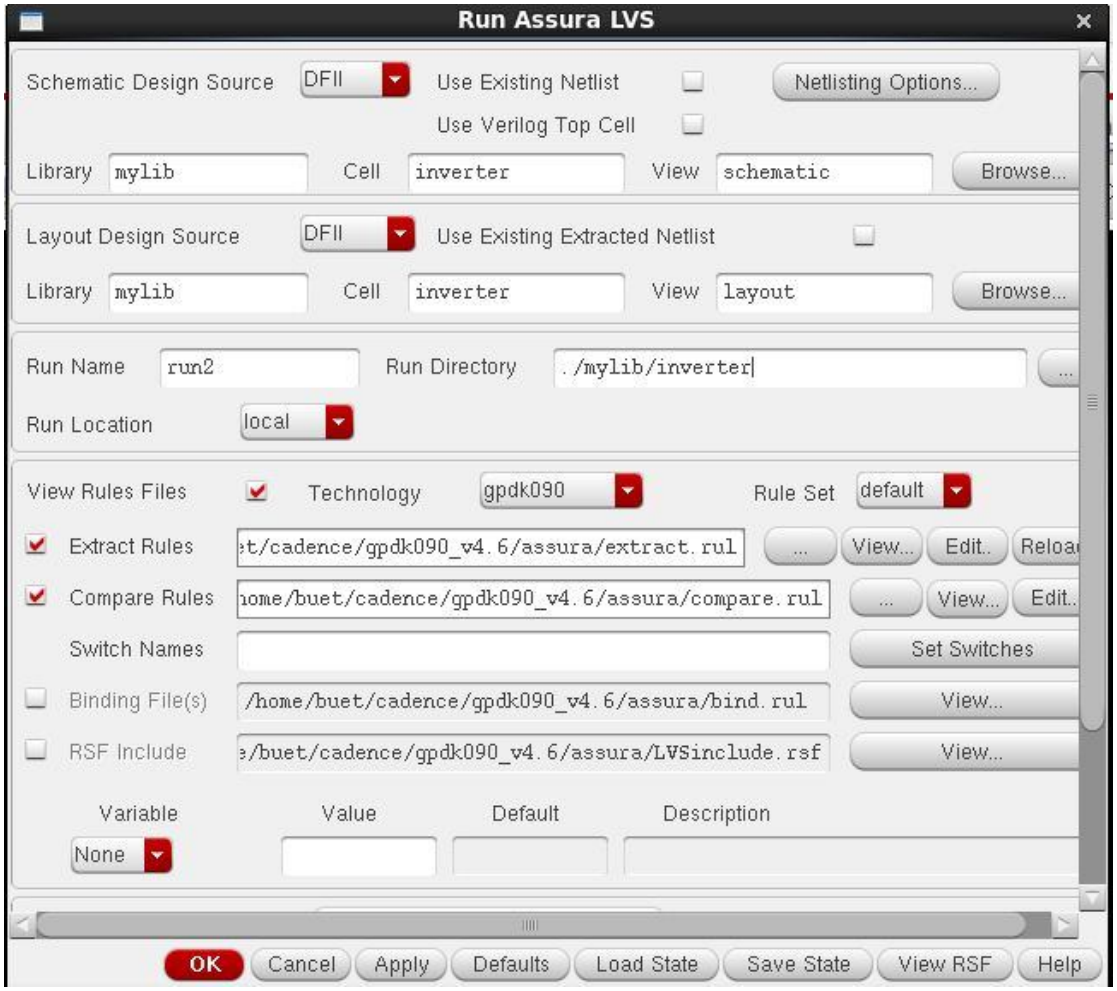
6. In ELW execute File → Preference, and ***Enable*** the ***Preview*** Button. Now press the ***Preview the next error for current rule*** arrow (left and right arrow) and see the errors in layout. To browse to next error use the up and down arrow.
7. You can refer to rule file for more information, correct all the DRC errors and Re-run the DRC.
8. If there are no errors in the layout then a dialog box appears with ***No DRC errors found*** written in it, close on Close to terminate the DRC run.

Lab 4-4 Layout versus Schematic (LVS) Check in Assura LVS

In this lab we will perform the LVS check that will compare the schematic netlist and the layout netlist.

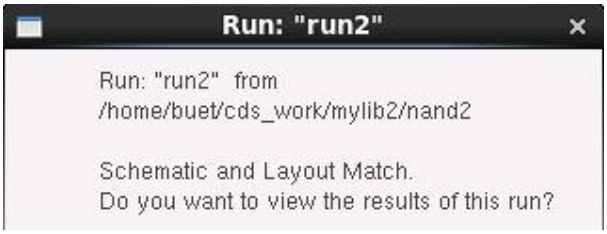
Running LVS

1. Select ***Assure → Run LVS*** from the layout window. The "Run Assura LVS" form appears. It will automatically load both the schematic and layout view of the cell.
2. Click ***OK*** to run LVS.
3. Once LVS is complete a window informs that the LVS completed successfully and ask if you want to see the results of this run. Click ***Yes*** in the window.
4. If the schematic and layout do not matches, ***LVS Debug*** window appears, and you are directed into ***LVS Debug Environment***.



In the ***LVS Debug*** window you can find the details of the mismatches and you need to correct all those mismatches and ***Re-run*** the LVS till you will be able to match the schematic with layout.

5. If the schematic and layout matches completely, you will get a window displaying ***Schematic and Layout Match***. Close the window to terminate the LVS run.



Report

Follow standard template of EEE 458 lab report and include the following also:

1. Show the print out of the layout. Measure its size. Could you achieve minimum sized layout? If not, why ?

2. What types of error did you received? What are the meanings of the error?

3. List and explain (including why the particular rule is necessary at all) all the rules that were relevant to the design of the inverter layout.

4. List some good practices for inverter layout and explain their significance.