系統晶片整合設計實驗 期末專題構想書

4108064101 杜冠廷

1. 主題：二維離散小波轉換(Discrete Time Wavelet Transform)

2. 架構：

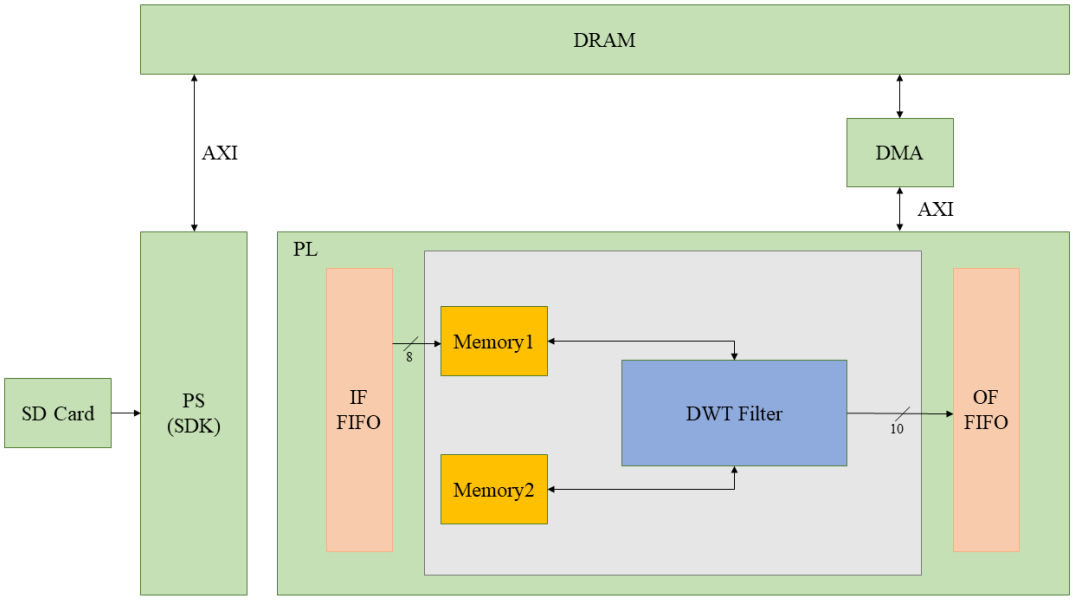

Figure 1 System Architecture

Figure 2 DWT Architecture

Step1：

將欲進行 DWT 轉換之圖片資料存入 Memory1

Step2：

經過第一次 DWT 可得到左半邊低頻、右半邊高頻之圖像並存入 Memory2

Step3：

將上一步得到的圖像從 Memory2 取出再經過 DWT 轉換後將結果存入輸出

3. DWT Filter 原理

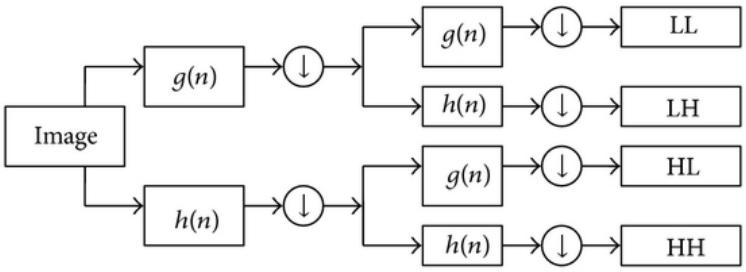

Figure 3 2D DWT Filter

$$s_j(n) = \sum_{k=0}^{L} s_{j-1}(k)g(2n-k) \quad \text{Eq1.}$$

$$s_j(n) = \sum_{k=0}^{L} s_{j-1}(k)h(2n-k) \quad \text{Eq2.}$$

將圖像分別通過低頻濾波器(Eq1.)及高頻濾波器(Eq2.)後再進行 down-sampling 以壓縮圖像資料。

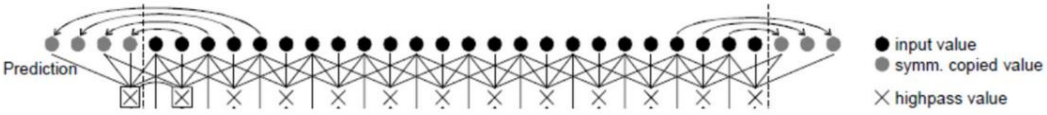

Figure 4 Symmetric extension scheme for boundary pixels

在圖像邊緣利用對稱拓展的方式處理，由於拓展時，僅用到圖像邊界的資料，因此不會增加過多資料量。同時由於拓展後的圖像在圖像邊界處是連續的，因此該方法有利於消除邊界效應。

4. 演算法實現

通過 Matlab 預先驗證原理之可行性

Figure 5 Test image

Figure 6 Image after DWT processing

5. 參考資料：

[1] M.Puttaraju, and Dr.A.R.Aswatha “FPGA Implementation of 5/3 Integer DWT for Image Compression” International Journal of Advanced Computer Science and Applications, Vol. 3, No. 10, 2012

[2] G. K. Khan and A. G. Sawant, "Spartan 6 FPGA implementation of 2D-discrete wavelet transform in Verilog HDL," 2016 IEEE International Conference on Advances in Electronics, Communication and Computer Technology (ICAECCT), 2016, pp. 139-143, doi: 10.1109/ICAECCT.2016.7942570

[3] Hardware Design of the Discrete Wavelet Transform: an Analysis of Complexity, Accuracy and Operating Frequency Dora M. Ballesteros L. 1, Diego Renza 2 and Luis Fernando Pedraza 3 Received: 28-04-2016 | Accepted: 21-10-2016 | Online: 18-11-2016 PACS: 84.40.Ua; 07.50.Qx doi:10.17230/ingciencia.12.24.6