VLSI DSP Design HW 4

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Q1

(a) Set of scheduling and projection are permissible means that

$$\begin{cases} s^t \cdot d \neq 0 \\ s^t \cdot e \geq 0 \end{cases}$$

In this question, $e = \begin{bmatrix} i \\ j \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \end{bmatrix}, \begin{bmatrix} 1 \\ 1 \end{bmatrix}, \begin{bmatrix} 0 \\ 1 \end{bmatrix}$

i. $s^t \cdot d = [1,0]\begin{bmatrix} 1 \\ 0 \end{bmatrix} = 1 \neq 0$, $s^t \cdot e = [1,0]\begin{bmatrix} 1 & 1 & 0 \\ 0 & 1 & 1 \end{bmatrix} = [1,1,0]$

all elements are not less then zero

ii. $s^t \cdot d = [0,1]\begin{bmatrix} 1 \\ 0 \end{bmatrix} = 0 \Rightarrow$ illegal

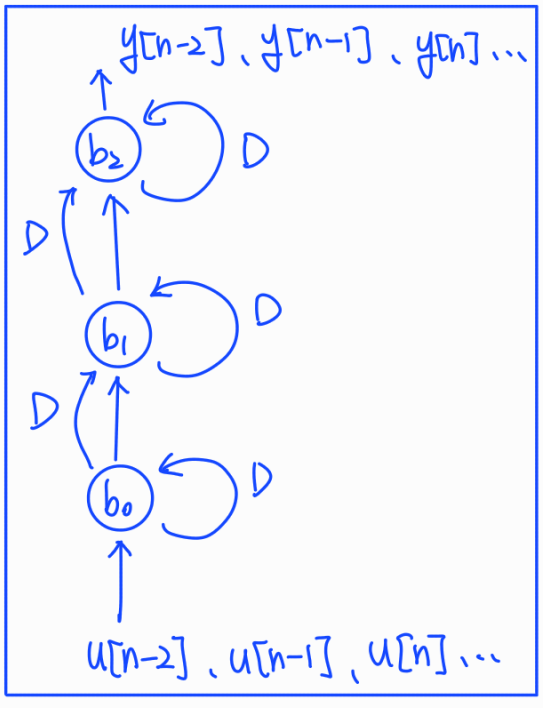
iii. $s^t \cdot d = [1,1]\begin{bmatrix} 1 \\ 0 \end{bmatrix} = 1 \neq 0$, $s^t \cdot e = [1,1]\begin{bmatrix} 1 & 1 & 0 \\ 0 & 1 & 1 \end{bmatrix} = [1,1,1]$

iv. $s^t \cdot d = [1,1]\begin{bmatrix} 0 \\ 1 \end{bmatrix} = 1 \neq 0$, $s^t \cdot e = [1,1]\begin{bmatrix} 1 & 1 & 0 \\ 0 & 1 & 1 \end{bmatrix} = [1,1,1]$

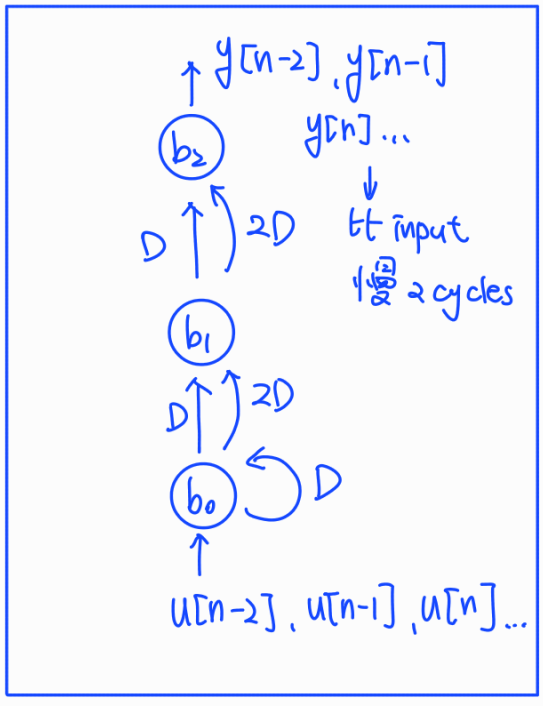
Thus, i, iii, iv are permissible. #

(b).

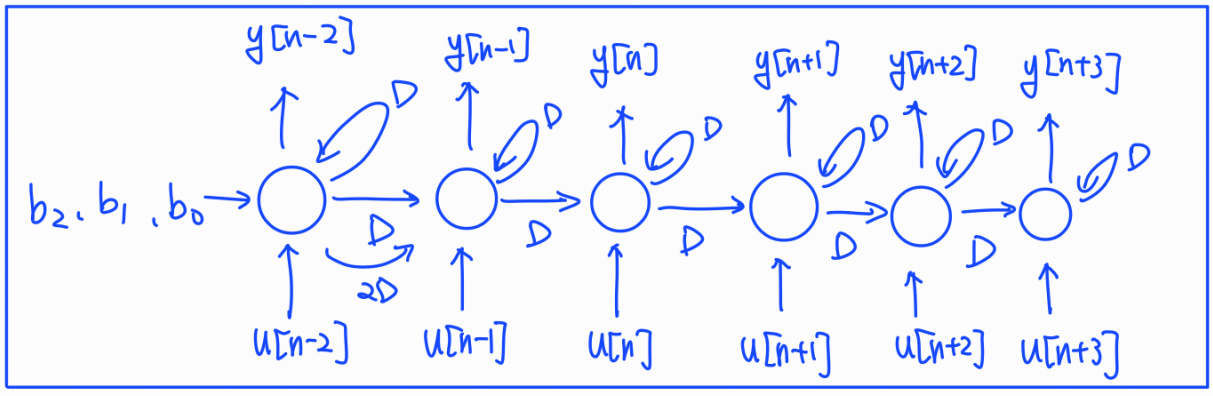
i



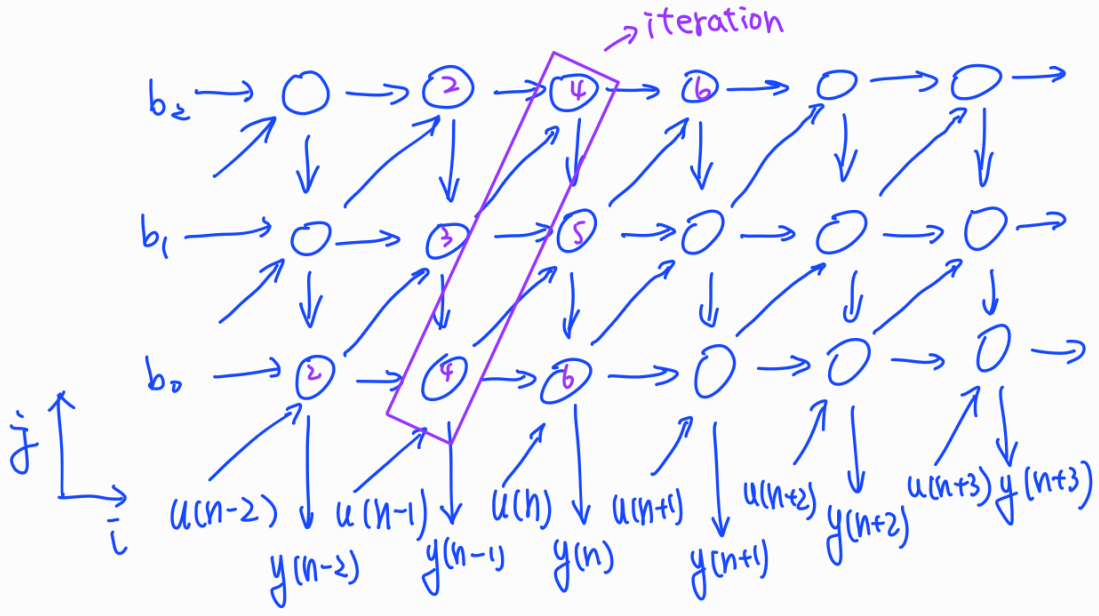
iii



iv.



(C)



Set $d=\begin{bmatrix}1\\0\end{bmatrix}$ then P will be $[0\ 1]$ because $P\cdot d=0$

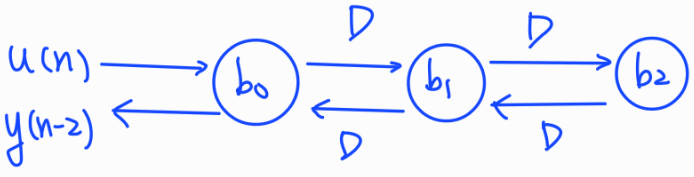
The dependence vector is $\begin{bmatrix}1\\1\end{bmatrix}, \begin{bmatrix}0\\-1\end{bmatrix}, \begin{bmatrix}1\\0\end{bmatrix}$

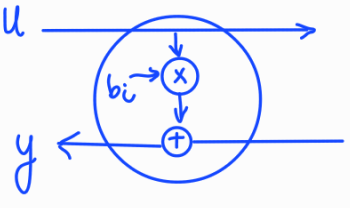
Select scheduling vector $s=\begin{bmatrix}2\\-1\end{bmatrix}$

$$\begin{cases} s^t\cdot e=[2\ -1]\begin{bmatrix}1&0&1\\1&-1&0\end{bmatrix}=[1\ 1\ 2]\geq[0\ 0\ 0] \\ s^t\cdot d=[2\ -1]\begin{bmatrix}1\\0\end{bmatrix}=2\neq 0 \end{cases}$$

from arc mapping

$$\begin{bmatrix}2&-1\\0&1\end{bmatrix}\begin{bmatrix}1&0&1\\0&-1&1\end{bmatrix}=\begin{bmatrix}2&1&1\\0&-1&1\end{bmatrix}$$





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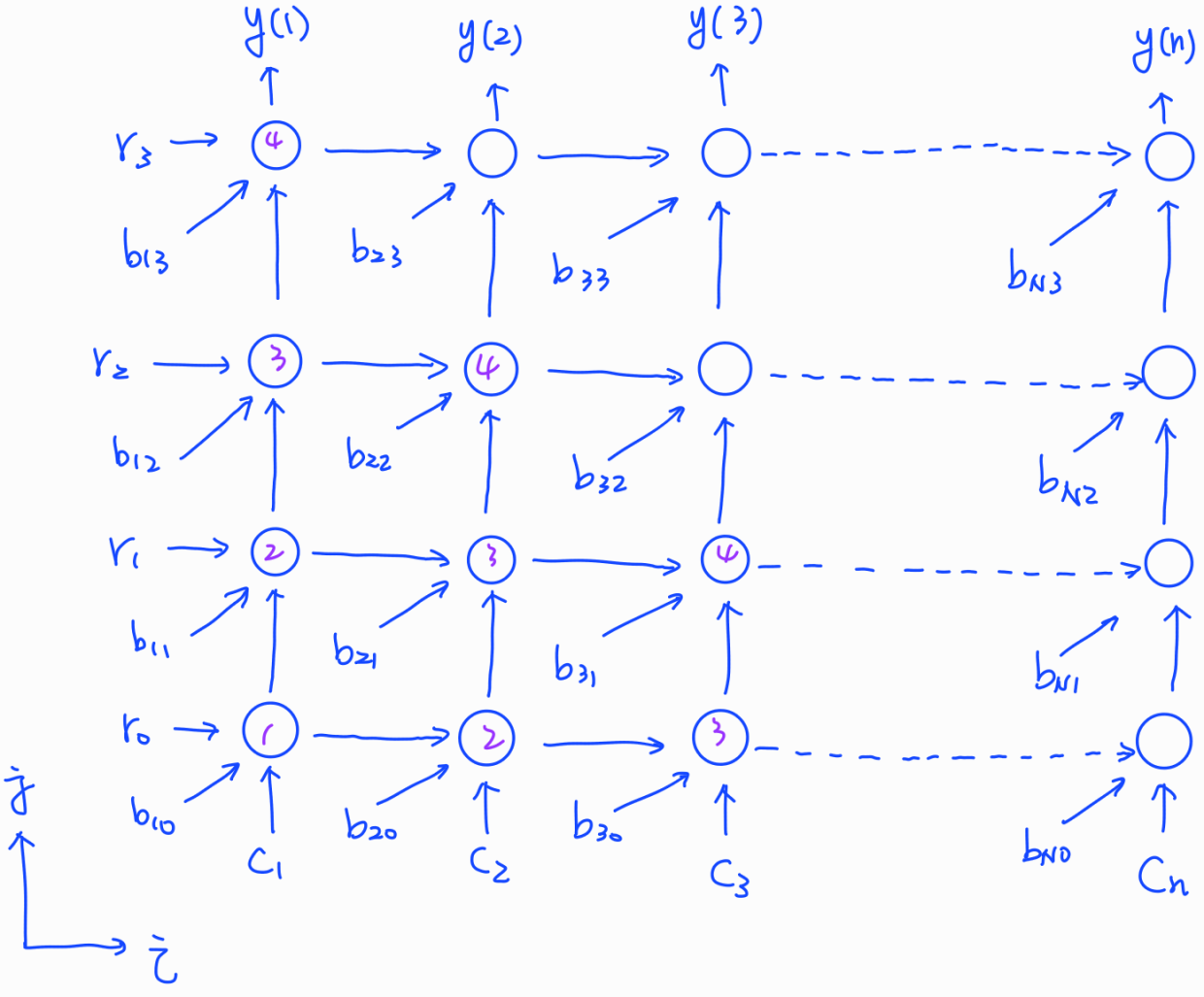
Q2.

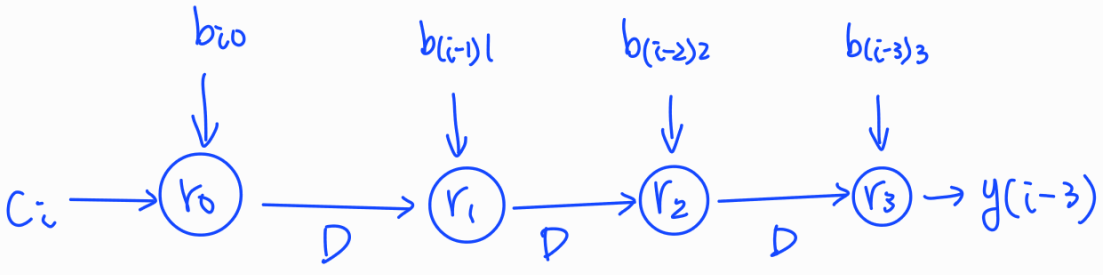
(a)

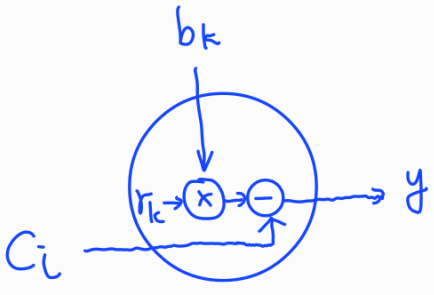


(b)

projection vector $d = \begin{bmatrix} 1 \\ 0 \end{bmatrix}$, scheduling vector $s = \begin{bmatrix} 1 \\ 1 \end{bmatrix}$

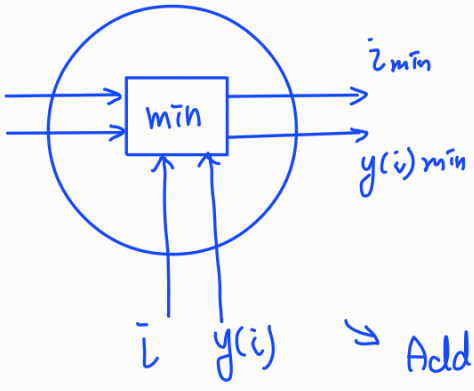
arc mapping $\begin{bmatrix} s^t \\ P \end{bmatrix} \cdot e = \begin{bmatrix} 1 & 1 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} = \begin{bmatrix} 1 & 1 \\ 0 & 1 \end{bmatrix}$ → systolic array





(c)

Comparator module



After comparing, the smaller values of y(i) and i are passed to the next stage. #

↘ Add comparator to each output terminal of DG