2023 Spring VLSI DSP Homework Assignment #5

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Part I. Data Flow Graph and mapping to hardware in the systolic array structure

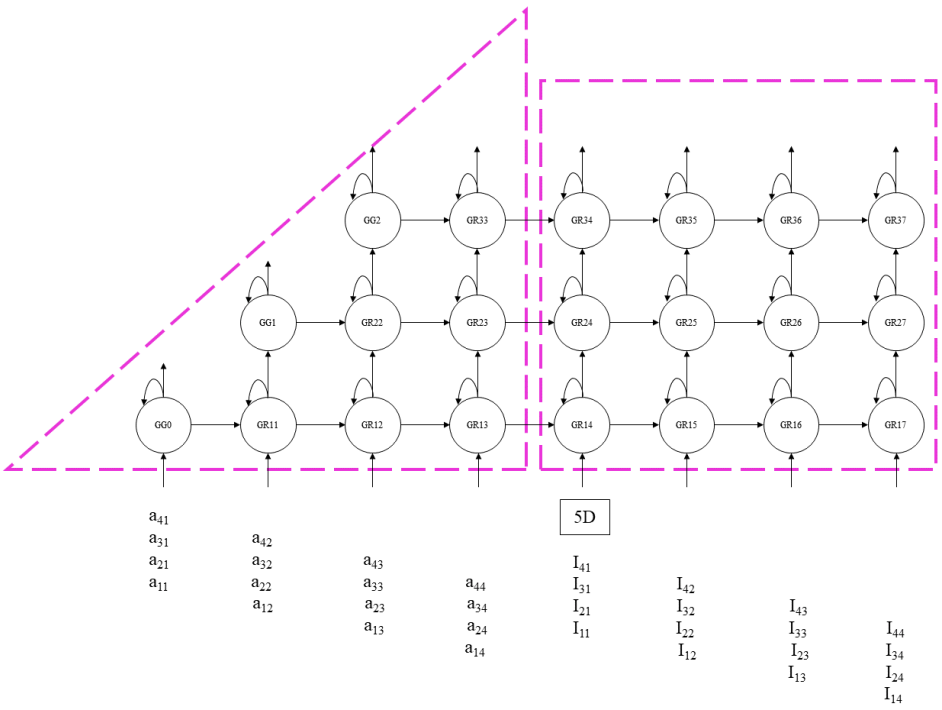

Figure 1 Data Flow Graph

Part II. Determine the word length and the length of the integral part and the fractional part

To measure the error, we utilize the quantization error value (δ) to compute and evaluate the discrepancy in the difference between the floating-point R matrix and the fixed-point R̂ matrix, as shown in Eq(2-1).

$$\delta(R) = \frac{\sqrt{\sum(r_{ij} - \hat{r}_{ij})^2}}{\sqrt{\sum {r_{ij}}^2}} \qquad \text{Eq(2-1)}$$

Similarly, we measure the error between the floating-point Q matrix and the fixed-point Q̂ matrix like Eq(2-2).

$$\delta(Q) = \frac{\sqrt{\sum(q_{ij} - \hat{q}_{ij})^2}}{\sqrt{\sum {q_{ij}}^2}} \qquad \text{Eq(2-2)}$$

After evaluating the delta function using MATLAB, we can obtain the required variable values for each fixed-point operation, such that the delta of R matrix and Q

matrix do not exceed 0.01. The variable values are as follows:

Table 1 fixed-point operation variable value

	Signedness	Word length	Fraction length	Rounding Method
R(output)	signed	12	3	Nearest
Q(output)	signed	12	11	Nearest
R(computing)	signed	20	10	Nearest
Q(computing)	signed	20	18	Nearest
K	signed	22	21	Nearest

Part III. Implementation Result

a. Verilog simulation Result vs. Matlab fixed point simulation result

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----------------------------
--                        --       |__||
--  Congratulations !!    --      / 0.0  |
--                        --    /_____   |
--  Simulation PASS!!     --   /^ ^ ^ \  |
--                        --  |^ ^ ^ ^ |w|
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```

Figure 2 verilog simulation correction

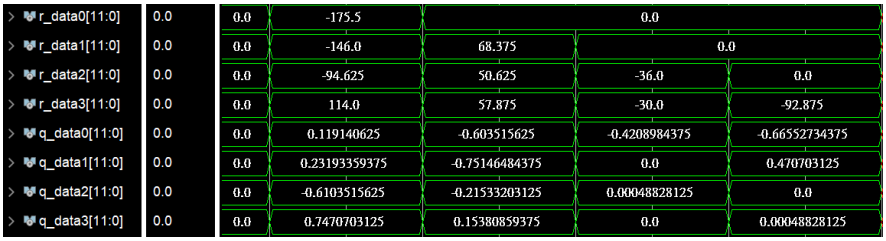


Figure 3 verilog output wave

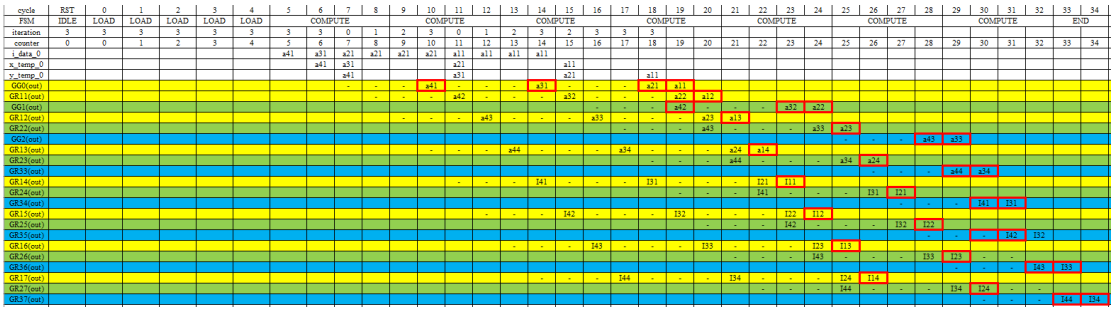
-175.5000	-146	-94.6250	114
0	68.3750	50.6250	57.8750
0	0	-36	-30
0	0	0	-92.8750

Figure 4 Matlab result of R

0.1191	0.8262	-0.4048	0.3721
-0.6035	-0.3384	-0.6958	0.1880
-0.4209	0.4014	-0.0503	-0.8105
-0.6655	0.2012	0.5898	0.4087

Figure 5 Matlab result of R

b. Timing diagram



cycle	RST	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34
FSM	IDLE	LOAD	LOAD	LOAD	LOAD	LOAD	COMPUTE				COMPUTE				COMPUTE				COMPUTE				COMPUTE				COMPUTE				COMPUTE				END	
iteration	3	3	3	3	3	3	3	3	0	1	2	3	0	1	2	3	2	3	3	3																
counter	0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34
i_data_0							a41	a31	a21	a21	a21	a21	a11	a11	a11	a11																					
x_temp_0								a41	a31				a21				a11																			
y_temp_0									a41				a31				a21			a11																
GG0(out)									-	-	-	a41	-	-	-	a31	-	-	-	a21	a11															
GR11(out)										-	-	-	a42	-	-	-	a32	-	-	-	a22	a12														
GG1(out)																			-	-	a42	-	-	-	a32	a22									
GR12(out)											-	-	-	a43	-	-	-	a33	-	-	-	a23	a13													
GR22(out)																			-	-	-	a43	-	-	-	a33	a23								
GG2(out)																											-	-	-	a43	a33					
GR13(out)												-	-	-	a44	-	-	-	a34	-	-	-	a24	a14												
GR23(out)																							a44	-	-	-	a34	a24							
GR33(out)																															a44	a34				
GR14(out)													-	-	-	I41	-	-	-	I31	-	-	-	I21	I11											
GR24(out)																					-	-	-	I41	-	-	-	I31	I21							
GR34(out)																														-	-	-	I41	I31		
GR15(out)														-	-	-	I42	-	-	-	I32	-	-	-	I22	I12										
GR25(out)																						-	-	-	I42	-	-	-	I32	I22						
GR35(out)																															-	-	-	I42	I32	
GR16(out)															-	-	-	I43	-	-	-	I33	-	-	-	I23	I13									
GR26(out)																							-	-	-	I43	-	-	-	I33	I23	-	-			
GR36(out)																															-	-	-	I43	I33	
GR17(out)																-	-	-	I44	-	-	-	I34	-	-	-	I24	I14								
GR27(out)																								-	-	-	I44	-	-	-	I34	I24	-	-		
GR37(out)																																-	-	-	I44	I34

Figure 6 System time diagram

c. Clock cycles needed to complete one QR factorization

From figure 6, we can get the system need 35 cycles to complete one QR factorization.

d. The initiation interval of two successive QR factorizations

Because the datas need to output from system, the initiation interval of two successive QR factorizations is 35 cycles.