2023 Spring VLSI DSP Homework Assignment #3

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a. Determining the word length of the filter coefficients

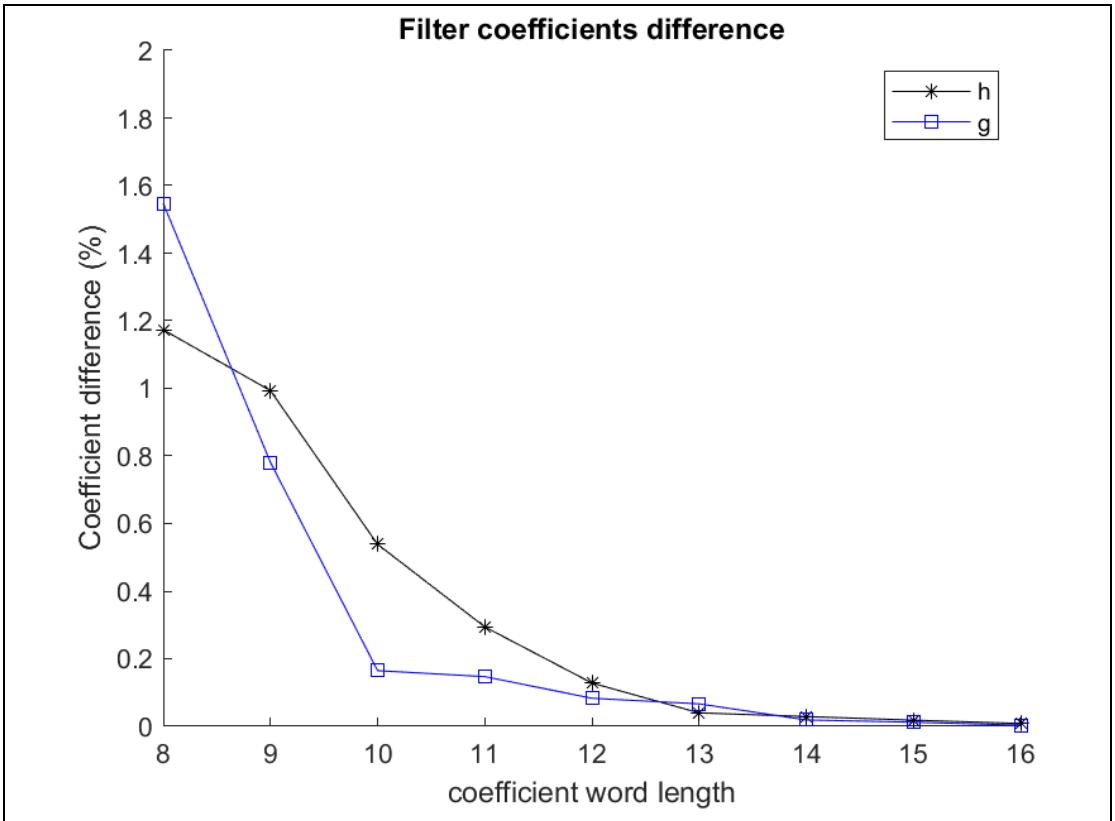
Matlab code:

Computing the filter coefficients difference between floating point and fixed point

```
clear all
close all
clc

%Filter coefficients
h = [ 0.037828455507;
     -0.023849465020;
     -0.110624404418;
      0.377402855613;
      0.852698679009;
      0.377402855613;
     -0.110624404418;
     -0.023849465020;
      0.037828455507];

g = [-0.064538882629;
      0.040689417609;
      0.418092273222;
     -0.788485616406;
      0.418092273222;
      0.040689417609;
     -0.064538882629];

W = 16;
h_error = zeros(W, 1);
g_error = zeros(W, 1);

for i = 8 : W
    h_fix = fi(h, 1, i, i-1);
    g_fix = fi(g, 1, i, i-1);
```

```
    h_error(i) = sum(abs(h - double(h_fix))) * 100;
    g_error(i) = sum(abs(g - double(g_fix))) * 100;
end

figure(1)
hold on
plot(h_error,'k*-');
plot(g_error,'bs-');
legend('h', 'g');
xlabel('coefficient word length');
ylabel('Coefficient difference (%)');
xlim([8 W]);
ylim([0 2.0]);
title('Filter coefficients difference');
hold off
```

Result:



Choosing the word length of the filter coefficients are 11.

b. Determining the word length of the filter outputs at each level

Matlab code:

```
clear all
close all
clc

%Read image
test_image = fi(imread('HW3_test_image.bmp') ,0 ,8 ,0);

%Define output result matrix
DWT_out = zeros(512,512);

%Define image process length
L = 512;

%Define fixed point precision
layer1_fixed = numerictype(true, 10, 0); % max :  504 min : -223 width(min.) = f
+  9 + 1 (f == fraction number)
layer2_fixed = numerictype(true, 11, 0); % max :  985 min : -295 width(min.) = f
+ 10 + 1 (f == fraction number)
layer3_fixed = numerictype(true, 12, 0); % max : 1952 min : -469 width(min.) = f
+ 11 + 1 (f == fraction number)

%DWT
[out_l ,out_h] = DWT_row_processing(L ,test_image ,layer1_fixed);
[out_ll ,out_hl ,out_lh ,out_hh] =
DWT_column_processing(L ,out_l ,out_h ,layer1_fixed);
DWT_out(1 : 256 ,257 : 512)   = out_hl;
DWT_out(257 : 512 ,1 : 256)   = out_lh;
DWT_out(257 : 512 ,257 : 512) = out_hh;

[out_l_2 ,out_h_2] = DWT_row_processing(256 ,out_ll ,layer2_fixed);
[out_ll_2 ,out_hl_2 ,out_lh_2 ,out_hh_2] =
DWT_column_processing(256 ,out_l_2 ,out_h_2 ,layer2_fixed);
DWT_out(1 : 128 ,129 : 256)   = out_hl_2;
```

```
DWT_out(129 : 256 ,1 : 128)   = out_lh_2;
DWT_out(129 : 256 ,129 : 256) = out_hh_2;

[out_l_3 ,out_h_3] = DWT_row_processing(128 ,out_ll_2 ,layer3_fixed);
[out_ll_3 ,out_hl_3 ,out_lh_3 ,out_hh_3] =
DWT_column_processing(128 ,out_l_3 ,out_h_3 ,layer3_fixed);
DWT_out(1 : 64 ,1 : 64)     = out_ll_3;
DWT_out(1 : 64 ,65 : 128)   = out_hl_3;
DWT_out(65 : 128 ,1 : 64)   = out_lh_3;
DWT_out(65 : 128 ,65 : 128) = out_hh_3;

%IDWT
[I_out_l_2 ,I_out_h_2] =
IDWT_column_processing(128 ,out_ll_3 ,out_lh_3 ,out_hl_3 ,out_hh_3);
[inv_pic_2] = IDWT_row_processing(128 ,I_out_l_2 ,I_out_h_2);

[I_out_l_1 ,I_out_h_1] =
IDWT_column_processing(256 ,inv_pic_2 ,out_lh_2 ,out_hl_2 ,out_hh_2);
[inv_pic_1] = IDWT_row_processing(256 ,I_out_l_1 ,I_out_h_1);

[I_out_l ,I_out_h] =
IDWT_column_processing(L ,inv_pic_1 ,out_lh ,out_hl ,out_hh);
[inv_pic] = IDWT_row_processing(L ,I_out_l ,I_out_h);

%PSNR
MSE = 0;
for i = 1 : 512
    for j = 1 : 512
         MSE = MSE + ((double(test_image(i ,j)) - double(inv_pic(i ,j))) ^ 2);
    end
end
MSE = MSE / (512 ^ 2);
PSNR = 10 * (log10((255 ^ 2) / MSE));
disp(['PSNR = ',num2str(PSNR) ,' dB']);

%Display image after processing
figure(1)
imshow(mat2gray(double(test_image)));
```

```
figure(2)
imshow(mat2gray(double(inv_pic)));
```

```
function [out_l ,out_h] = DWT_row_processing(L ,pic ,fixed_size)

%Filter coefficients
h_floating = [ 0.037828455507;
              -0.023849465020;
              -0.110624404418;
               0.377402855613;
               0.852698679009;
               0.377402855613;
              -0.110624404418;
              -0.023849465020;
               0.037828455507];

g_floating = [-0.064538882629;
               0.040689417609;
               0.418092273222;
              -0.788485616406;
               0.418092273222;
               0.040689417609;
              -0.064538882629];

%Fixed point coefficients
h = fi(h_floating ,1 ,11 ,10);
g = fi(g_floating ,1 ,11 ,10);

%Symmetric extension at picture boundary
p_l = zeros(L ,L + 8 ,'like', fi([], fixed_size));
p_l = [pic( : ,5) pic( : ,4) pic( : ,3) pic( : ,2) pic pic( : ,L - 1) pic( : ,L -
2) pic( : ,L - 3) pic( : ,L - 4)];
p_h = zeros(L ,L + 6 ,'like', fi([], fixed_size));
p_h = [pic( : ,4) pic( : ,3) pic( : ,2) pic pic( : ,L - 1) pic( : ,L - 2)
pic( : ,L - 3)];

%Compute output picture
for i = 1 : L
    %Lowpass filter
```

```
    temp_l  = conv(p_l(i , :) ,h);
    out_l(i , 1 : (L / 2)) = fi(temp_l(1 ,9 : 2 : (L + 7)) ,fixed_size);

    %Highpass filter
    temp_h  = conv(p_h(i , :) ,g);
    out_h(i , 1 : (L / 2)) = fi(temp_h(1 ,8 : 2 : (L + 6)) ,fixed_size);
end

end
```

```
function [out_ll ,out_hl ,out_lh ,out_hh] =
DWT_column_processing(L ,input_l ,input_h ,fixed_size)

%Filter coefficients
h_floating = [ 0.037828455507;
              -0.023849465020;
              -0.110624404418;
               0.377402855613;
               0.852698679009;
               0.377402855613;
              -0.110624404418;
              -0.023849465020;
               0.037828455507];

g_floating = [-0.064538882629;
               0.040689417609;
               0.418092273222;
              -0.788485616406;
               0.418092273222;
               0.040689417609;
              -0.064538882629];

%Fixed point coefficients
h = fi(h_floating ,1 ,11 ,10);
g = fi(g_floating ,1 ,11 ,10);

%Symmetric extension at picture boundary
input_l_extension_for_l = zeros(L + 8 ,L / 2 ,'like', fi([], fixed_size));
```

```
input_l_extension_for_l = [input_l(5 , : ); input_l(4 , : ); input_l(3 , : );
input_l(2 , : ); input_l; input_l(L - 1 , : ); input_l(L - 2 , : ); input_l(L -
3, : ); input_l(L - 4, : )];
input_l_extension_for_h = zeros(L + 6 ,L / 2 ,'like', fi([], fixed_size));
input_l_extension_for_h = [input_l(4 , : ); input_l(3 , : ); input_l(2 , : );
input_l; input_l(L - 1 , : ); input_l(L - 2 , : ); input_l(L - 3, : )];
input_h_extension_for_l = zeros(L + 8 ,L / 2 ,'like', fi([], fixed_size));
input_h_extension_for_l = [input_h(5 , : ); input_h(4 , : ); input_h(3 , : );
input_h(2 , : ); input_h; input_h(L - 1 , : ); input_h(L - 2 , : ); input_h(L -
3, : ); input_h(L - 4, : )];
input_h_extension_for_h = zeros(L + 6 ,L / 2 ,'like', fi([], fixed_size));
input_h_extension_for_h = [input_h(4 , : ); input_h(3 , : ); input_h(2 , : );
input_h; input_h(L - 1 , : ); input_h(L - 2 , : ); input_h(L - 3, : )];

%Compute output picture
for i = 1 : L/2
    %Lowpass filter
    temp_ll = conv(input_l_extension_for_l( : ,i) ,h);
    out_ll(1 : (L / 2) ,i) = fi(temp_ll(9 : 2 : (L + 7) ,1) ,fixed_size);

    temp_hl = conv(input_h_extension_for_l( : ,i) ,h);
    out_hl(1 : (L / 2) ,i) = fi(temp_hl(9 : 2 : (L + 7) ,1) ,fixed_size);

    %Highpass filter
    temp_lh = conv(input_l_extension_for_h( : ,i) ,g);
    out_lh(1 : (L / 2) ,i) = fi(temp_lh(8 : 2 : (L + 6) ,1) ,fixed_size);

    temp_hh = conv(input_h_extension_for_h( : ,i) ,g);
    out_hh(1 : (L / 2) ,i) = fi(temp_hh(8 : 2 : (L + 6) ,1) ,fixed_size);
end

end
```

IDWT_column_processing function and IDWT_row_processing function are the same as HW2 assignment.

Result:

```
PSNR = 51.0375 dB
```

The word length of the filter outputs at layer 1:

Data Type Mode	Fixed-point: binary point scaling
Signed or unsigned	Signed
Word Length	10
Sign bit Length	1
Integer Length	9
Fraction Length	0

The word length of the filter outputs at layer 2:

Data Type Mode	Fixed-point: binary point scaling
Signed or unsigned	Signed
Word Length	11
Sign bit Length	1
Integer Length	10
Fraction Length	0

The word length of the filter outputs at layer 3:

Data Type Mode	Fixed-point: binary point scaling
Signed or unsigned	Signed
Word Length	12
Sign bit Length	1
Integer Length	11
Fraction Length	0

c. The area of each multiplier, adder, and register

Verilog code:

Multiplier

```
module multiplier #(
parameter pic_width = 9)
(
input  signed [10:0]             coe,
input  signed [pic_width - 1:0] pic,
output signed [10 + pic_width:0] mult_result);

assign mult_result = coe * pic;

endmodule
```

Adder

```
module adder #(
parameter data_width = 20,
parameter out_width = 10)
(
input         [data_width - 1:0] data_a,
input         [data_width - 1:0] data_b,
output signed [out_width - 1:0]  result);

wire signed [data_width:0]  add_result;

assign add_result = data_a + data_b;
assign result = {add_result[data_width] ,add_result[out_width - 2:0]};

endmodule
```

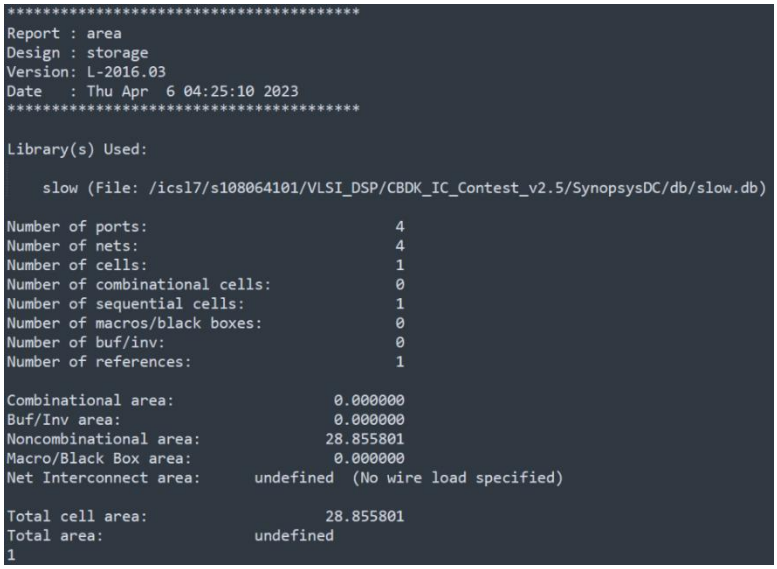
Register

```
module storage (
input      clk,
input      rst,
input      Din,
output reg Dout);

always @(posedge clk) begin
    if (!rst) begin
        Dout <= 1'b0;
    end
    else begin
        Dout <= Din;
    end
end

endmodule
```

Result:

Multiplier	
Layer 1	``` ** Report : area Design : multiplier Version: L-2016.03 Date : Fri Apr 7 15:28:54 2023 ** Library(s) Used: slow (File: /icsl7/s108064101/VLSI_DSP/CBDK_IC_Contest_v2.5/SynopsysDC/db/slow.db) Number of ports: 40 Number of nets: 316 Number of cells: 250 Number of combinational cells: 250 Number of sequential cells: 0 Number of macros/black boxes: 0 Number of buf/inv: 79 Number of references: 23 Combinational area: 2873.698269 Buf/Inv area: 268.189196 Noncombinational area: 0.000000 Macro/Black Box area: 0.000000 Net Interconnect area: undefined (No wire load specified) Total cell area: 2873.698269 Total area: undefined 1 ```
Layer 2	``` ** Report : area Design : multiplier Version: L-2016.03 Date : Fri Apr 7 15:31:50 2023 ** Library(s) Used: slow (File: /icsl7/s108064101/VLSI_DSP/CBDK_IC_Contest_v2.5/SynopsysDC/db/slow.db) Number of ports: 42 Number of nets: 334 Number of cells: 266 Number of combinational cells: 266 Number of sequential cells: 0 Number of macros/black boxes: 0 Number of buf/inv: 82 Number of references: 22 Combinational area: 3046.833069 Buf/Inv area: 278.373596 Noncombinational area: 0.000000 Macro/Black Box area: 0.000000 Net Interconnect area: undefined (No wire load specified) Total cell area: 3046.833069 Total area: undefined 1 ```
Layer 3	``` ** Report : area Design : multiplier Version: L-2016.03 Date : Fri Apr 7 15:33:47 2023 ** Library(s) Used: slow (File: /icsl7/s108064101/VLSI_DSP/CBDK_IC_Contest_v2.5/SynopsysDC/db/slow.db) Number of ports: 44 Number of nets: 366 Number of cells: 286 Number of combinational cells: 286 Number of sequential cells: 0 Number of macros/black boxes: 0 Number of buf/inv: 85 Number of references: 21 Combinational area: 3491.551866 Buf/Inv area: 288.557996 Noncombinational area: 0.000000 Macro/Black Box area: 0.000000 Net Interconnect area: undefined (No wire load specified) Total cell area: 3491.551866 Total area: undefined 1 ```

Adder	
Layer 1	``` ** Report : area Design : adder Version: L-2016.03 Date : Fri Apr 7 15:29:43 2023 ** Library(s) Used: slow (File: /icsl7/s108064101/VLSI_DSP/CBDK_IC_Contest_v2.5/SynopsysDC/db/slow.db) Number of ports: 50 Number of nets: 75 Number of cells: 27 Number of combinational cells: 27 Number of sequential cells: 0 Number of macros/black boxes: 0 Number of buf/inv: 0 Number of references: 8 Combinational area: 446.416212 Buf/Inv area: 0.000000 Noncombinational area: 0.000000 Macro/Black Box area: 0.000000 Net Interconnect area: undefined (No wire load specified) Total cell area: 446.416212 Total area: undefined 1 ```
Layer 2	``` ** Report : area Design : adder Version: L-2016.03 Date : Fri Apr 7 15:32:09 2023 ** Library(s) Used: slow (File: /icsl7/s108064101/VLSI_DSP/CBDK_IC_Contest_v2.5/SynopsysDC/db/slow.db) Number of ports: 53 Number of nets: 79 Number of cells: 28 Number of combinational cells: 28 Number of sequential cells: 0 Number of macros/black boxes: 0 Number of buf/inv: 0 Number of references: 8 Combinational area: 480.364213 Buf/Inv area: 0.000000 Noncombinational area: 0.000000 Macro/Black Box area: 0.000000 Net Interconnect area: undefined (No wire load specified) Total cell area: 480.364213 Total area: undefined 1 ```
Layer 3	``` ** Report : area Design : adder Version: L-2016.03 Date : Fri Apr 7 15:34:01 2023 ** Library(s) Used: slow (File: /icsl7/s108064101/VLSI_DSP/CBDK_IC_Contest_v2.5/SynopsysDC/db/slow.db) Number of ports: 56 Number of nets: 83 Number of cells: 29 Number of combinational cells: 29 Number of sequential cells: 0 Number of macros/black boxes: 0 Number of buf/inv: 0 Number of references: 8 Combinational area: 514.312215 Buf/Inv area: 0.000000 Noncombinational area: 0.000000 Macro/Black Box area: 0.000000 Net Interconnect area: undefined (No wire load specified) Total cell area: 514.312215 Total area: undefined 1 ```

Register	
1 bit register	
Layer 1 output	$29 \times 10 = 290\ \mu m^2/per\ pixel$
Layer 2 output	$29 \times 11 = 319\ \mu m^2/per\ pixel$
Layer 3 output	$29 \times 12 = 348\ \mu m^2/per\ pixel$

Note:

Cell Library	Cell-Based Design Kit for IC Contest 製程: TSMC 0.13um 廠商: ARM Design Kit 版本：CBDK_IC_Contest_v2.5
Synthesis tool	Design Compiler 廠商: Synopsys

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