**2023 Spring VLSI DSP Homework Assignment #5**

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**Part I. Data Flow Graph and mapping to hardware in the systolic array structure**

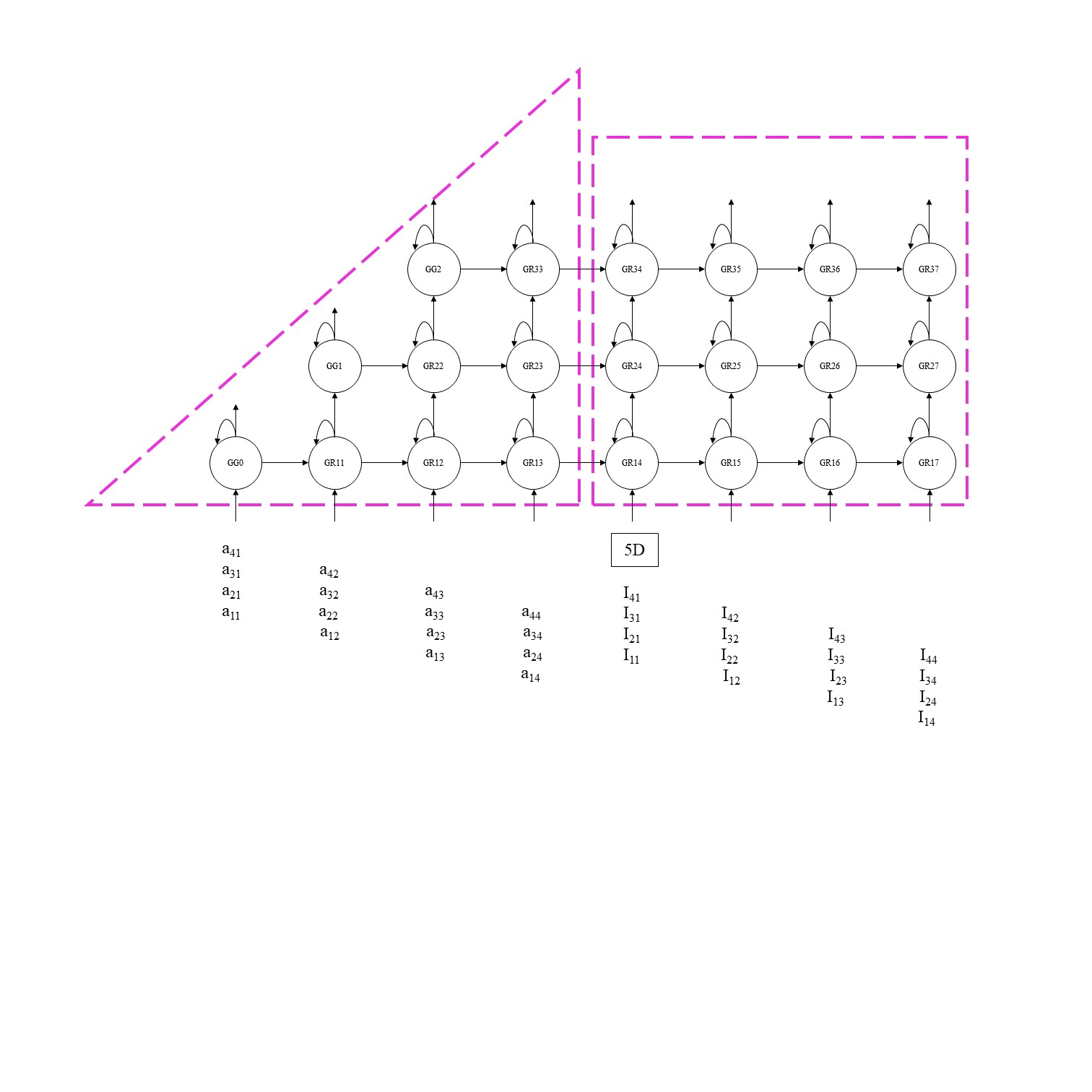


Figure 1 Data Flow Graph

**Part II. Determine the word length and the length of the integral part and the fractional part**

To measure the error, we utilize the quantization error value (δ) to compute and evaluate the discrepancy in the difference between the floating-point R matrix and the fixed-point R̂ matrix, as shown in Eq(2-1).

Eq(2-1)

Similarly, we measure the error between the floating-point Q matrix and the fixed-point Q̂ matrix like Eq(2-2).

Eq(2-2)

After evaluating the delta function using MATLAB, we can obtain the required variable values for each fixed-point operation, such that the delta of R matrix and Q matrix do not exceed 0.01. The variable values are as follows:

Table 1 fixed-point operation variable value

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | Signedness | Word length | Fraction length | Rounding Method |
| R(output) | signed | 12 | 3 | Nearest |
| Q(output) | signed | 12 | 11 | Nearest |
| R(computing) | signed | 20 | 10 | Nearest |
| Q(computing) | signed | 20 | 18 | Nearest |
| K | signed | 22 | 21 | Nearest |

**Part III. Implementation Result**

1. Verilog simulation Result vs. Matlab fixed point simulation result

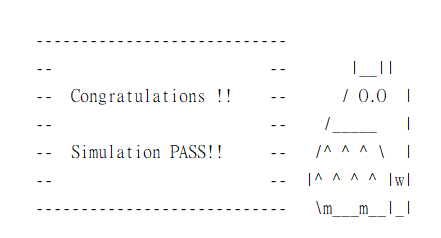


Figure 2 verilog simulation correction

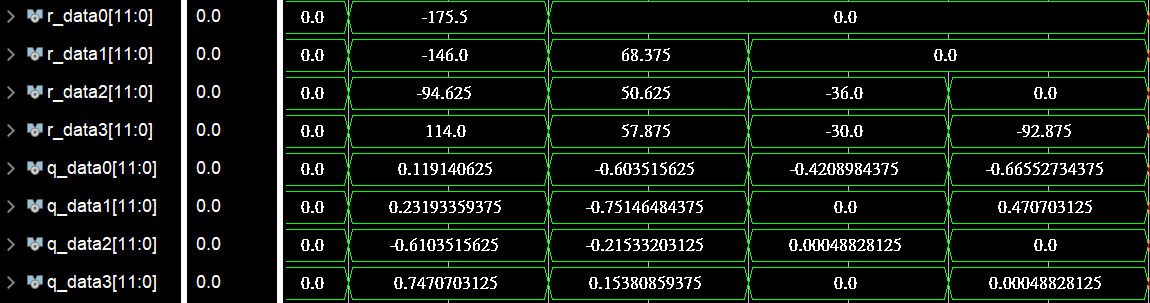


Figure 3 verilog output wave

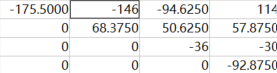


Figure 4 Matlab result of R

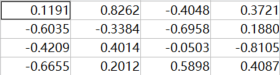


Figure 5 Matlab result of R

1. Timing diagram

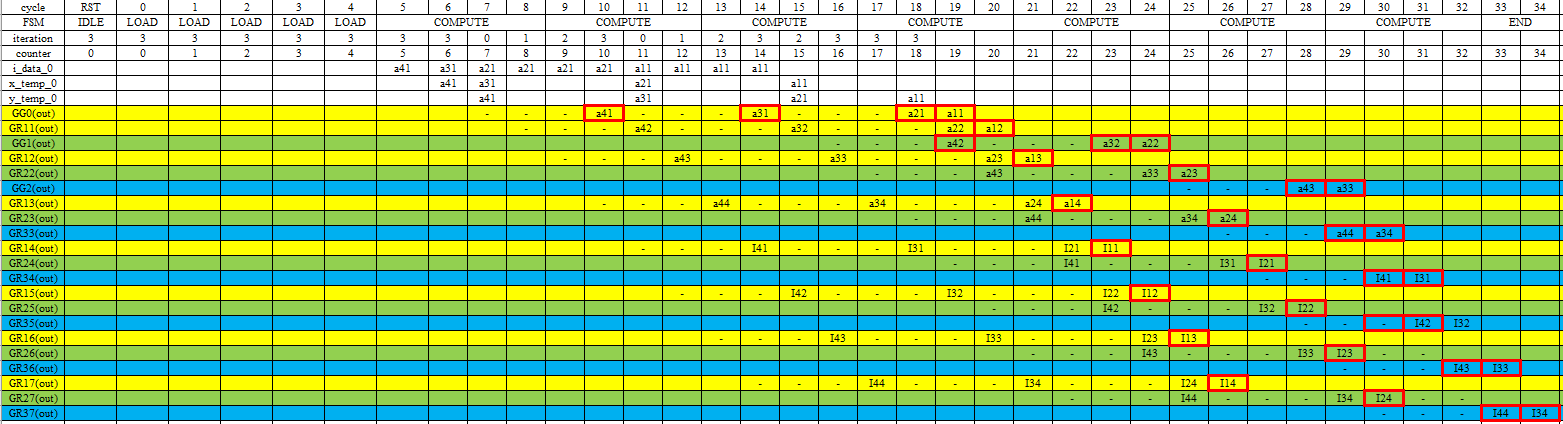


Figure 6 System time diagram

1. Clock cycles needed to complete one QR factorization

From figure 6, we can get the system need 35 cycles to complete one QR factorization.

1. The initiation interval of two successive QR factorizations

Because the datas need to output from system, the initiation interval of two successive QR factorizations is 35 cycles.