

Computer-Aided VLSI System Design

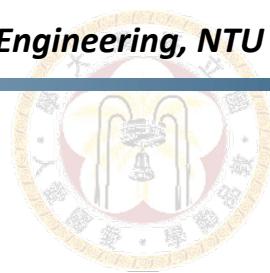
Chapter 7. Cell-based APR Flow Part2

Lecturer: Yu-Chen Lo

Graduate Institute of Electronics Engineering, National Taiwan University

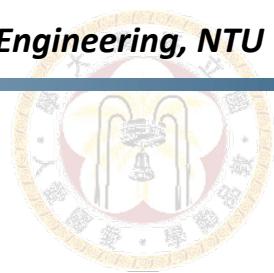


NTU GIEE

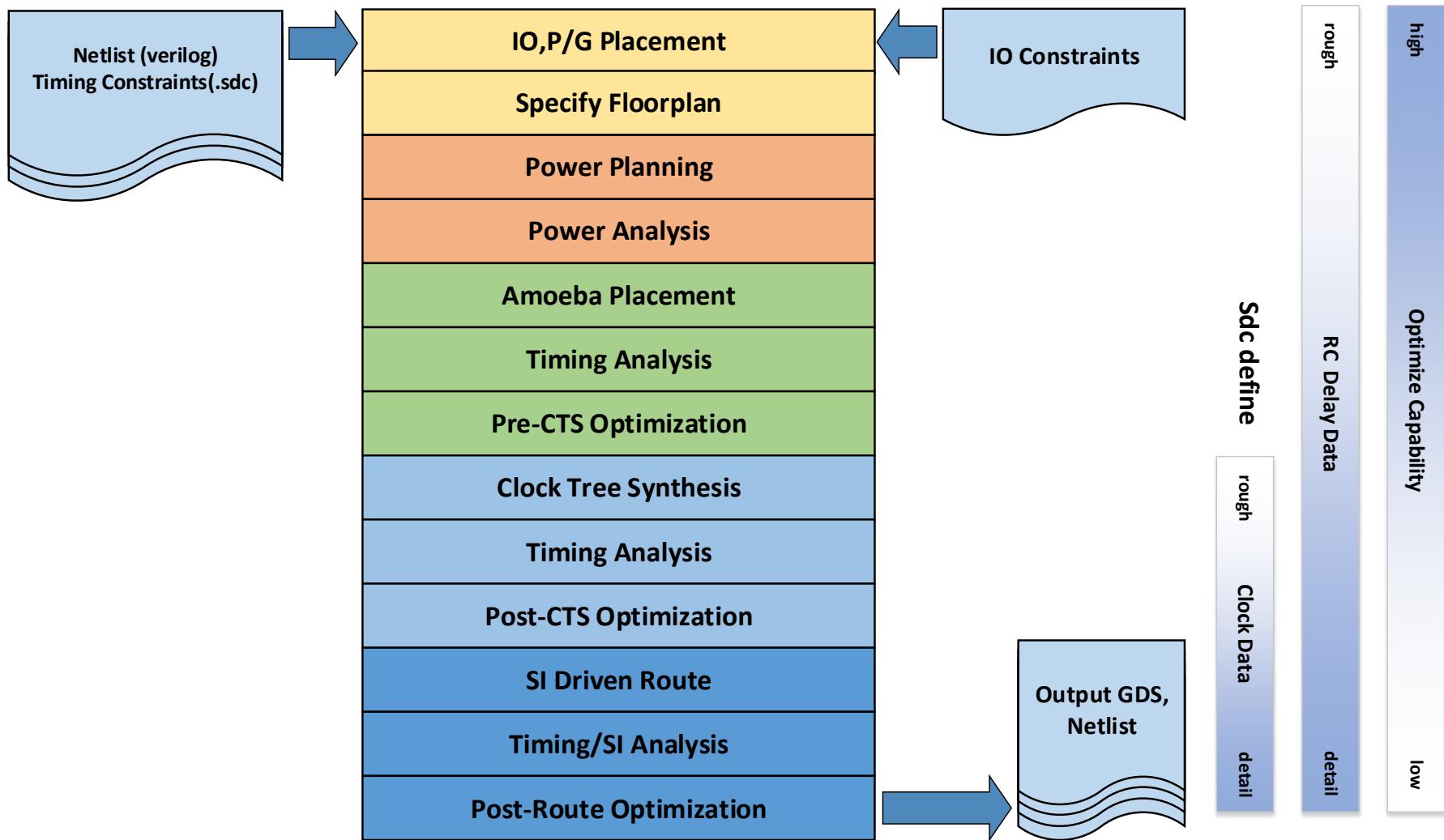


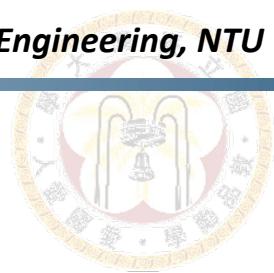
Outline

- **Automatic Place & Route – Innovus**
 - Power planning
 - Placement
 - Clock Tree Synthesis
 - Routing
- **Output data**
- **Timing Debug**
- **Engineering Change Order (ECO)**



Innovus P&R Flow

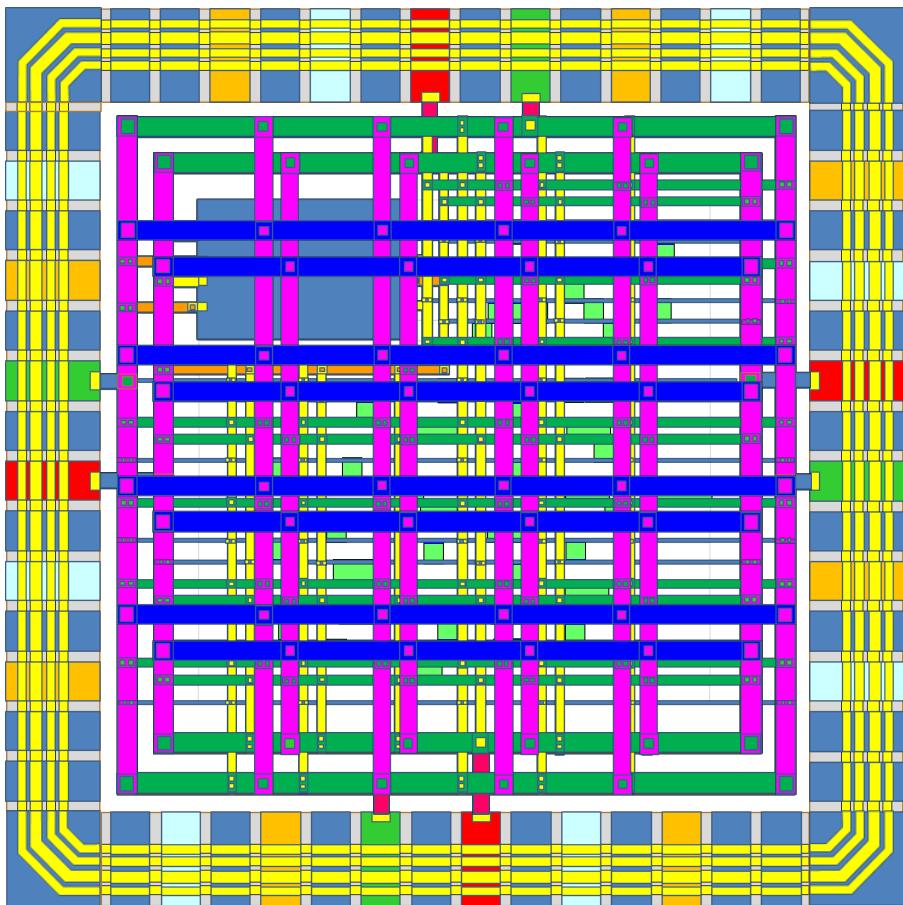


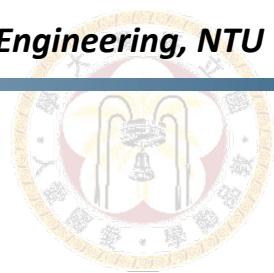


PowerPlan Order

hint: connect wider nets prior then narrow ones.

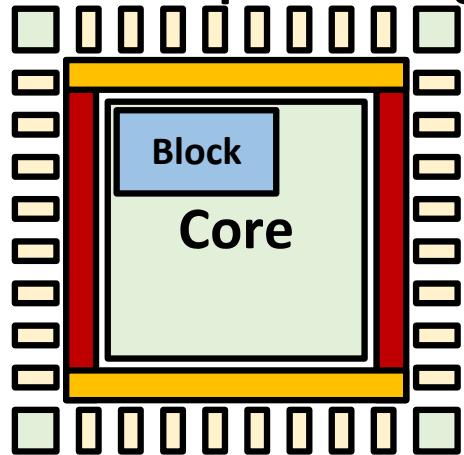
1. create power ring
2. connect pad pin
3. create block ring
4. connect block pin
5. create stripe
6. connect follow pin



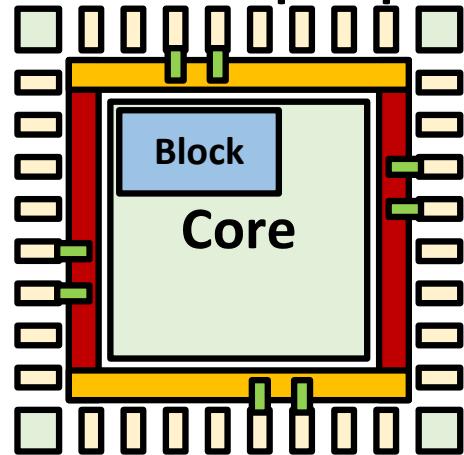


Power Planning Overview

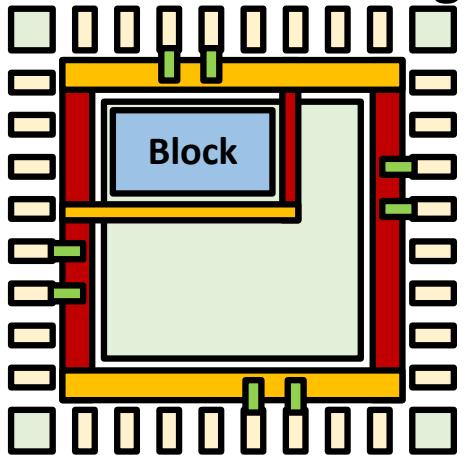
1. Create power ring



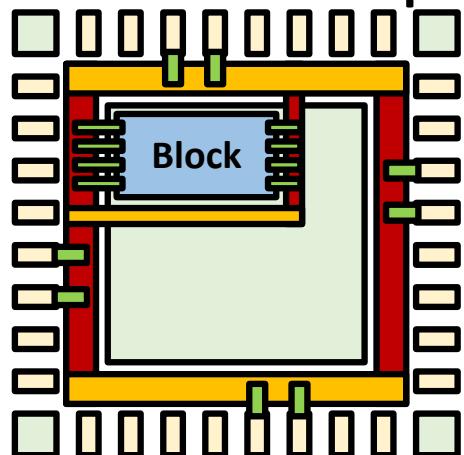
2. Connect pad pin



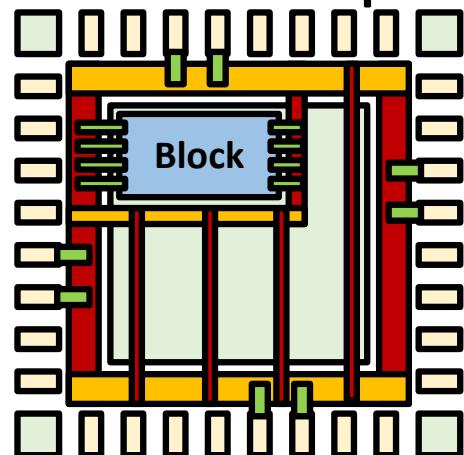
3. Create block ring



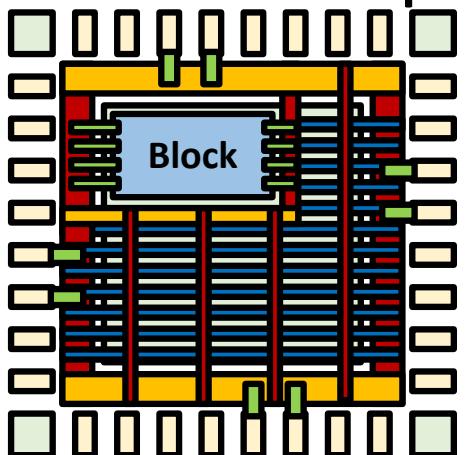
4. Connect block pin

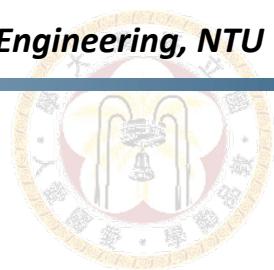


5. Create stripe



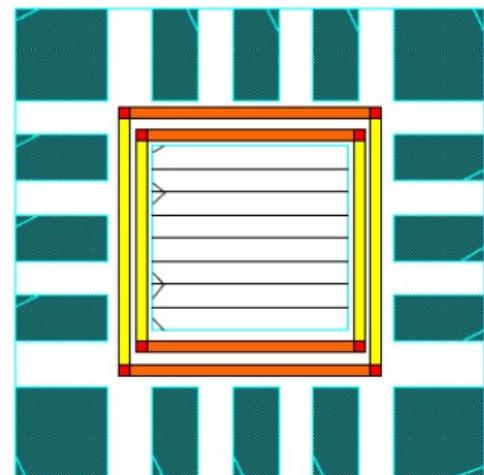
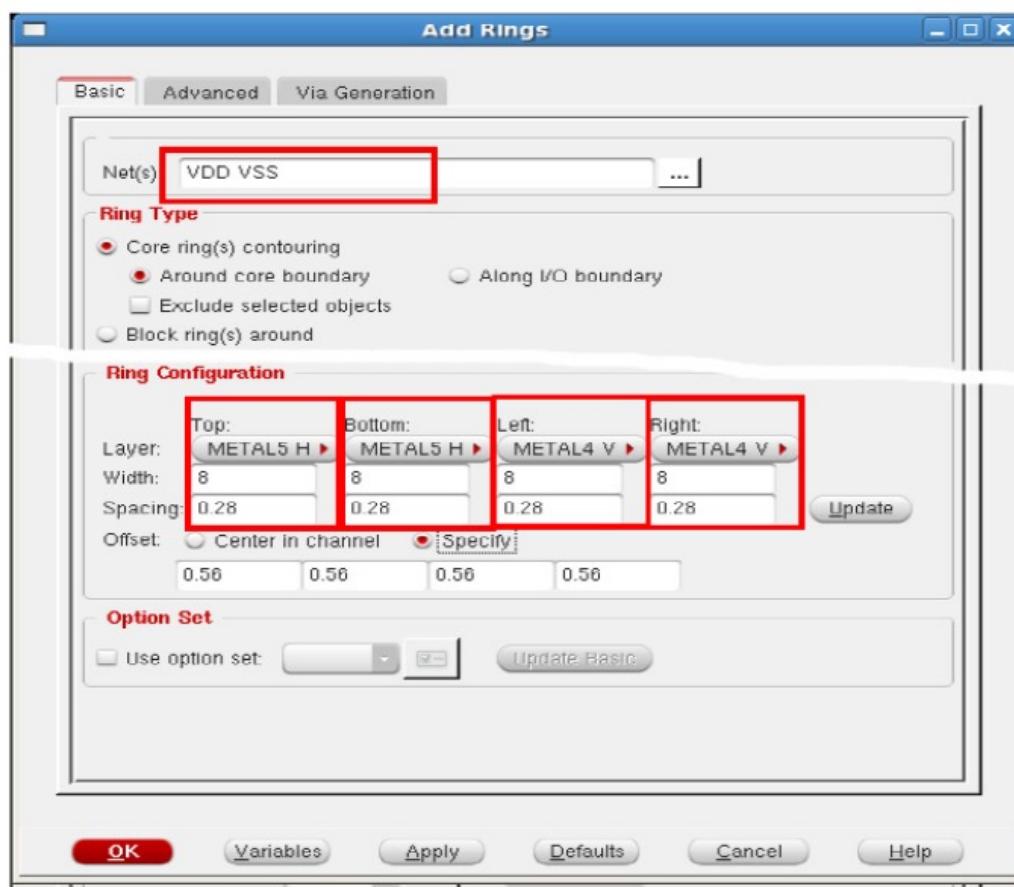
6. Connect follow pin

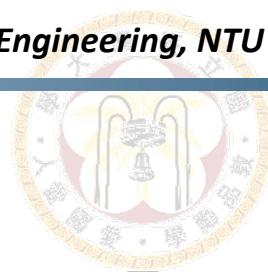




Power Planning: Add Rings

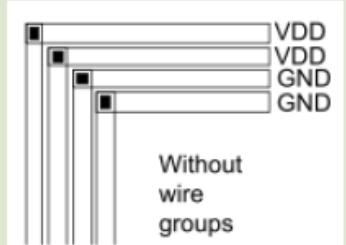
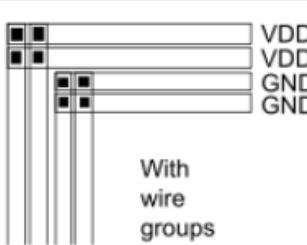
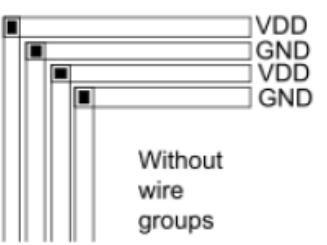
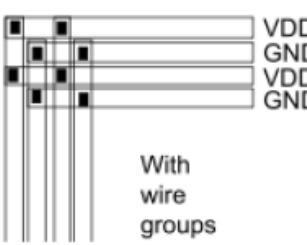
- **Power -> Power Planning -> Add Rings**
- Use wire group and interleaving to avoid slot DRC error

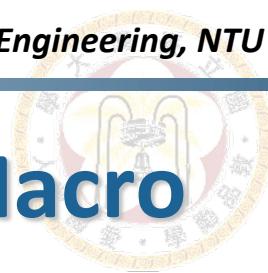




Power Planning: Power Ring

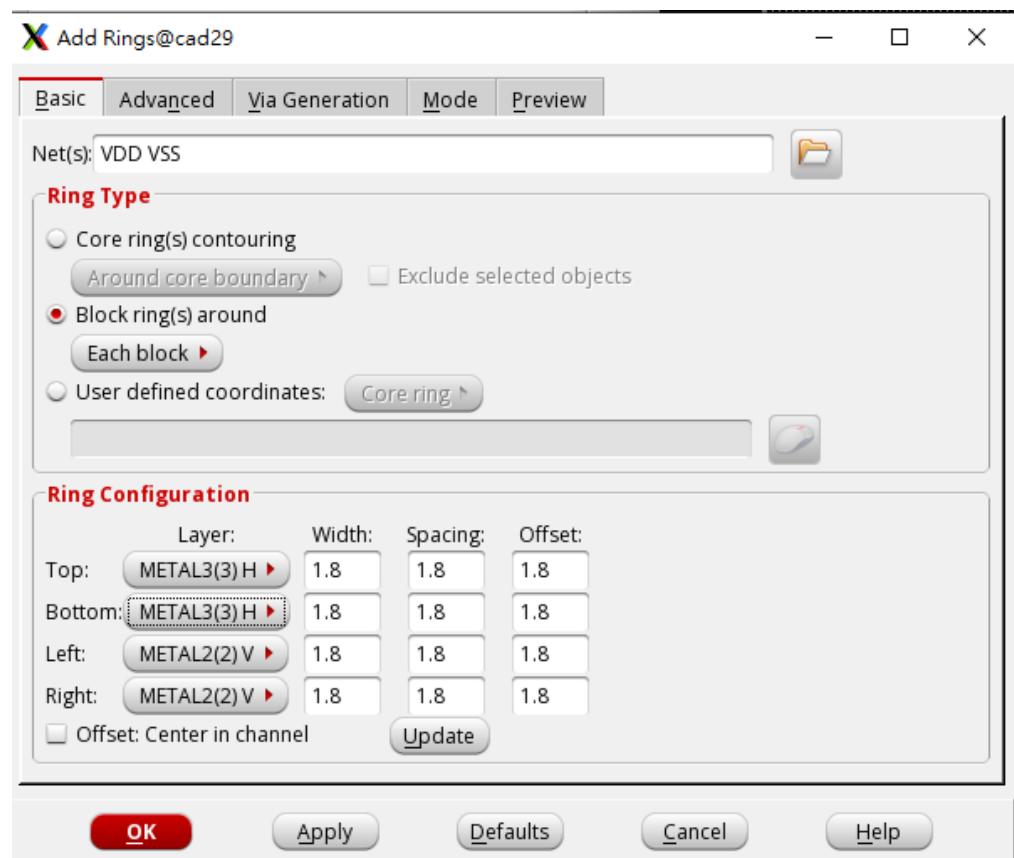
- Supply voltage for the core evenly by power pads
- Interleaving and wire group
 - To increase the coupling capacitance of power rings
 - Thus reduce the power noise

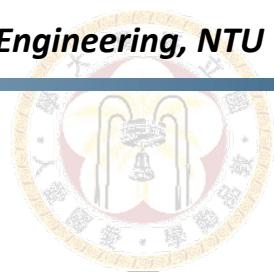
	Without Wire group	With Wire group
Without Interleaving	 <p>Without wire groups</p>	 <p>With wire groups</p>
Interleaving	 <p>Without wire groups</p>	 <p>With wire groups</p>



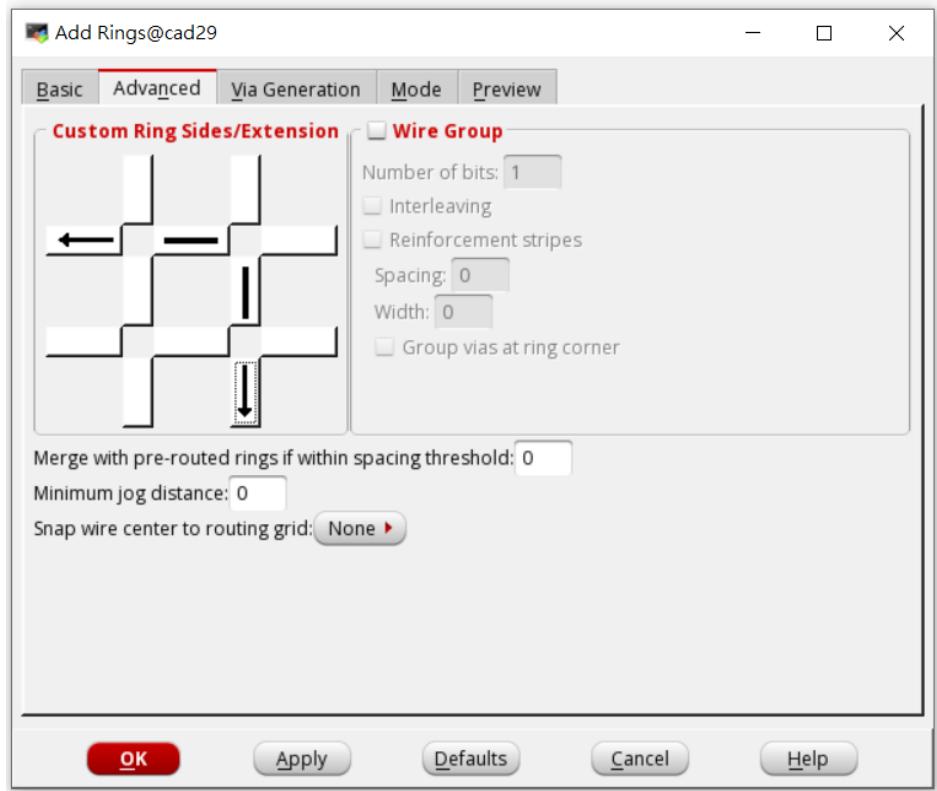
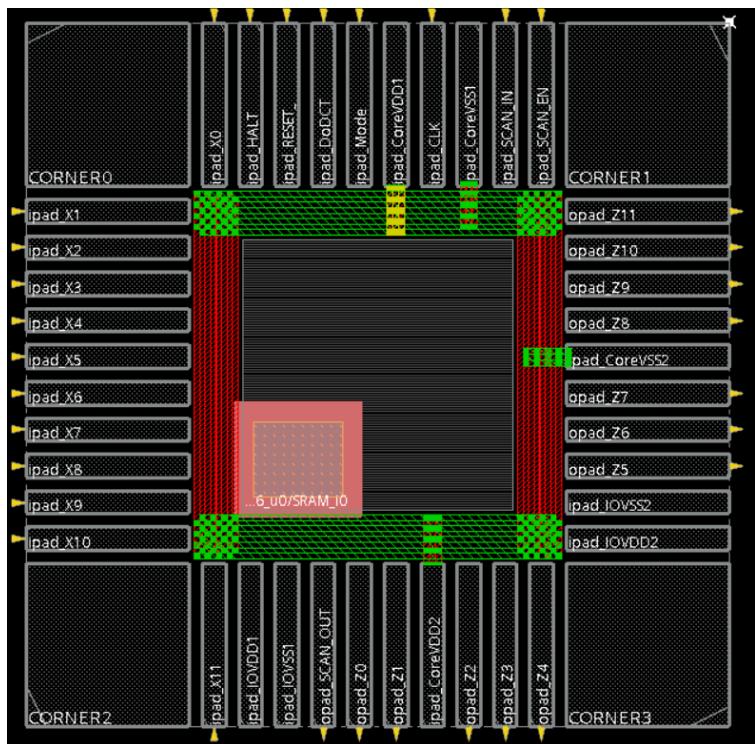
Power Planning: Block Ring for Hard Macro

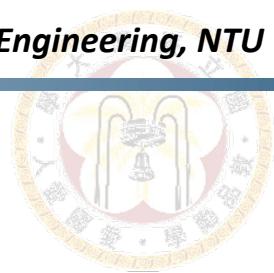
- Supply voltage for hard macros
- Add block ring
 - Specify nets
 - Block ring around
 - Specify metals
 - Width, offset
 - Extension
 - Wiregroups



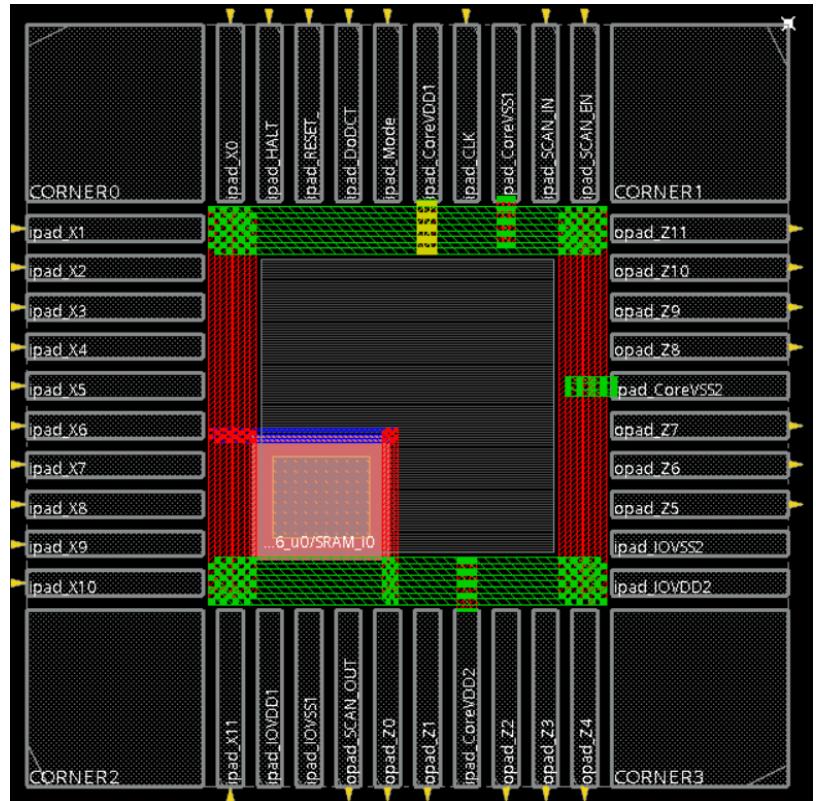
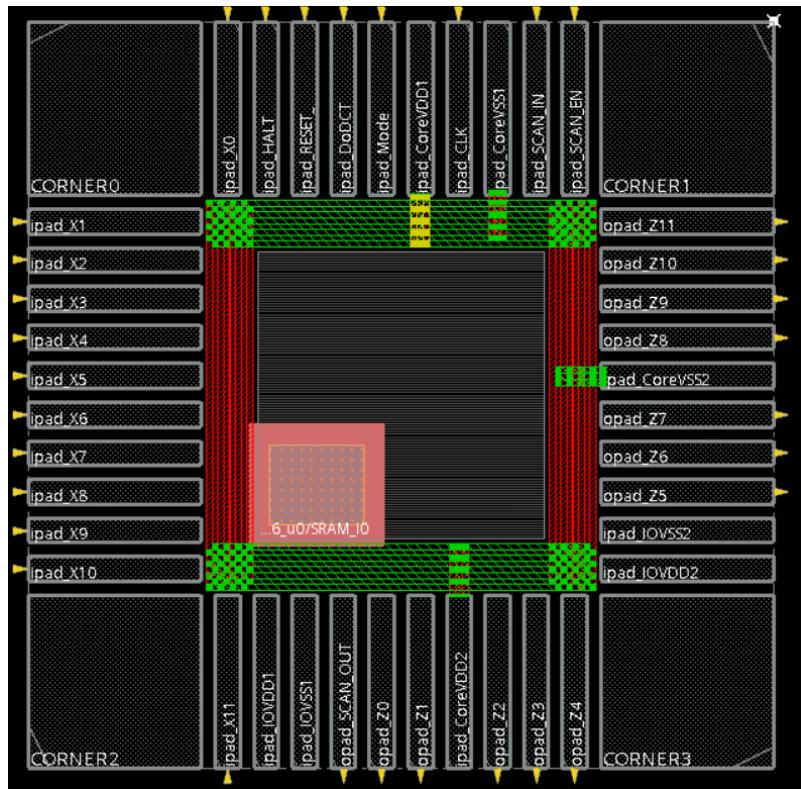


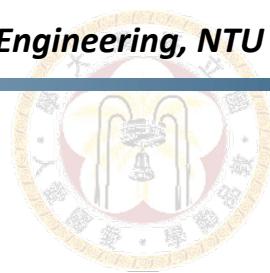
Specify Block Ring Extension





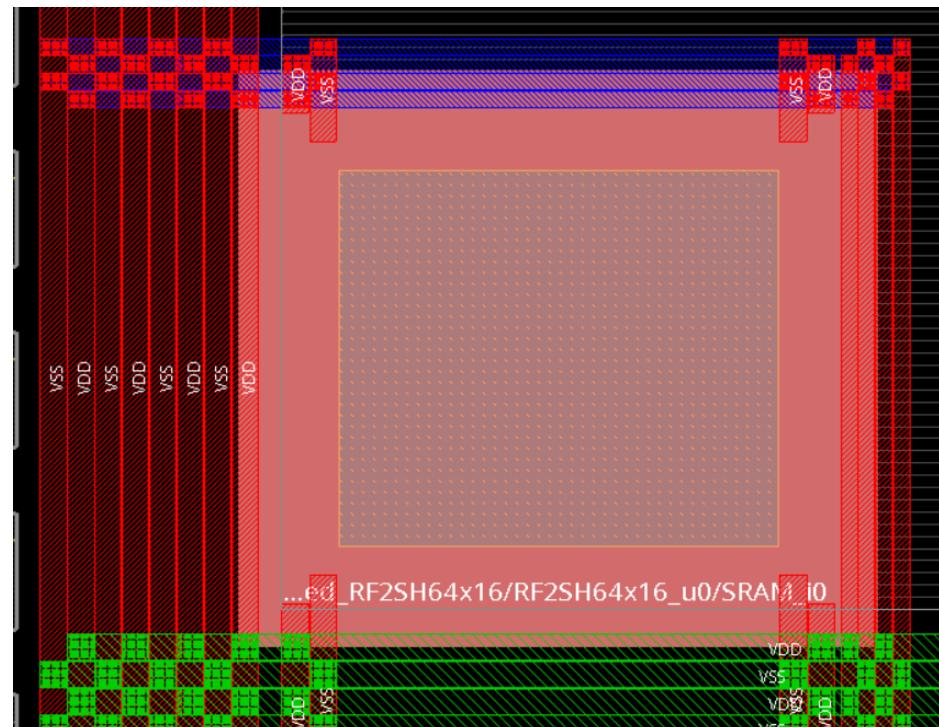
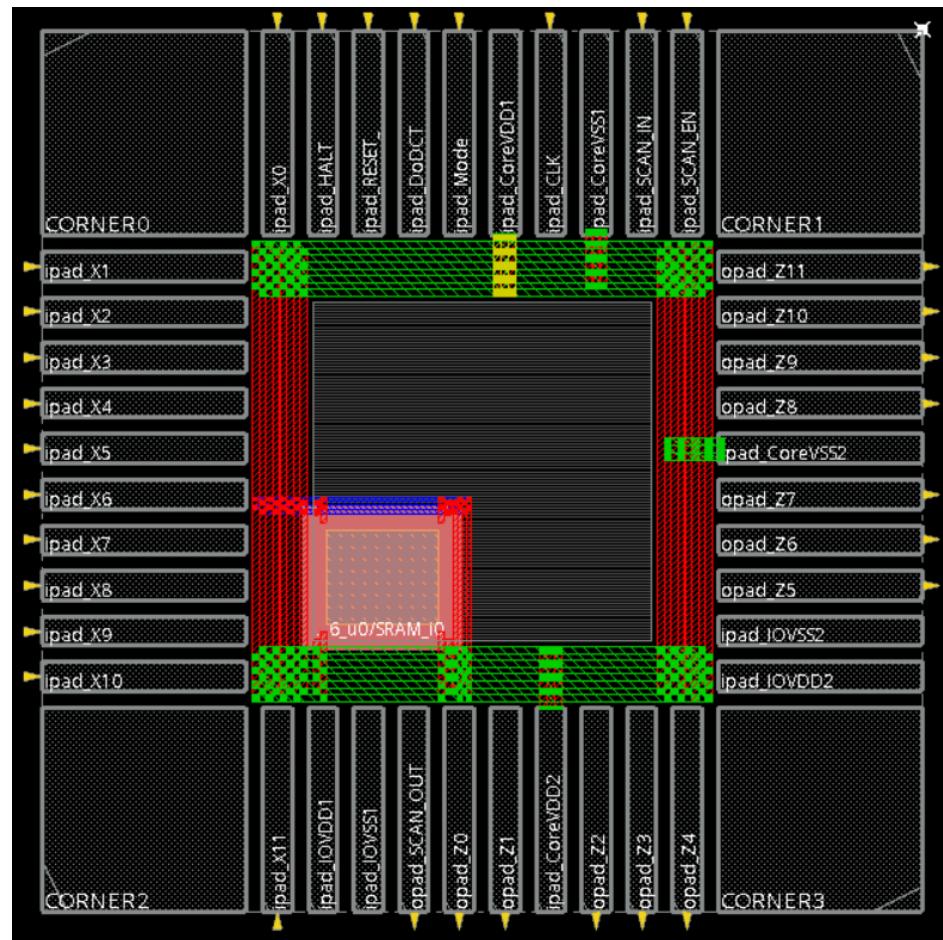
Specify Block Ring Extension

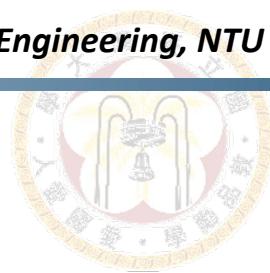




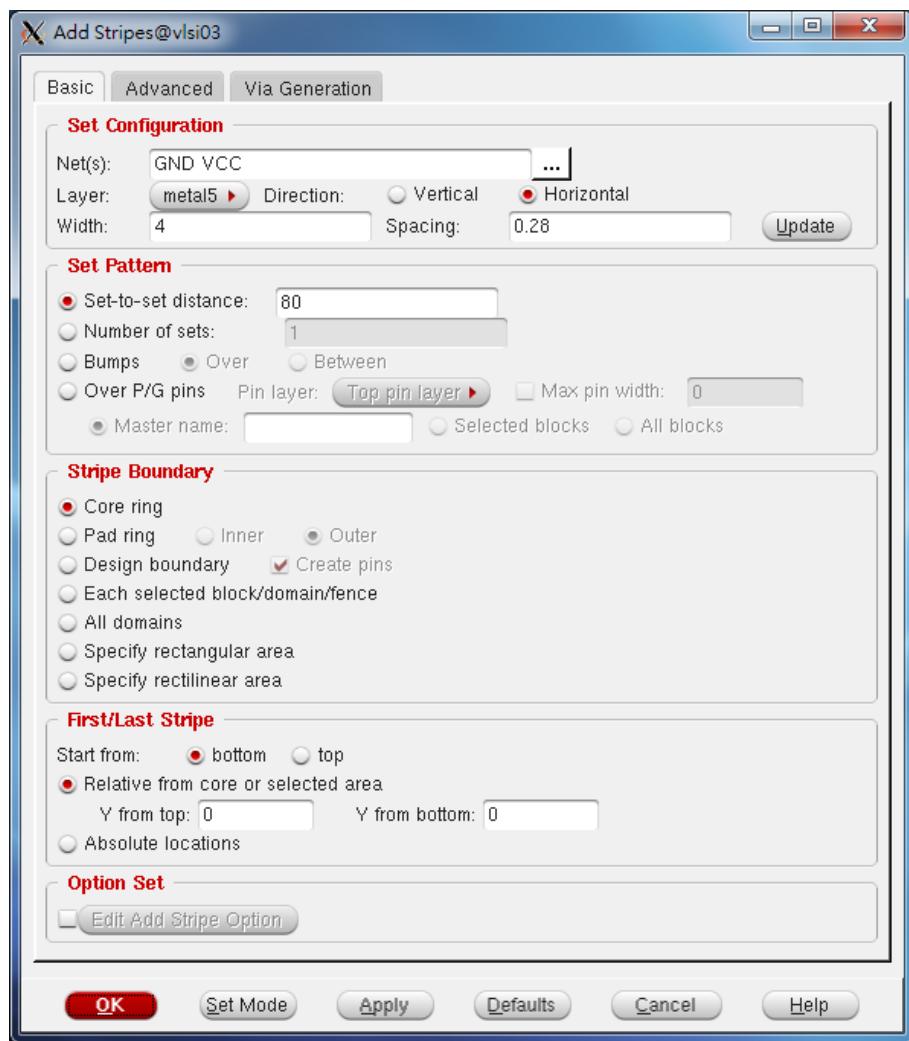
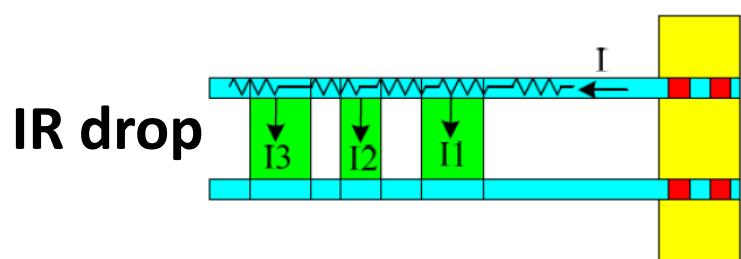
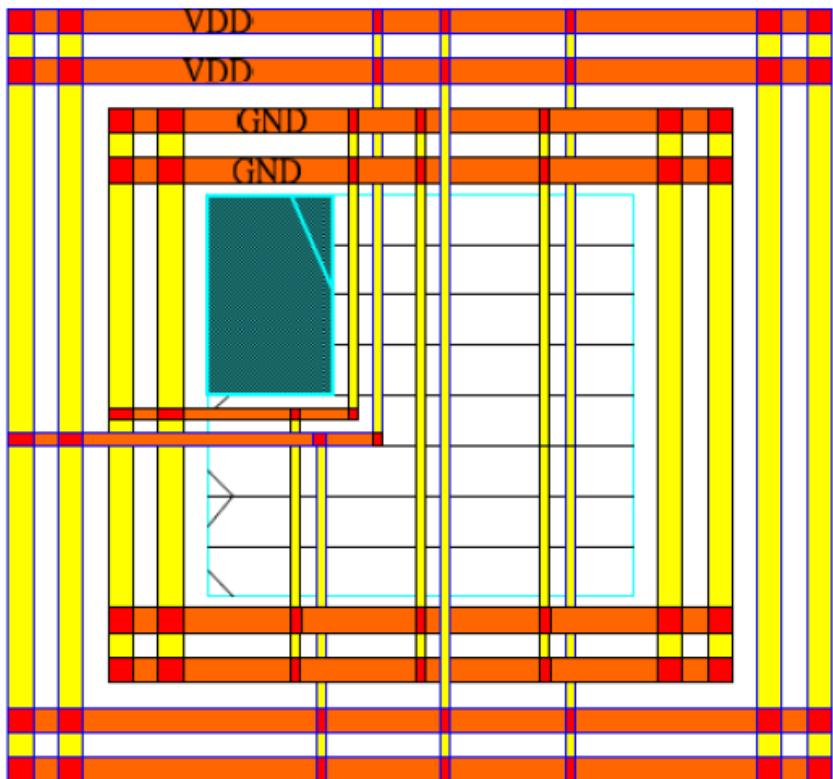
Power Planning: Block Pin

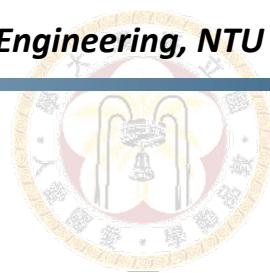
- Connect block rings and power rings





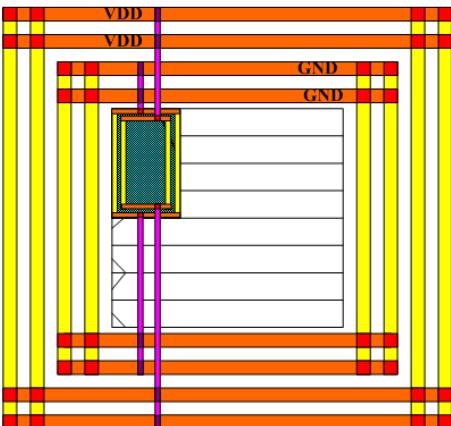
Power Planning: Add Stripes





Connect block power pin

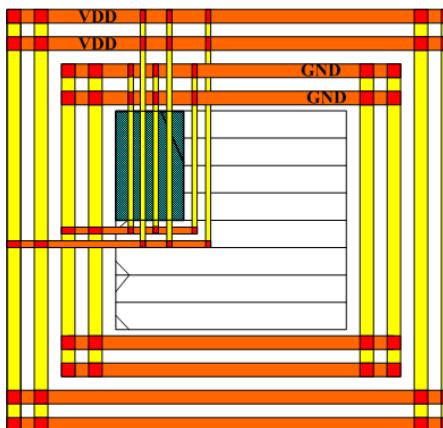
ring type:



add stripes

- set to set distance

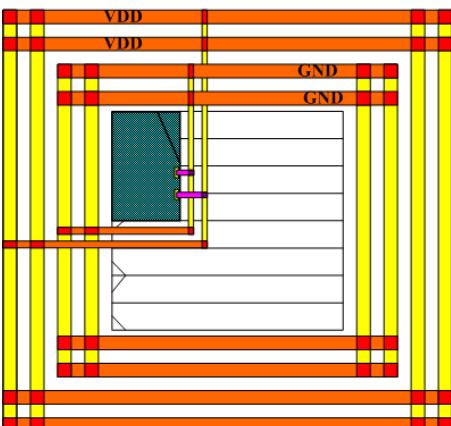
rail type (vertical) :



add stripes

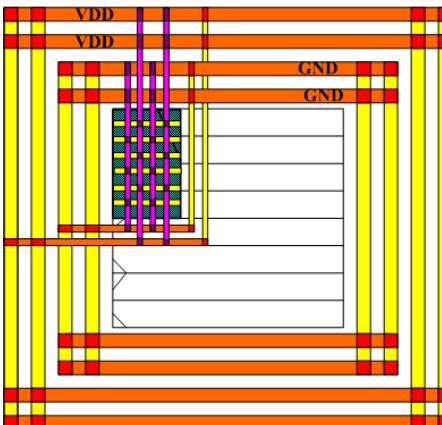
- over p/g pins

pin type:



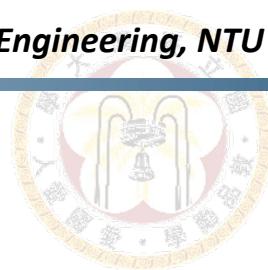
Sroute - block

rail type (horizontal) :



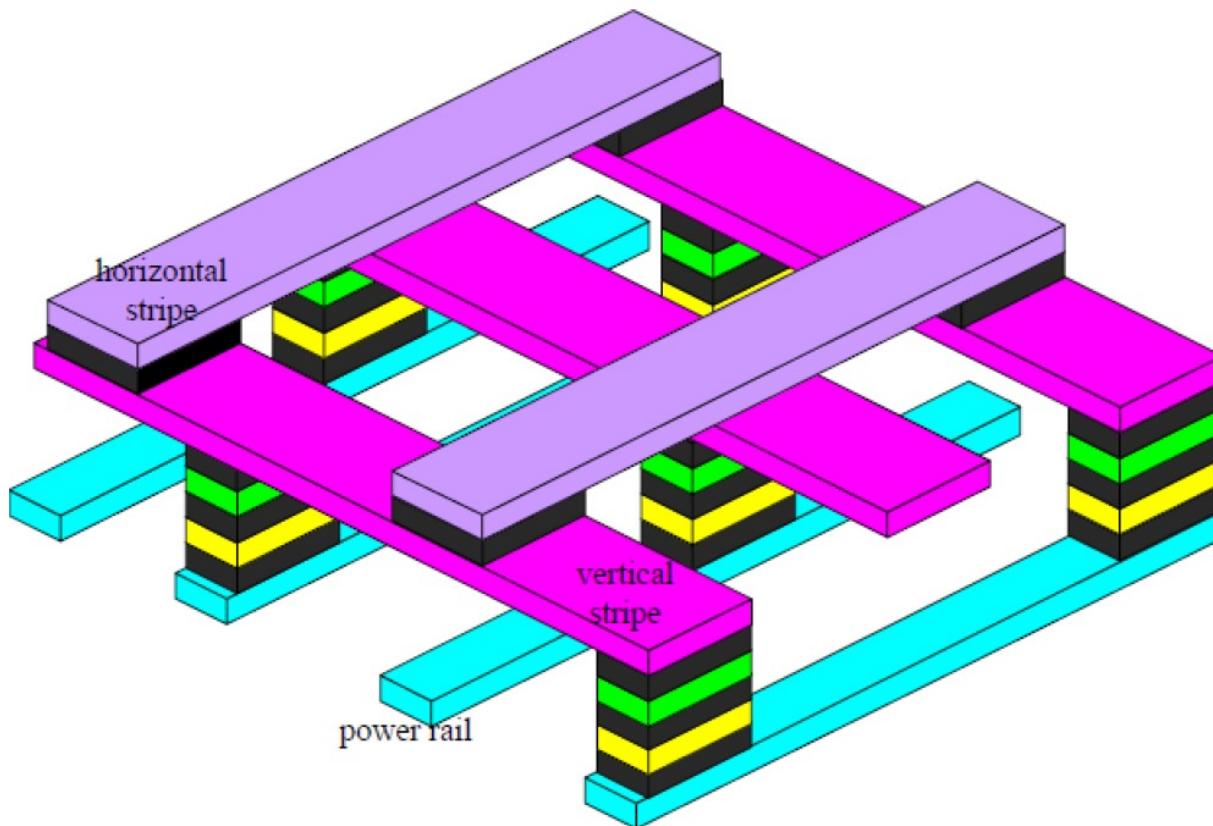
add stripes

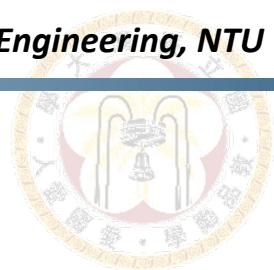
- set to set distance



Power Planning: Power Stripes

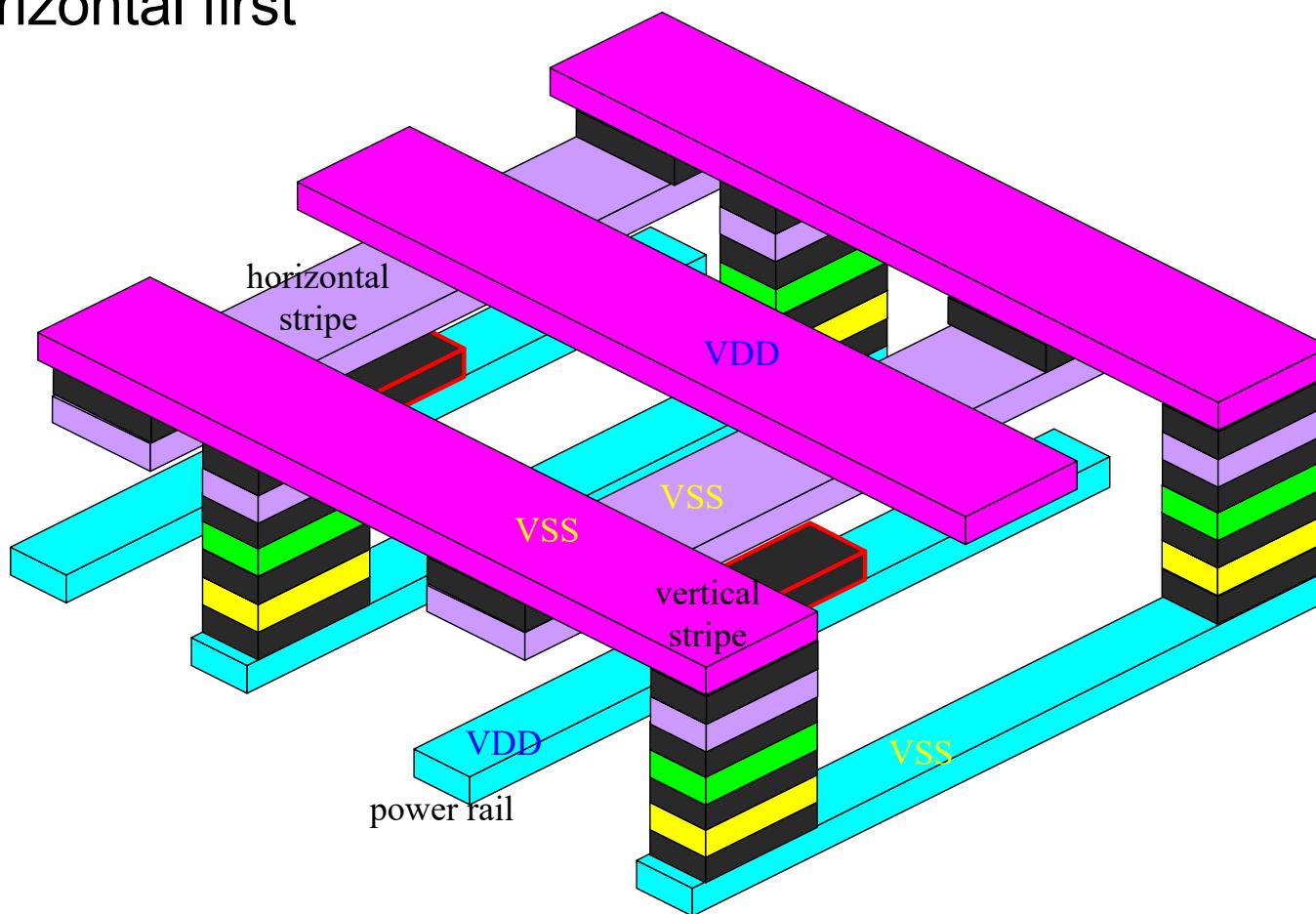
- Supply voltage for hard macros and follow pins by power rings
- Connection should not be mixed with pad pins

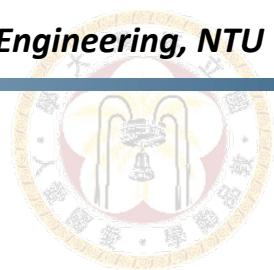




Stripes – Wrong Order

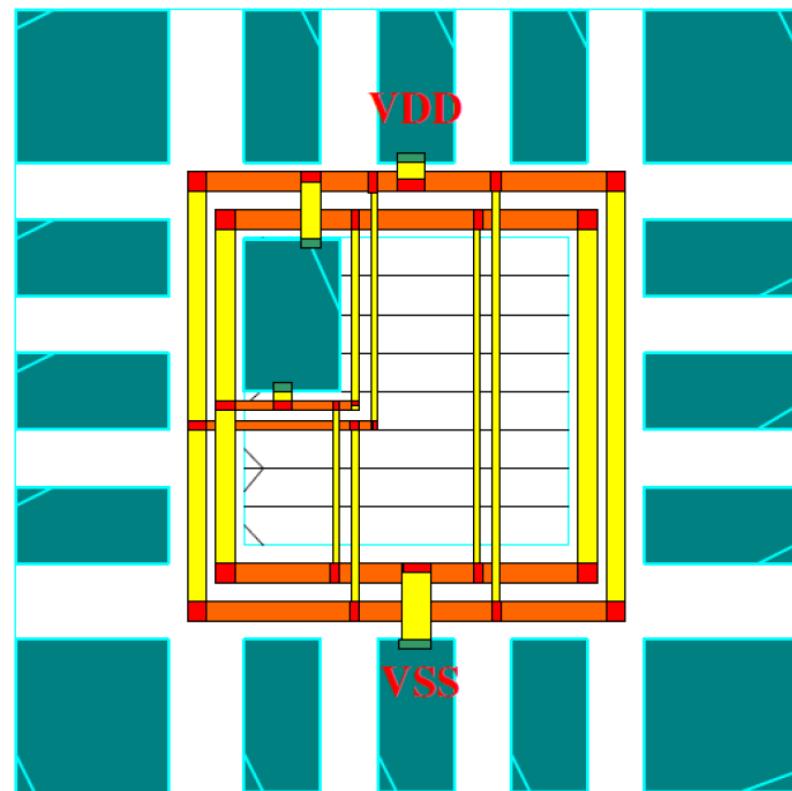
horizontal first

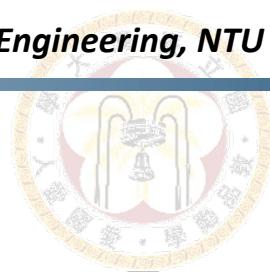




Special Route (SRoute)

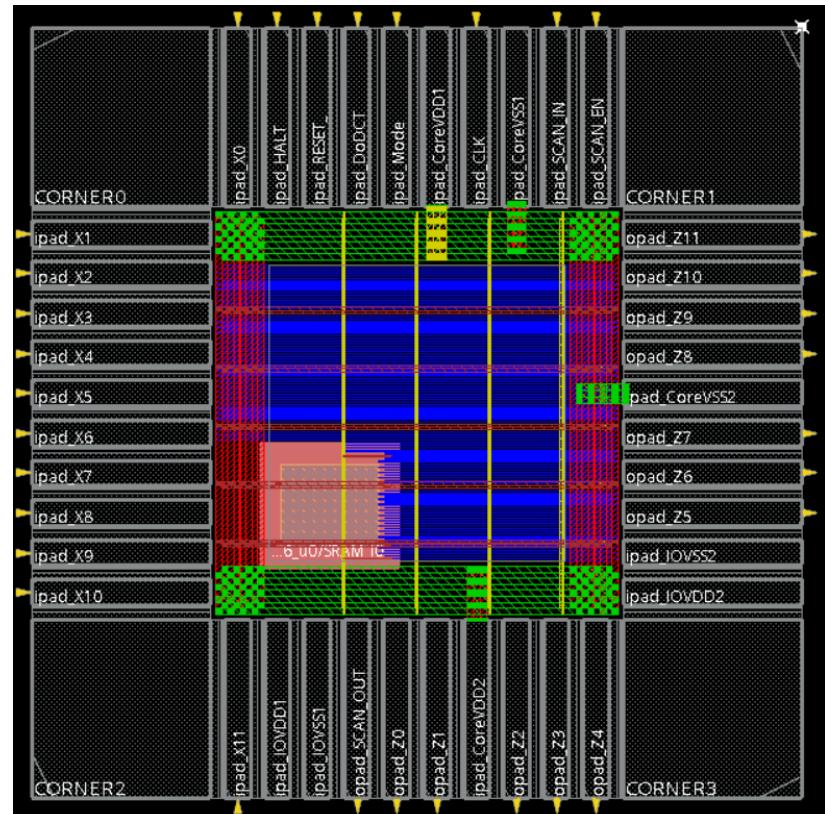
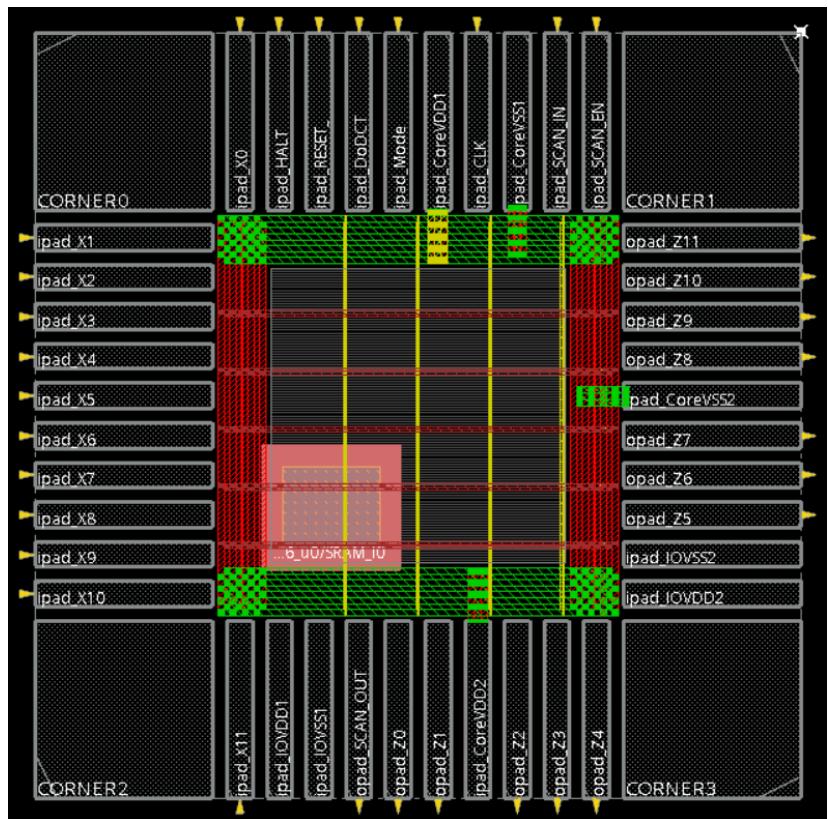
- Route -> Special Route
- Route Special Net (power/ground net)
 - Block pins
 - Pad pins
 - Pad rings
 - Follow pins
 - Floating stripes
 - Secondary power pins

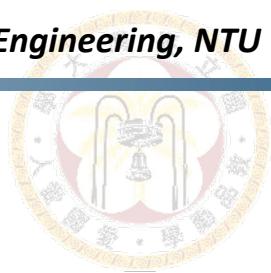




Power Planning: Follow Pins

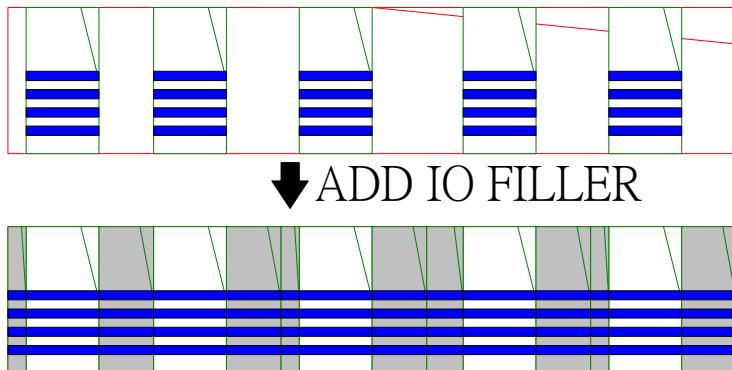
- Supply voltage for std cells by power stripes





Connect Pad Power Ring

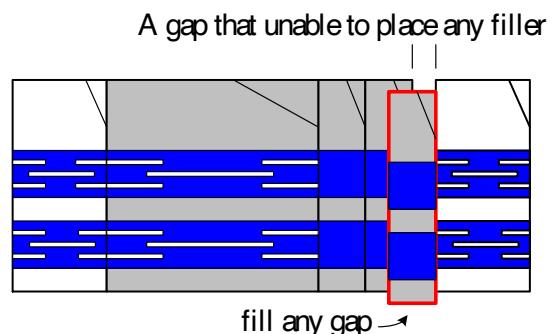
- Connect IO pad power bus by inserting IO filler.

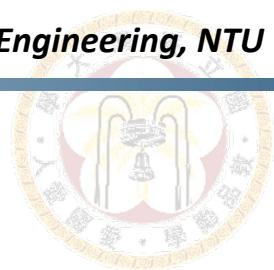


- Add from wider filler to narrower filler.

— *source addIoFillers.cmd*

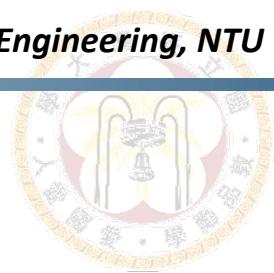
```
addIoFiller -cell PFILLER20 -prefix IOFILLER
addIoFiller -cell PFILLER10 -prefix IOFILLER
addIoFiller -cell PFILLER5 -prefix IOFILLER
addIoFiller -cell PFILLER1 -prefix IOFILLER
addIoFiller -cell PFILLER05 -prefix IOFILLER
addIoFiller -cell PFILLER0005 -prefix IOFILLER -fillAnyGap
```





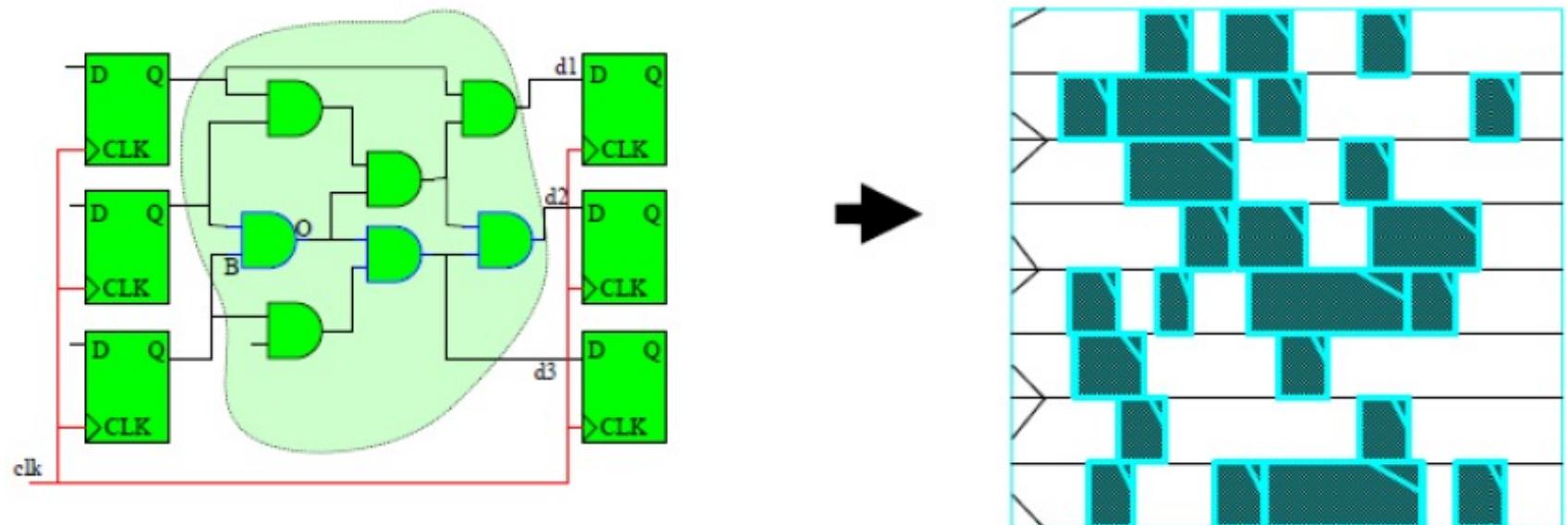
Power stripe strategy

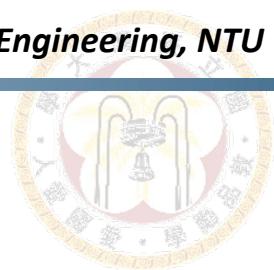
- The density of power mesh dominate the capability of current transfer.
- Width & Set to Set distance
 - Used to adjust power plan density
 - thinner, more frequent stripes are better than thicker, less frequent stripe
- Stripe cut back on routing resource, make stripe every metal above metal 4
- Let metal n connect only to metal n-1



Placement

- **Place -> Place Standard Cells**
 - Innovus #> createBasicPathGroups -expanded
 - Innovus #> get_path_groups
 - Innovus #> place_opt_design
- **Using commands in placement**



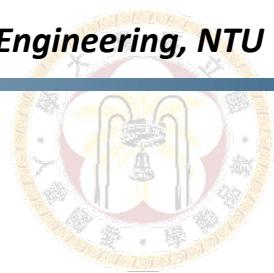


Placement Global Variable

- Set process node
 - *setDesignMode -process 45*
- Set OCV timing analysis mode
 - *setAnalysisMode -analysisType onChipVariation -crror both*
- Set max placement density
 - *setPlaceMode -place_global_max_density 70*
- Expand path groups
 - *createBasicPathGroups -expanded*

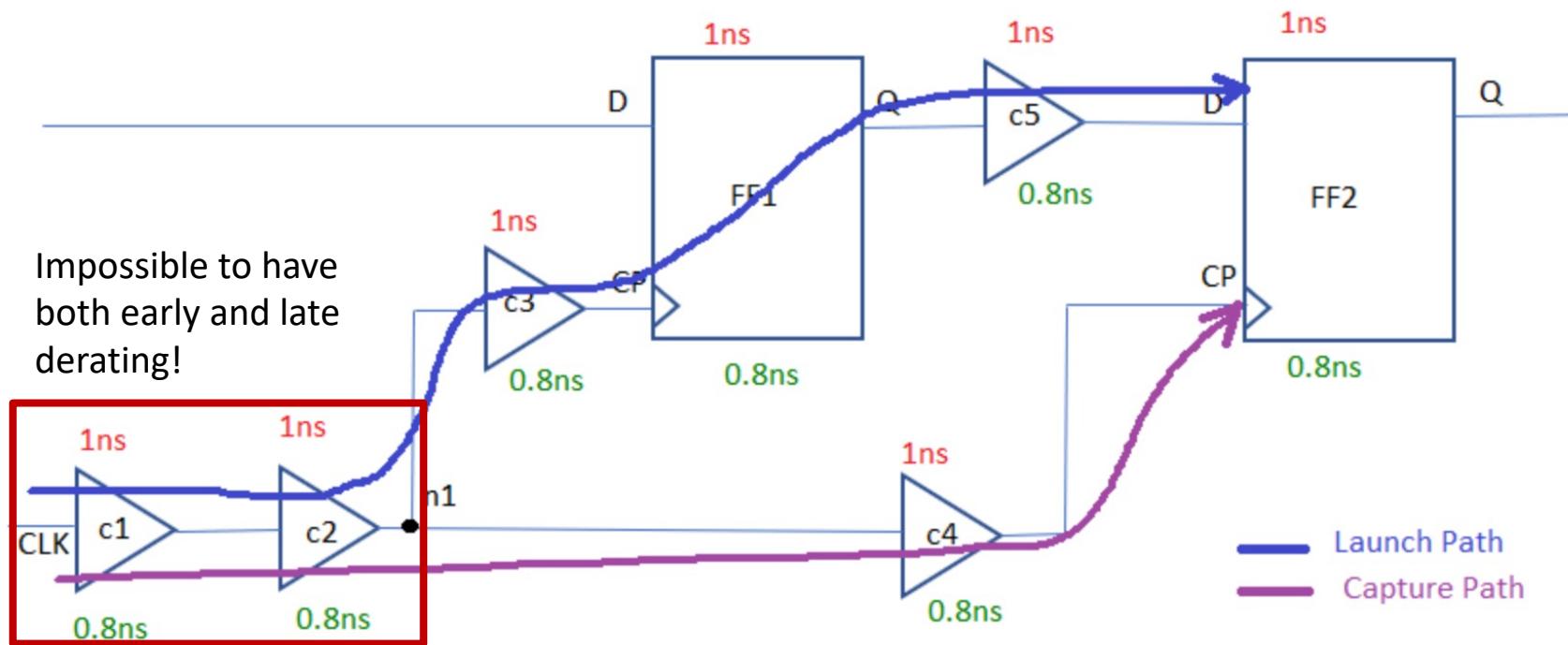
expand path groups

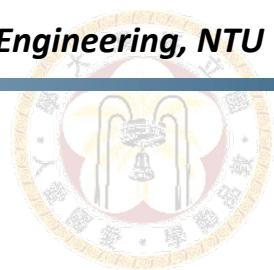
Setup mode	all	reg2reg	reg2cgate	in2reg	reg2out	in2out	default
WNS (ns):	0.010	0.010	2.266	3.432	0.774	N/A	0.000
TNS (ns):	0.000	0.000	0.000	0.000	0.000	N/A	0.000
Violating Paths:	0	0	0	0	0	N/A	0
All Paths:	3423	3339	27	45	12	N/A	0



CRPR/CPPR for Reg2Reg path

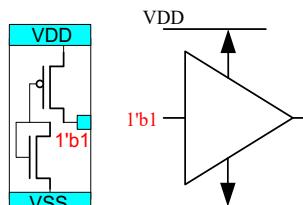
- Common Path Pessimism Removal (Cadence)
Clock Reconvergence Pessimism Removal (Synopsys)
- Remove pessimistic timing analysis in clock common path



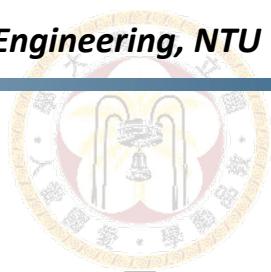


Add Tiehi/Tielo cell

- ◆ Tiehi/Tielo cell connect tiehi/tielo net to supply voltage or ground with resistor
- ◆ Tiehi/Tielo cell is added for ESD protection.
- ◆ *Place → Tie Hi/Lo Cell → Add*



```
setTieHiLoMode -maxDistance 100 -maxFanout 10  
addTieHiLo -cell {LOGIC0_X1 LOGIC1_X1}
```



Timing Analysis

Timing → Report Timing ...

Basic Advanced

Use Existing Extraction and Timing Data

Design Stage

Pre-Place Pre-CTS Post-CTS Post-Route Sign-Off

Analysis Type

Setup Hold

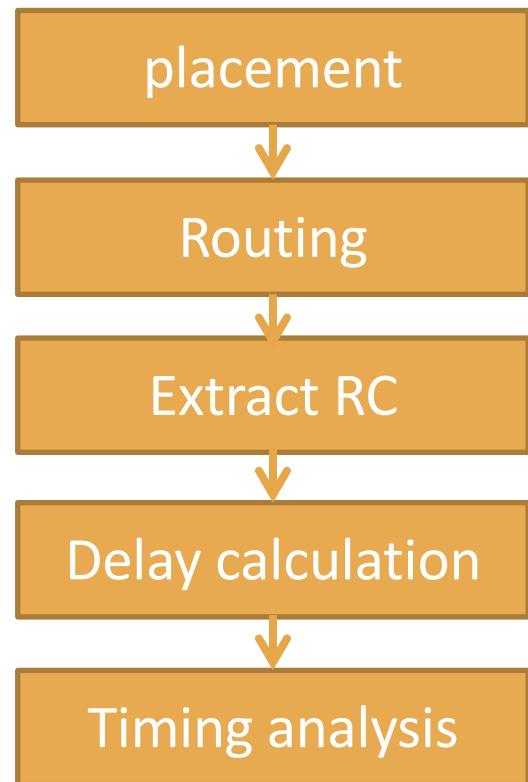
Reporting Options

Number of Paths: 50

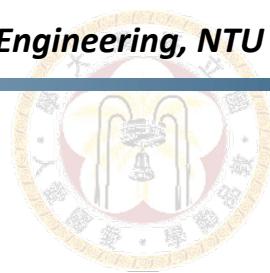
Report file(s) Prefix: CHIP_preCTS

Output Directory: timingReports

Buttons: **OK** (red), Apply, Cancel, Help



timeDesign -preCTS -prefix CHIP_preCTS -outDir timingReports



Timing Analysis Report

■ Summary

Setup mode	all	reg2reg	reg2cgate	in2reg	reg2out	in2out	default
WNS (ns):	-0.098	-0.098	2.225	3.447	0.781	N/A	0.000
TNS (ns):	-0.282	-0.282	0.000	0.000	0.000	N/A	0.000
Violating Paths:	5	5	0	0	0	N/A	0
All Paths:	3423	3339	27	45	12	N/A	0

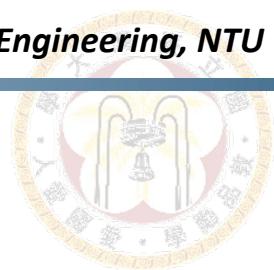
DRVs	Real		Total
	Nr nets(terms)	Worst Vio	Nr nets(terms)
max_cap	0 (0)	0.000	0 (0)
max_tran	0 (0)	0.000	0 (0)
max_fanout	0 (0)	0	0 (0)
max_length	0 (0)	0	0 (0)

■ Default output directory: ./timingReports

CHIP_preCTS_all.tarpt.gz
 CHIP_preCTS.cap.gz
 CHIP_preCTS_default.tarpt.gz
 CHIP_preCTS.fanout.gz
 CHIP_preCTS_in2out.tarpt.gz

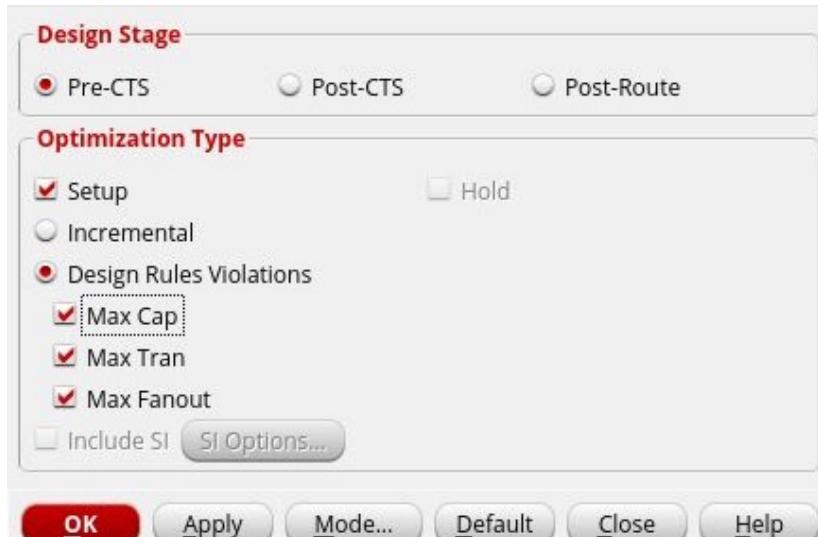
CHIP_preCTS_in2reg.tarpt.gz
 CHIP_preCTS.length.gz
 CHIP_preCTS_reg2cgate.tarpt.gz
 CHIP_preCTS_reg2out.tarpt.gz
 CHIP_preCTS_reg2reg.tarpt.gz

CHIP_preCTS.slk
 CHIP_preCTS.summary.gz
 CHIP_preCTS.tran.gz

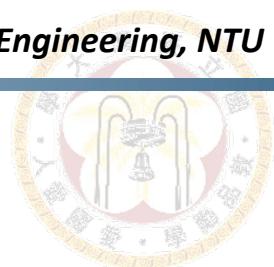


Optimization

ECO → Optimize Design...

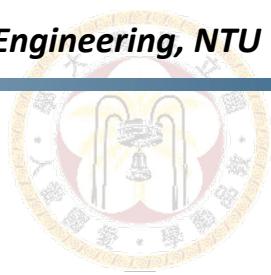


optDesign -preCTS -setup -prefix CHIP_preCTS -outDir timingReports

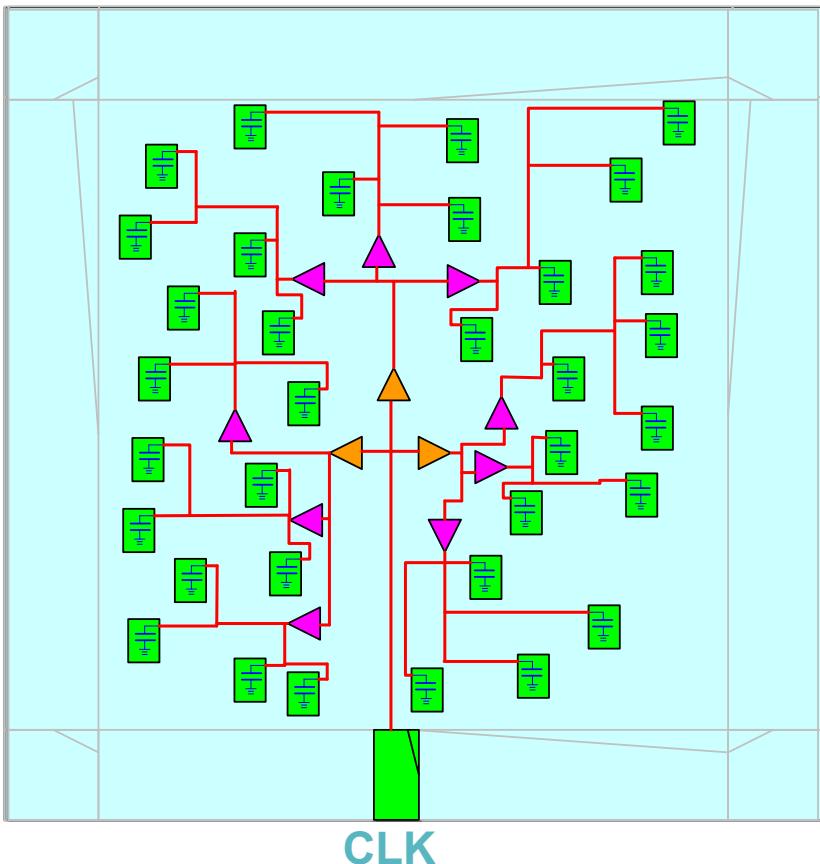


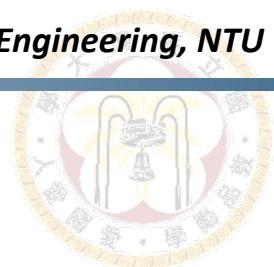
Clock Tree Synthesis (CTS)

- Add multi-level buffer trees according to the clk specification
- A good clock tree should have the same feature as described in the clock estimation
- CTS result will not follow spec if clk estimation is not realistic
- Clock issues
 - Heavy clock net loading
 - Long clock insertion delay
 - Clock skew
 - Clock to signal coupling effect
 - Clock is power hungry



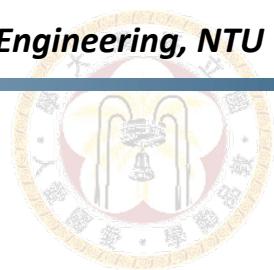
Clock Tree Topology





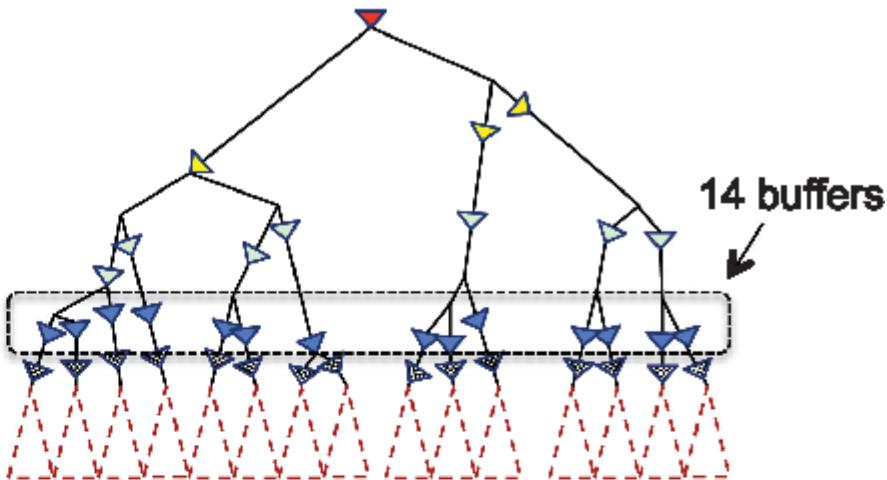
Edit .sdc before CTS

- **set_clock_latency**
 - source latency
 - clock network delay
- **set_clock_uncertainty**
 - clock jitter
 - clock skew
 - timing margin
- **Update .sdc file before CTS**
 - Comment **set_clock_latency**
 - Comment **set_clock_uncertainty**
 - Comment **set_ideal_network**
 - **Innovus #> update_constraint_mode -name CM_mode -sdc_files post_cts.sdc**

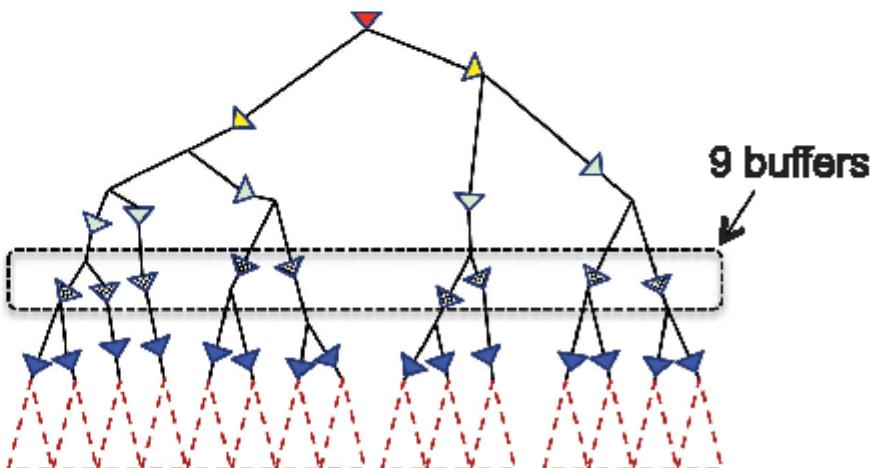


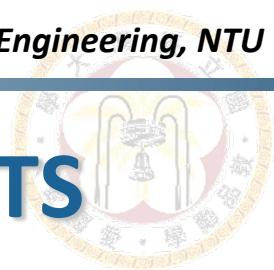
Optimization Example of CTS

Without CTS optimization



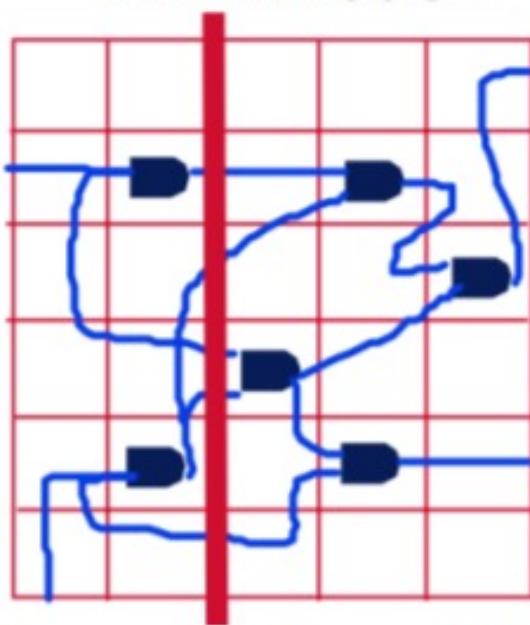
With CTS optimization



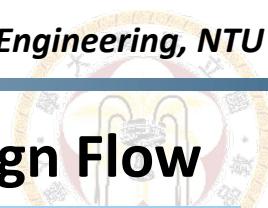


Possible Drawbacks of Traditional CTS

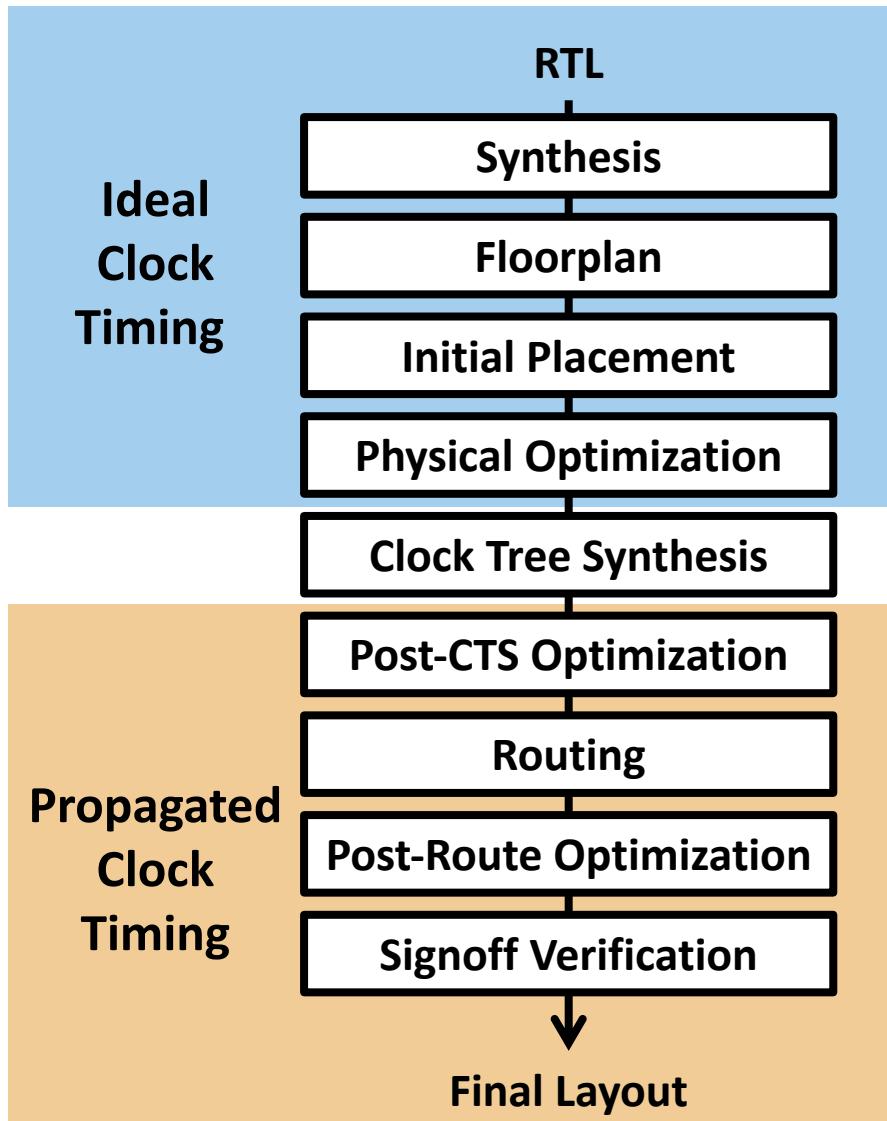
- More buffers are added
- Congestion may increase
- New timing violations



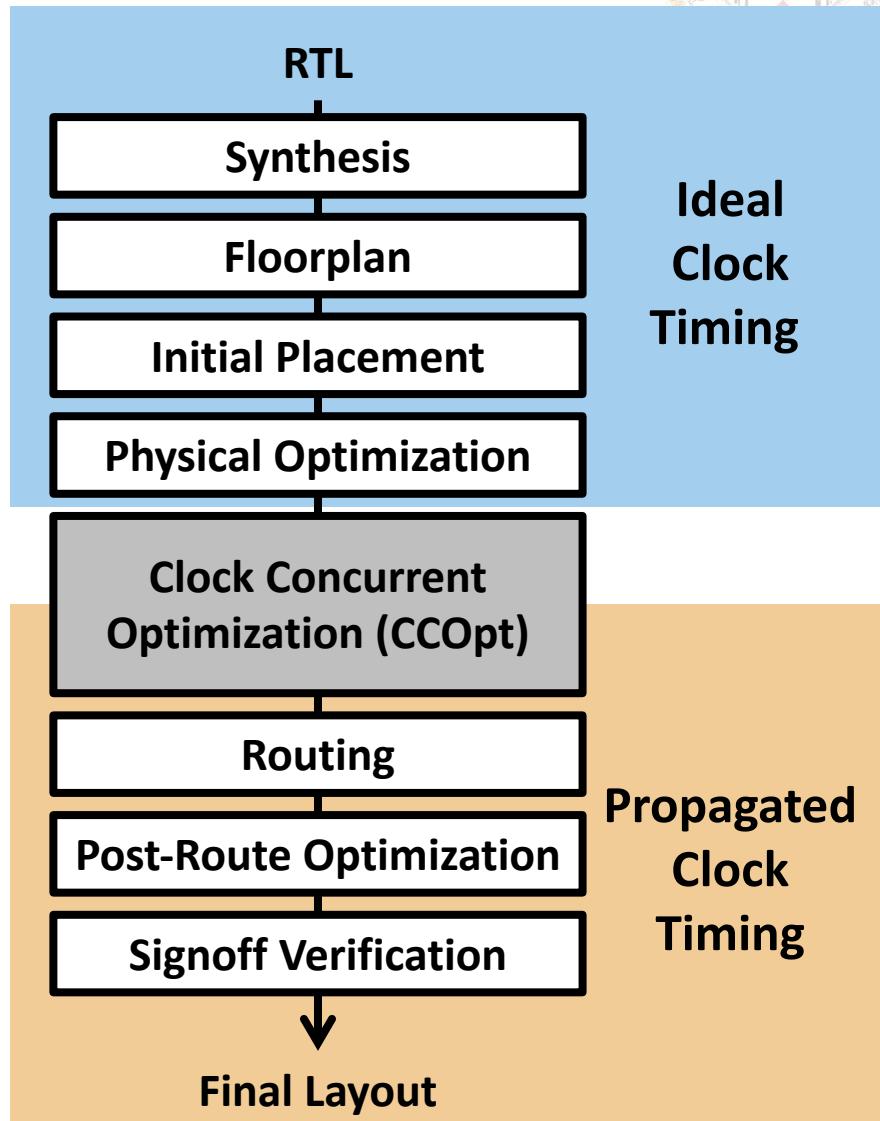
Congestion map

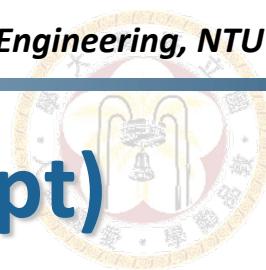


Traditional Design Flow



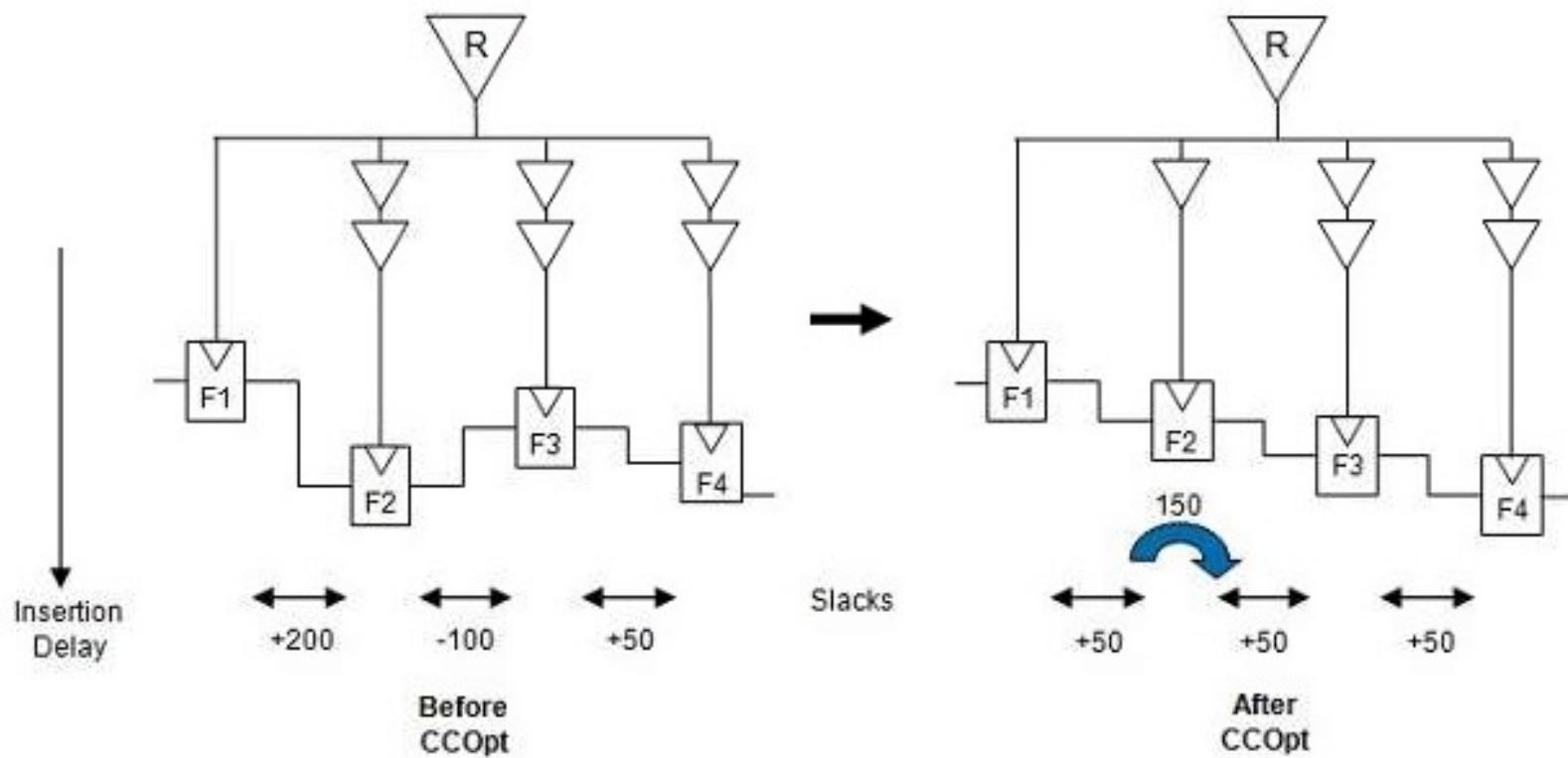
Clock Concurrent Design Flow

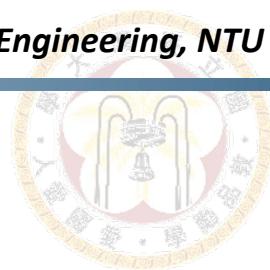




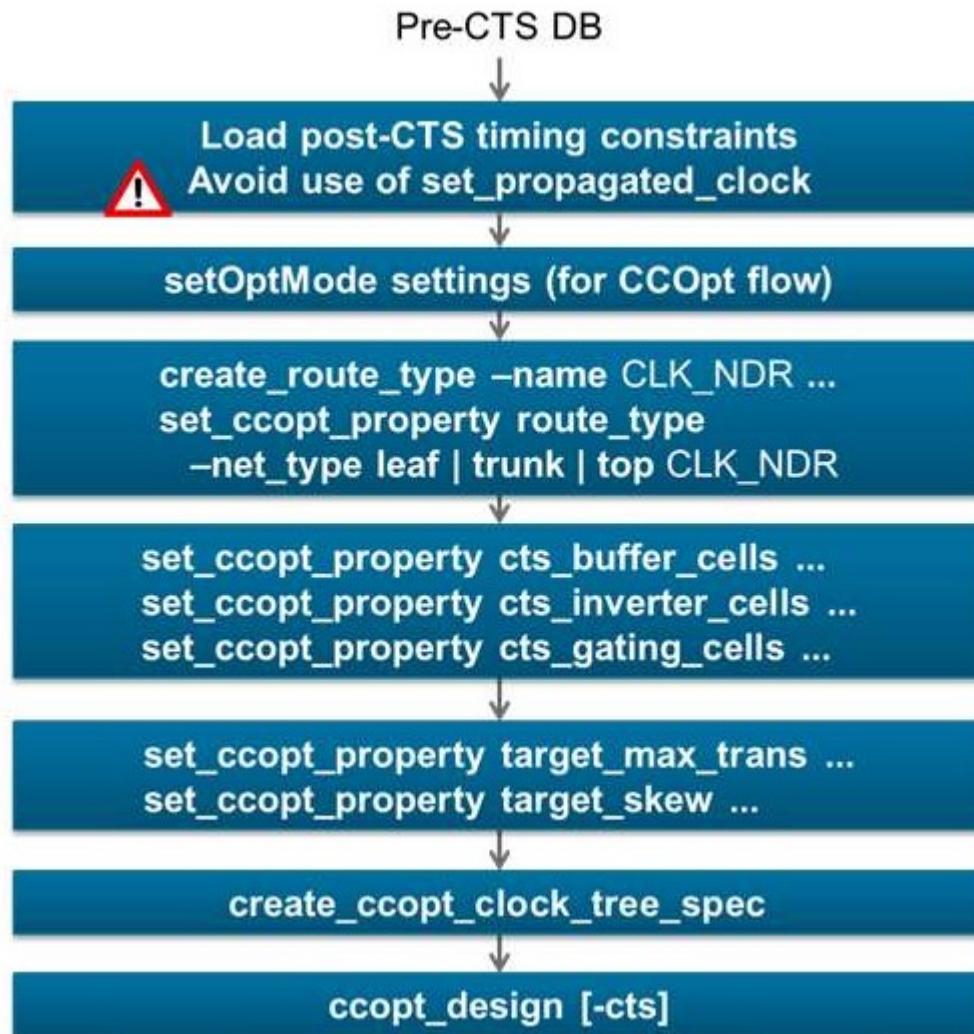
Clock Concurrent Optimization (CCOpt)

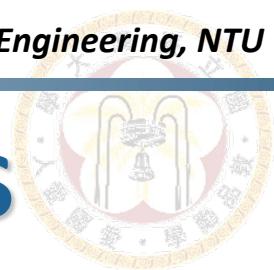
- CCOpt is used to optimize the clock network by
 - reasonable use of skewing
 - simultaneous optimization of clock path and logic path.





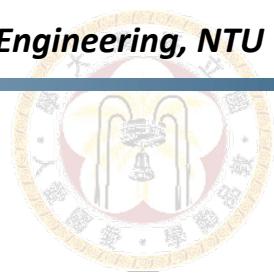
CCOpt Overview





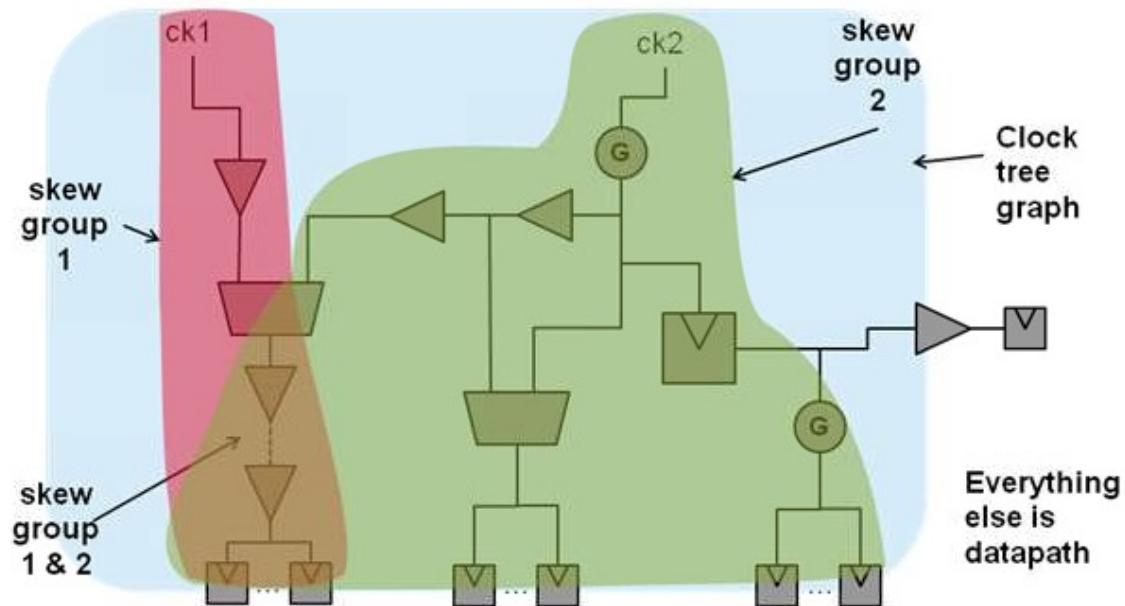
Create CCOpt Specification for CTS

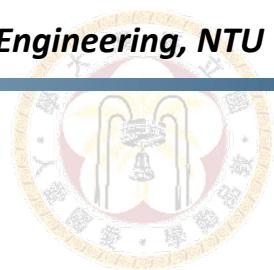
- Create a clock tree specification by analyzing the timing graph structure of all active setup and hold analysis views
 - **Innovus #> create_ccopt_clock_tree_spec**
- Or written to a file for inspection and then loaded
 - **Innovus #> create_ccopt_clock_tree_spec -file ccopt.spec**
 - **Innovus #> source ccopt.spec**



clock tree spec

- A clock tree specification contains `clock_tree`, `skew_group`, and `property` settings.





Configure Route Type

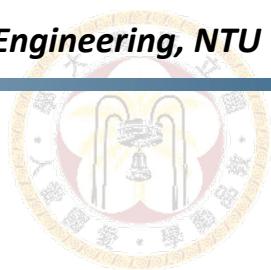
```
create_route_type -name leaf_rule -non_default_rule CTS_2W1S  
                  -top_preferred_layer M5 -bottom_preferred_layer M4
```

```
create_route_type -name trunk_rule -non_default_rule CTS_2W2S  
                  -top_preferred_layer M7 -bottom_preferred_layer M6  
                  -shield_net VSS -bottom_shield_layer M6
```

```
create_route_type -name top_rule -non_default_rule CTS_2W2S  
                  -top_preferred_layer M9 -bottom_preferred_layer M8  
                  -shield_net VSS -bottom_shield_layer M8
```

```
set_ccopt_property -net_type leaf route_type leaf_rule  
set_ccopt_property -net_type trunk route_type trunk_rule  
set_ccopt_property -net_type top route_type top_rule
```



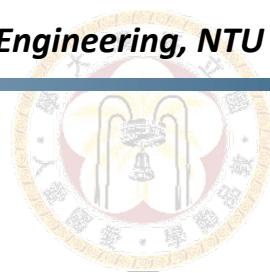


Non-Default Rule

- Define NDR
 - Double width is recommended to reduce resistance and permit use of bar shape vias.
 - Double spacing to reduce the capacitance impact of shielding.

```
add_ndr -name CTS2W2S \
    -width {metal3:metal7 0.28 metal8:metal9 0.56} \
    -spacing {metal3:metal7 0.28 metal8:metal 0.56} \
    -generate_via
```

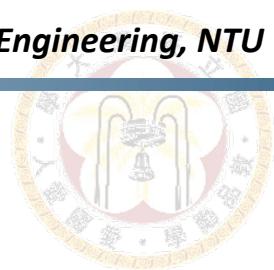
```
add_ndr -name CTS2W2S \
    -spacing_multiplier {metal3:metal9 2} \
    -width_multiplier {metal3:metal9 2} \
    -generate_via
```



Configure Library Cells

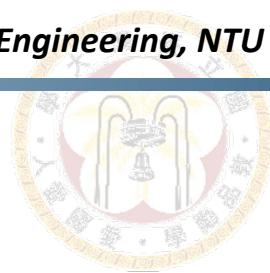
- Define library cells
 - LVT cells result lower insertion delay and less impact of OCV timing derates, therefore reducing the datapath dynamic and leakage power from optimization.
 - Permit the largest library cells may be undesirable for electromigration reasons and can increase clock power.
 - Very weak cells, for example X3 and below in many libraries, are usually undesirable due to poor cross-corner scaling characteristics and are sensitive to detailed routing jogs and changes.
 - Do not exclude small cells, such as X4, as otherwise CTS will be forced to use larger more power and area consuming cells.

```
set_ccopt_property buffer_cells { DCCKBUFX12 CKBUFX8 CKBUFX6 CKBUFX4 }
set_ccopt_property inverter_cells {DCCKINVX12 CKINVX8 CKINVX6 CKINVX4 }
set_ccopt_property clock_gating_cells {ICGX12 ICGX8 ICGX6}
set_ccopt_property logic_cells {CKNAND4 CKMX4}
set_ccopt_property use_inverters true
```



Configure Target

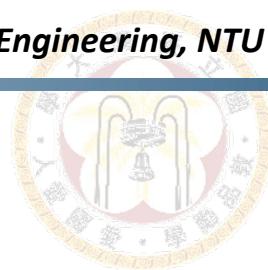
- Configure maximum transition target
 - `set_ccopt_property target_max_trans 100ps`
- Configure a skew target
 - `set_ccopt_property target_skew 50ps`
 - CTS will auto-generate skew targets where none are specified



CCOpt Clock Tree Debugger

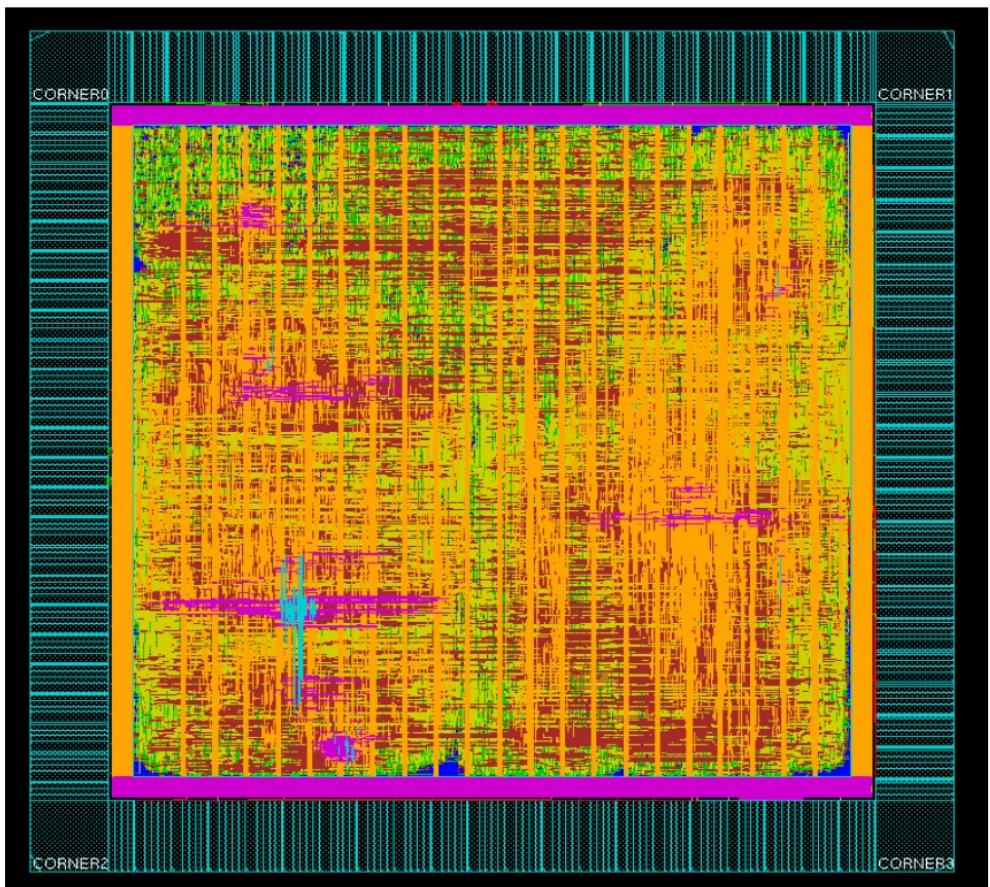
Clock → CCOpt Clock Tree Debugger..

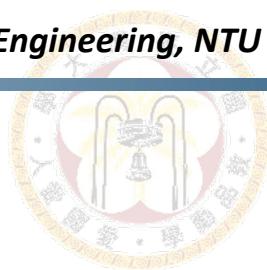




Routing

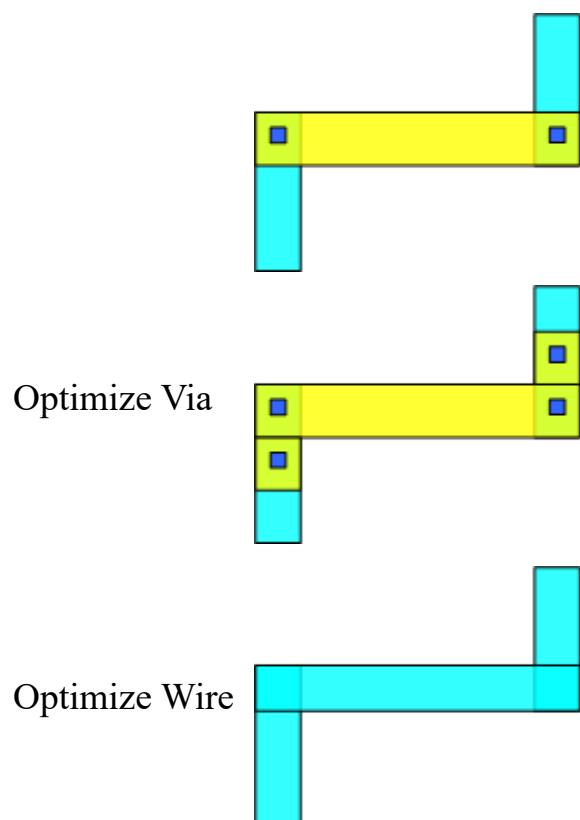
- A process to add wires essential for properly connecting the placed components while following all design rules
 - Std cells
 - Macro pins
 - I/O pads
- Goals
 - Optimized wire length
 - Min # of vias
 - Meet timing constraints
 - No LVS error
 - No DRC violations

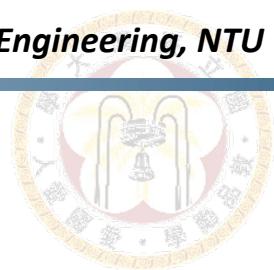




NanoRoute

■ Route -> NanoRoute ->Route

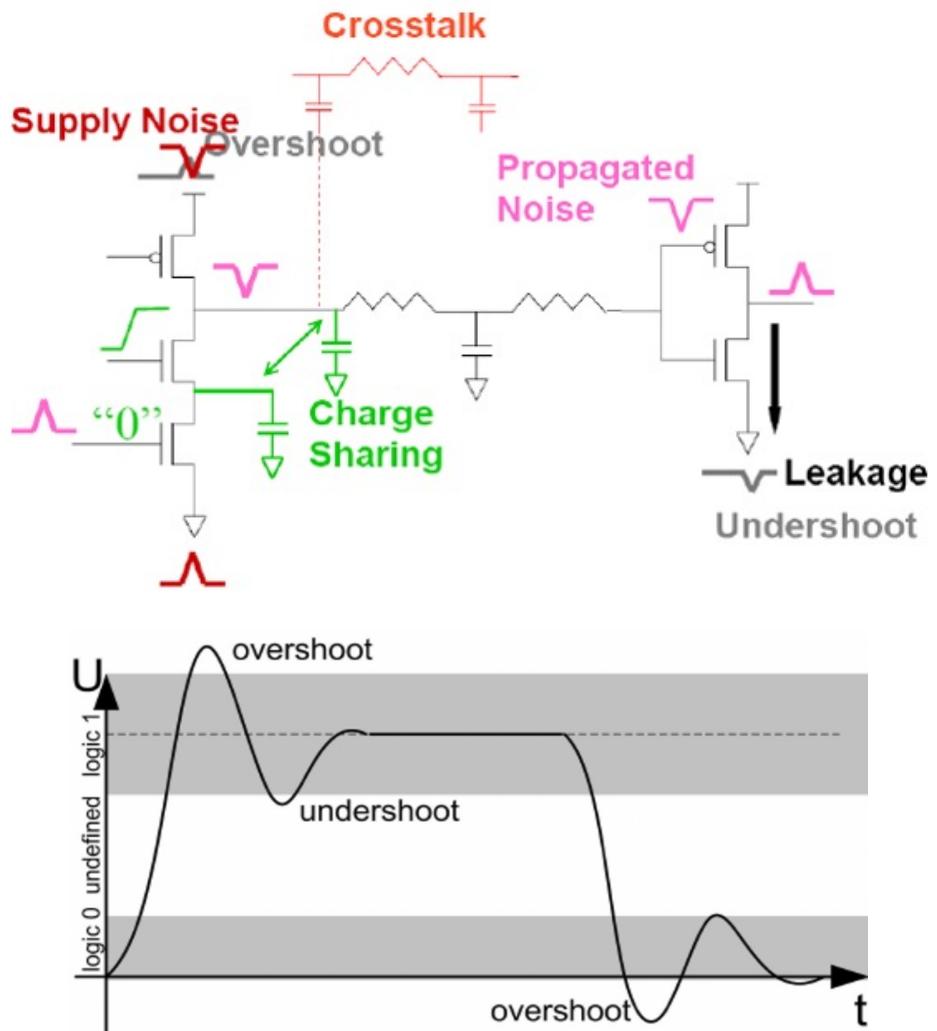


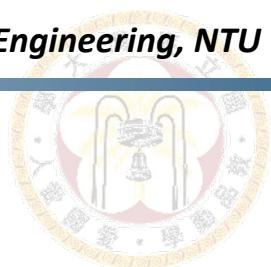


NanoRoute

■ Signal Integrity (SI) Issue

- Crosstalk
- Charge sharing
- Supply noise
- Leakage
- Propagated noise
- Overshoot
- Undershoot

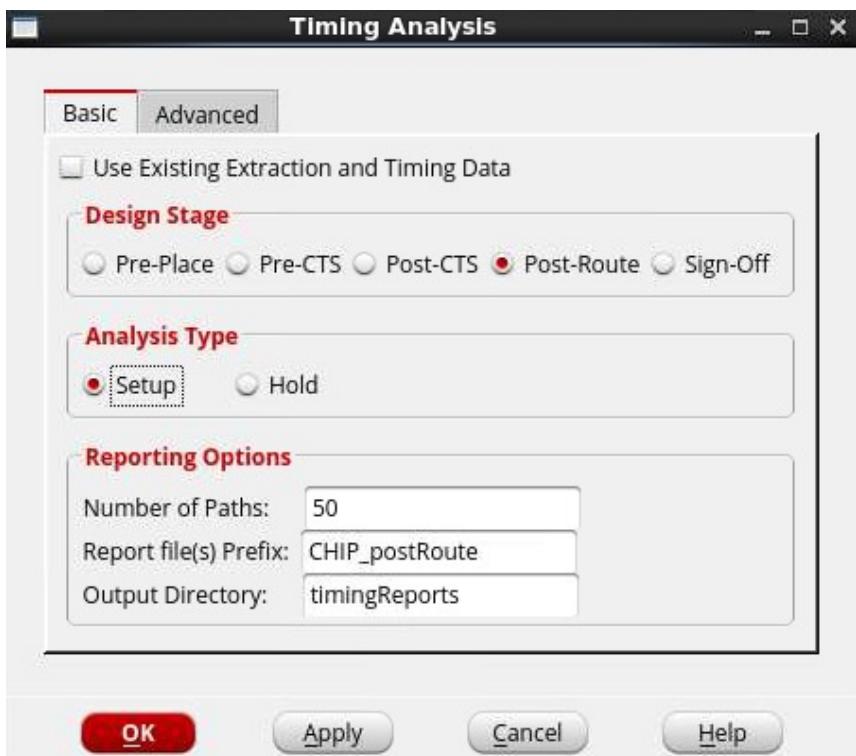


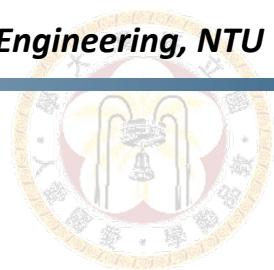


SI Aware Timing Analysis

```
set_db extract_rc_engine post_route  
set_db extract_rc_effort_level high  
set_db timing_enable_si_cppr true  
set_db delaycal_enable_si true  
time_design -post_route
```

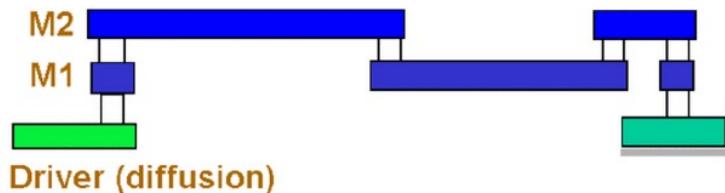
Timing → Report Timing ...

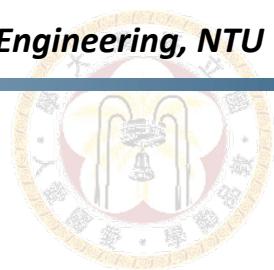




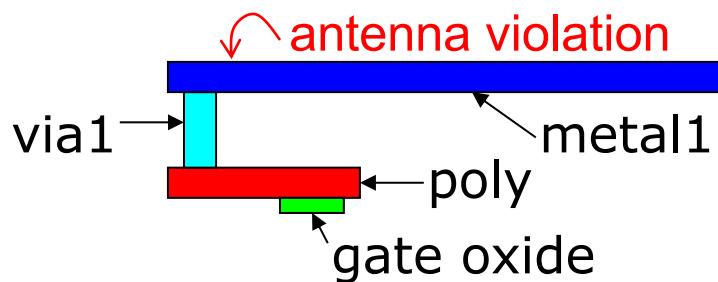
Antenna Effect

- In a chip manufacturing process, metal is initially deposited so it covers the entire chip
- The unneeded portions of the metal are removed by etching
- The exposed metal collect charge and form voltage potential
- If the voltage potential across the gate oxide becomes large enough, the current can damage the gate oxide
- Problem repair
 - Add jumper (change metal layer)
 - Add antenna cell (diode)
 - Add buffer

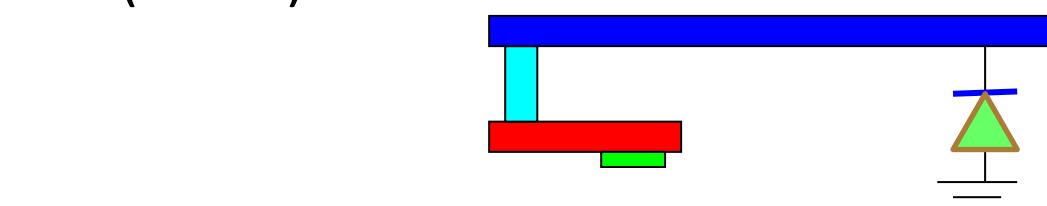
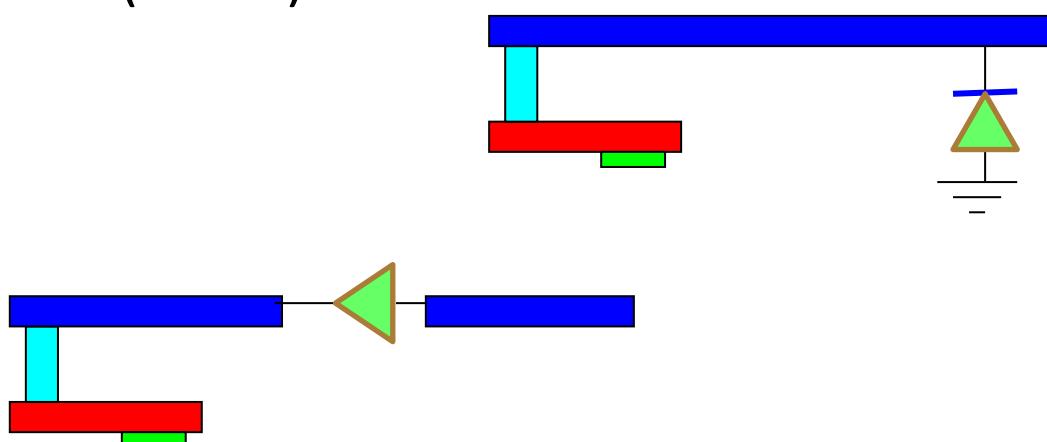
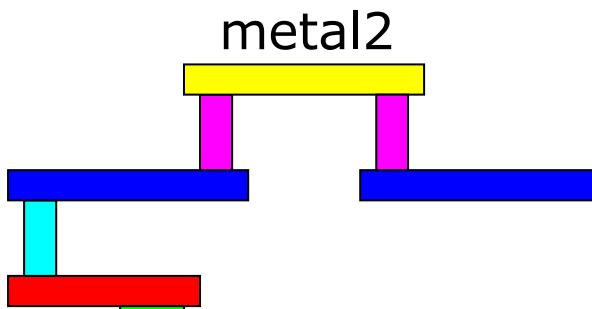




Antenna Problem Repair

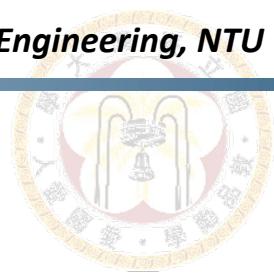


- Add jumper
- Add antenna cell (diode)
- Add buffer



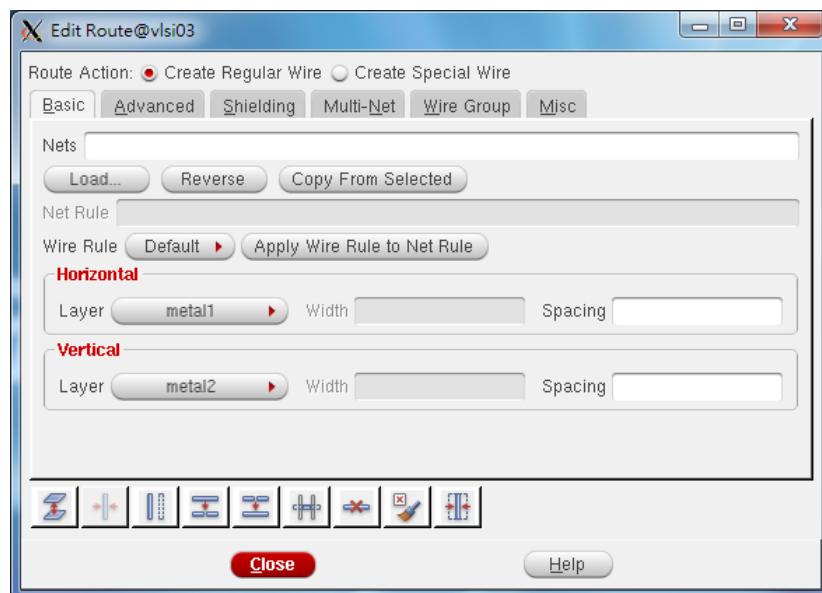
After Routing

- Still may have DRC violations since it uses tricks to prevent checking rules and faster the process
 - “*Search and Repair*” after routing
 - Re-routing again
 - Use other tools to do DRC check
- If DRC violations cannot be cleared in ~50 search & repair loops
 - Change your floorplan or redesign your system

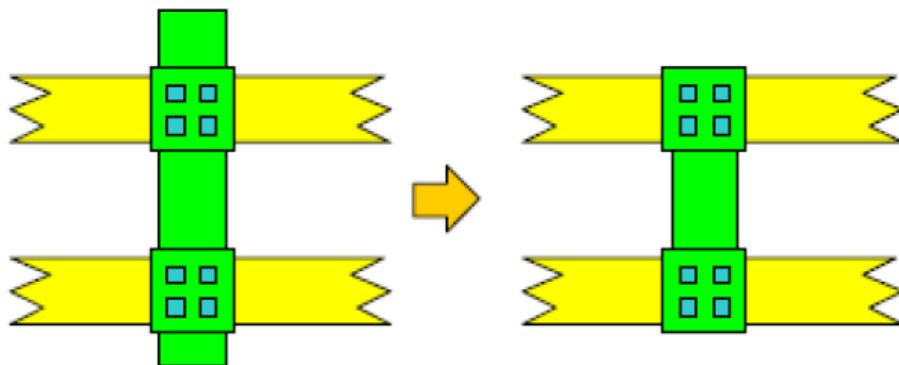


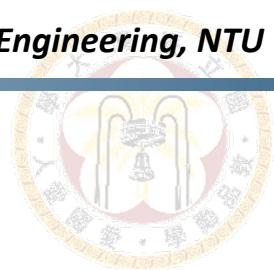
Edit Routing

- Hotkey: e



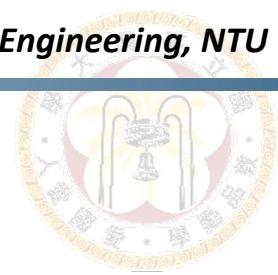
Trim wire
(hotkey : T)





Design for Manufacturing (DFM)

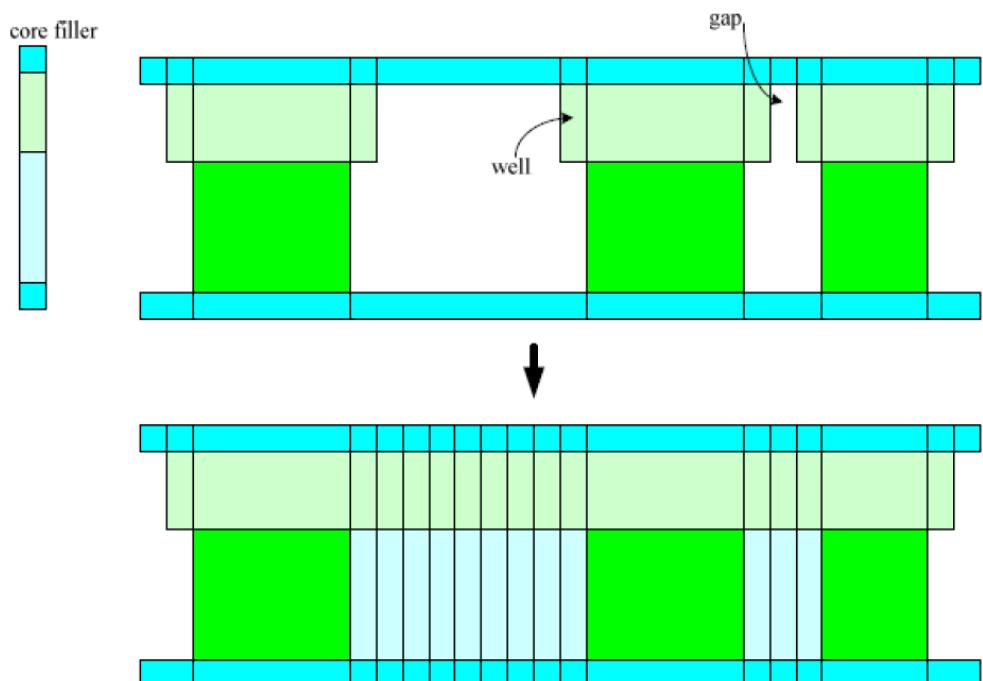
- **Process at the physical design stage of IC**
 - To ensure that the design can be accurately manufactured
- **To improve the yield by the following methods**
 - Add core fillers
 - Add dummy metals
 - Via swapping
 - Add bonding pad
 - Verify DRC & LVS

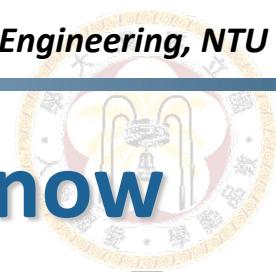


Add Core Fillers

- The core fillers are usually added to the place where std cells are not placed to make the density of the chip more uniform
- *Place -> Filler -> Add Filler*
 - Connect the NWELL/PWELL layer in core rows

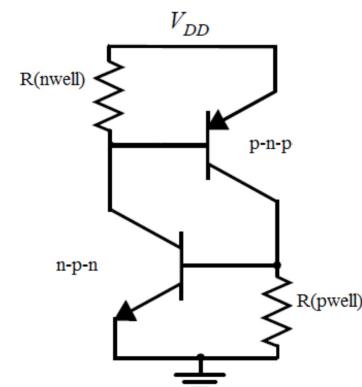
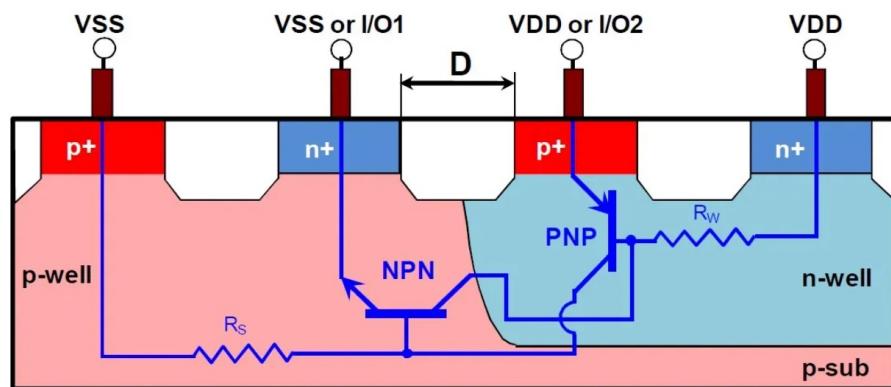
Add from wider
filler to narrow
filler (automatic)

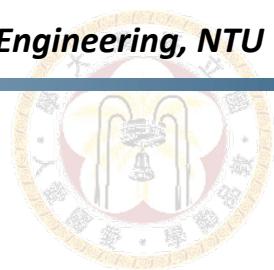




There Are Many Fillers You Need to Know

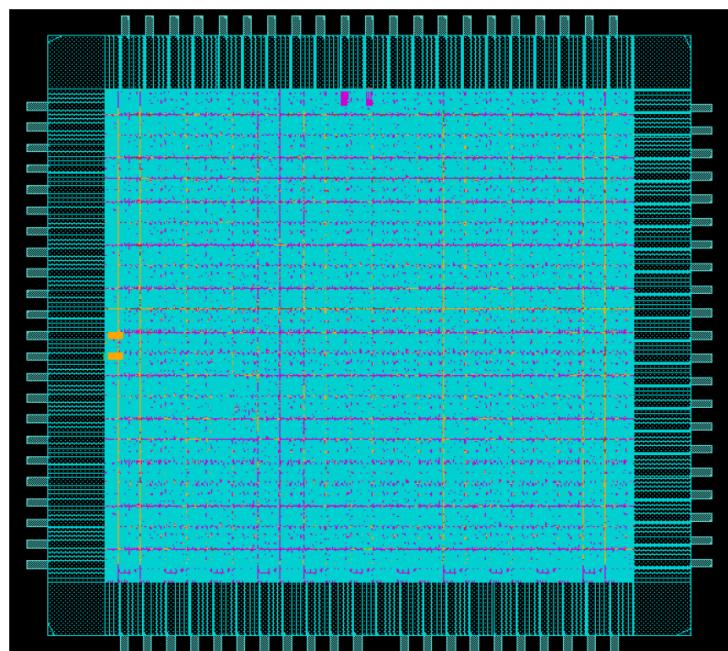
- Decoupling cap (DCAP) can reduced dynamic IR drop
- Welltap/Tapcell is a must < 65nm (Reduce latch-up possibility)
- Boundary cell (Endcap) guards site row boundary for well/implants continuity
- Spare cell is used for metal ECO
- Antenna and Tie cell
- **More info:** <https://aijishu.com/a/106000000157523>

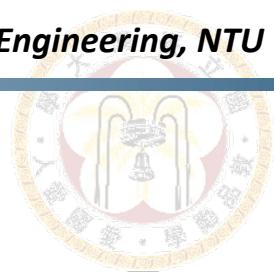




Add Dummy Metals

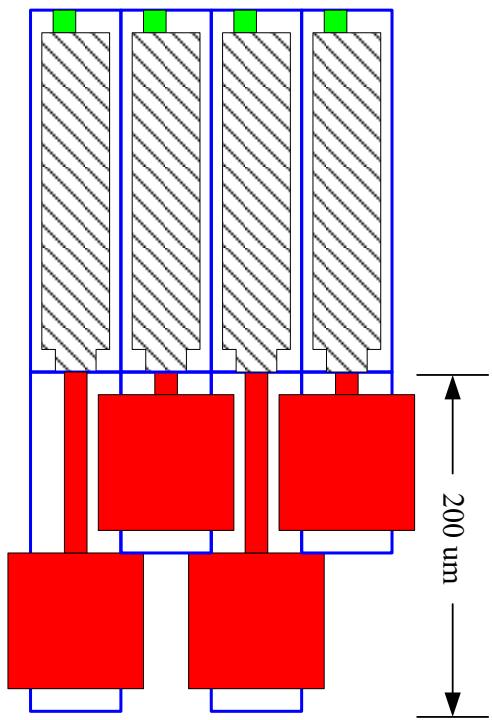
- **Why add dummy metal**
 - Meet minimize metal density rule
 - Prevent over etching
 - Prevent sagging in local area
 - Improve yield
 - Reduce on chip variation
- **Better connect dummy metal to VSS**
- **Drawback**
 - Introduce parasitic to signal line



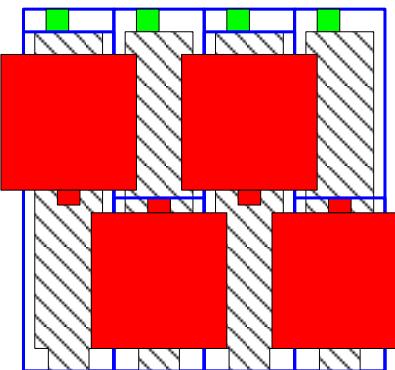


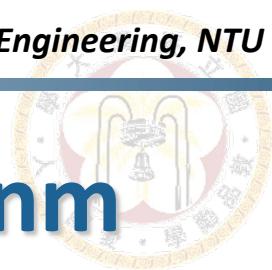
Circuit Under Bond Pad

traditional bonding pad

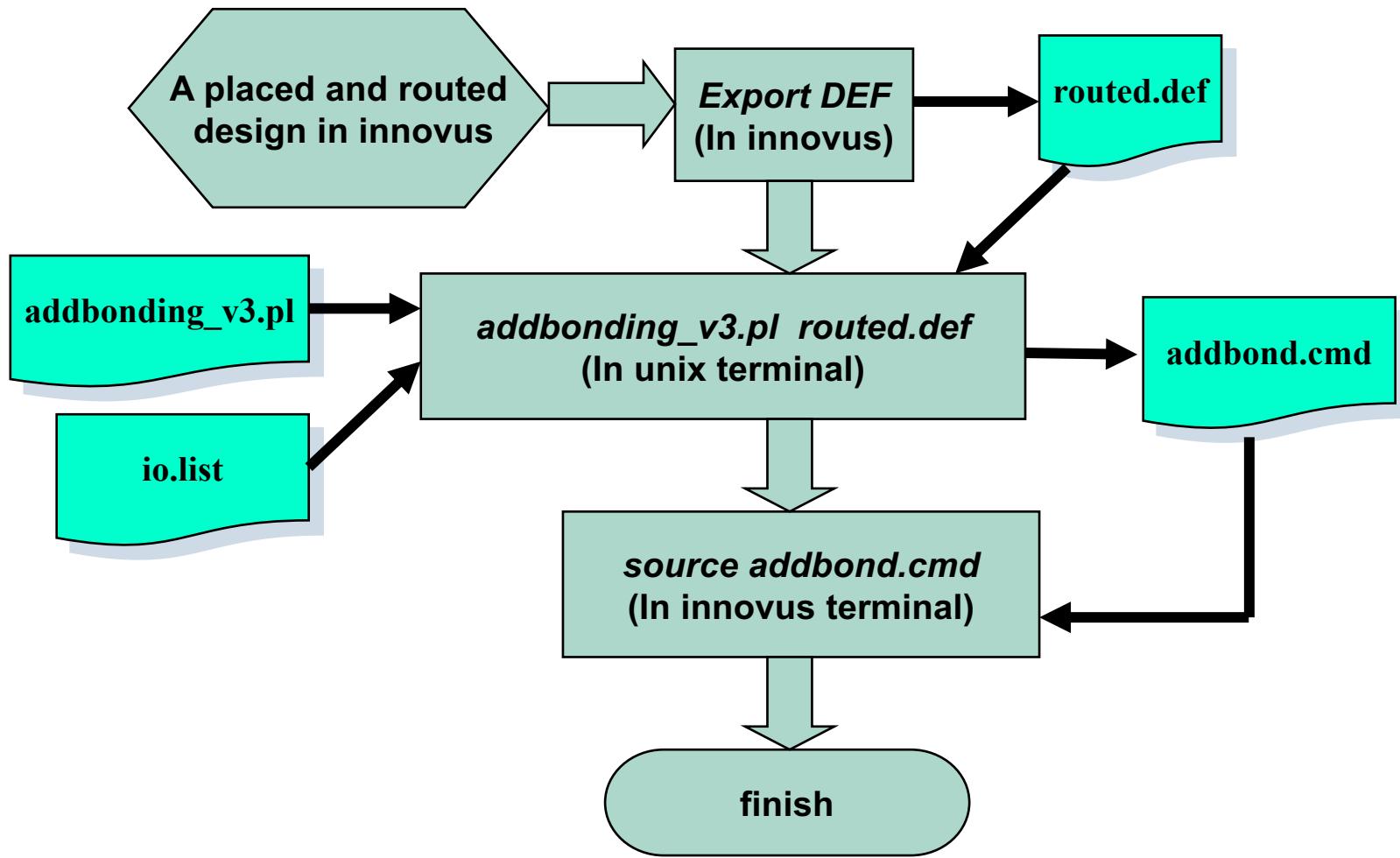


CUP bonding pad



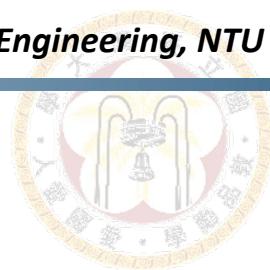


Add bonding pads flow in TSRI 40nm



Output Data

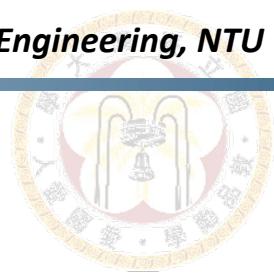
- Export GDS for DRC, LVS, LPE & tapeout
 - *Design -> Save -> GDS* LPE: layout parasitic extraction
- Export Netlist for LVS and simulation
 - *Design -> Save -> Netlist*
- Export the netlist and the .sdf for post layout simulation
 - **Innovus #> write_sdf**
- Export DEF for reordered scan chain
 - *Design -> Save -> DEF*



Export .sdf

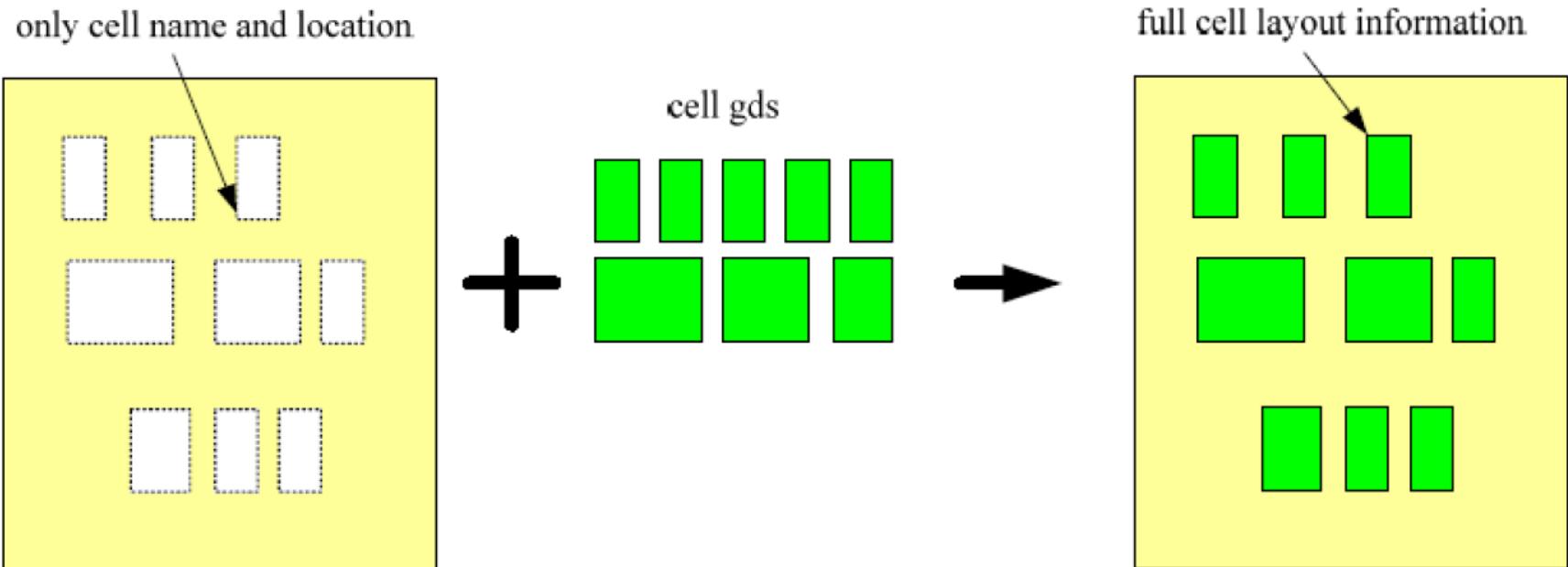
- Use following commands to export .sdf

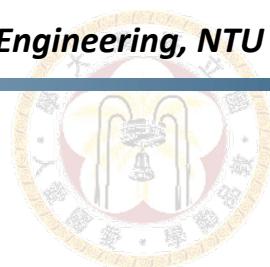
```
setAnalysisMode -analysisType bcwc  
  
write_sdf      -max_view AV_func_max \  
                -min_view AV_func_min \  
                -edges noedge \  
                -splitsetuphold \  
                -remashold \  
                -splitrecrm \  
                -min_period_edges none \  
                CHIP.sdf
```



What is GDS

- **Graphic data stream (GDS) is a binary file format for layout**
 - Represent layout data in a hierarchical format (.gds)
 - E.g. labels, shapes, layer information
 - Etching is based on the parameters provided in the file



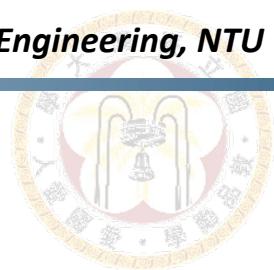


Export .gds

- Use following commands to export .sdf:

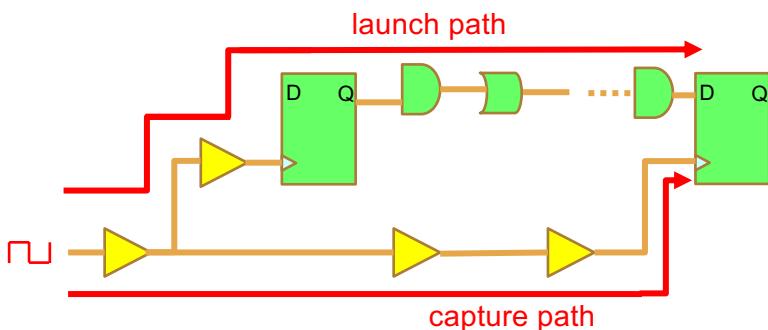
```
setStreamOutMode -specifyViaName default \
                  -Sevianames false \
                  -virtualConnection false \
                  -uniquifyCellNamesPrefix false \
                  -snapToMGrid false \
                  -textSize 1 \
                  -version 3
```

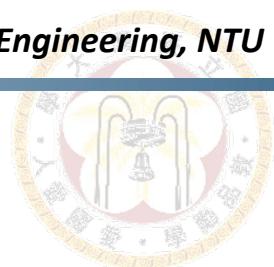
```
streamOut CHIP.gds -mapFile streamOut.map \
                    -merge {XXX.gds XXXX.gds} \
                    -stripes 1 -units 1000 -mode ALL
```



Debug Timing

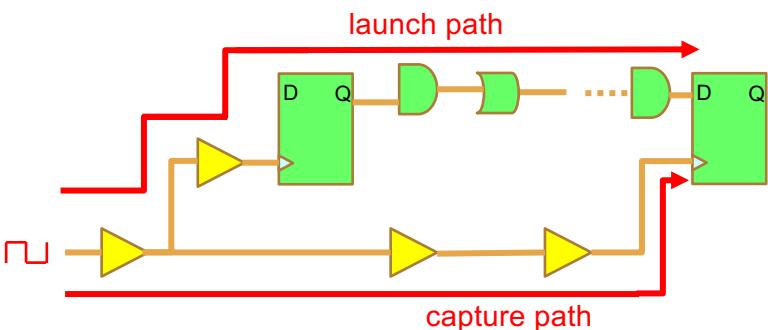
- Check all over the violation path
 - Is it a false path?
 - Unexpected clock latency, skew?
 - Suspiciously long buffer chain?
 - Unexpected large cell/net delay?
 - Incorrect library cell used?
 - Unrealistic drive strength?
 - Unreasonable uncertainty under clock period?
 - Unrealistic derating?
 - Set don't touch?
 - Set don't use?
 - Incorrect generated clock setting?

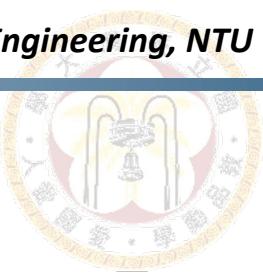




Debug Timing cont.

- Check all over the violation path
 - Path through congested routing area?
 - Path through dense cell area?
 - Path through channel?
 - Path detour?
 - Path around block?
 - Should blockage be removed?
 - How is the timing at pre-cts/post-cts/post-route stage?
 - Delay induced by SI?
 - Reconvergence clock?
 - Does log have warning or error about this path?





Timing Debug

Timing → Debug Timing

Timing Debug

Report File(s): top.mtarpt

File ► Analysis ► Category ►

Path Histogram

Category Summary

Name:	all
Total Path:	93
Passing Path:	84
Failing Path:	9
WNS:	-0.3640
TNS:	-0.7250

Path Group Analysis...

Clock Analysis...

Hierarchical Floorplan...

Hierarchical Port...

View Analysis...

Critical False Path

Bottleneck Analysis

DRV Analysis

Noise Result Analysis...

Hierarchical Analysis Viewer...

Clock Matrix Viewer...

Path Category

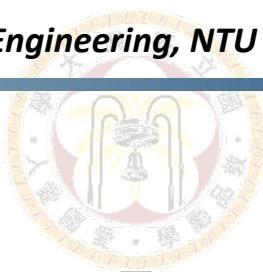
Category	H	Category Name	Correction	WNS	TNS	#Failing Path
1	all		-0.364	-0.725		
2	REG->OUT		-0.364	-0.364		
3	REG->REG		-0.091	-0.361		
4	uncategorized		0.000	0.000		

Path List

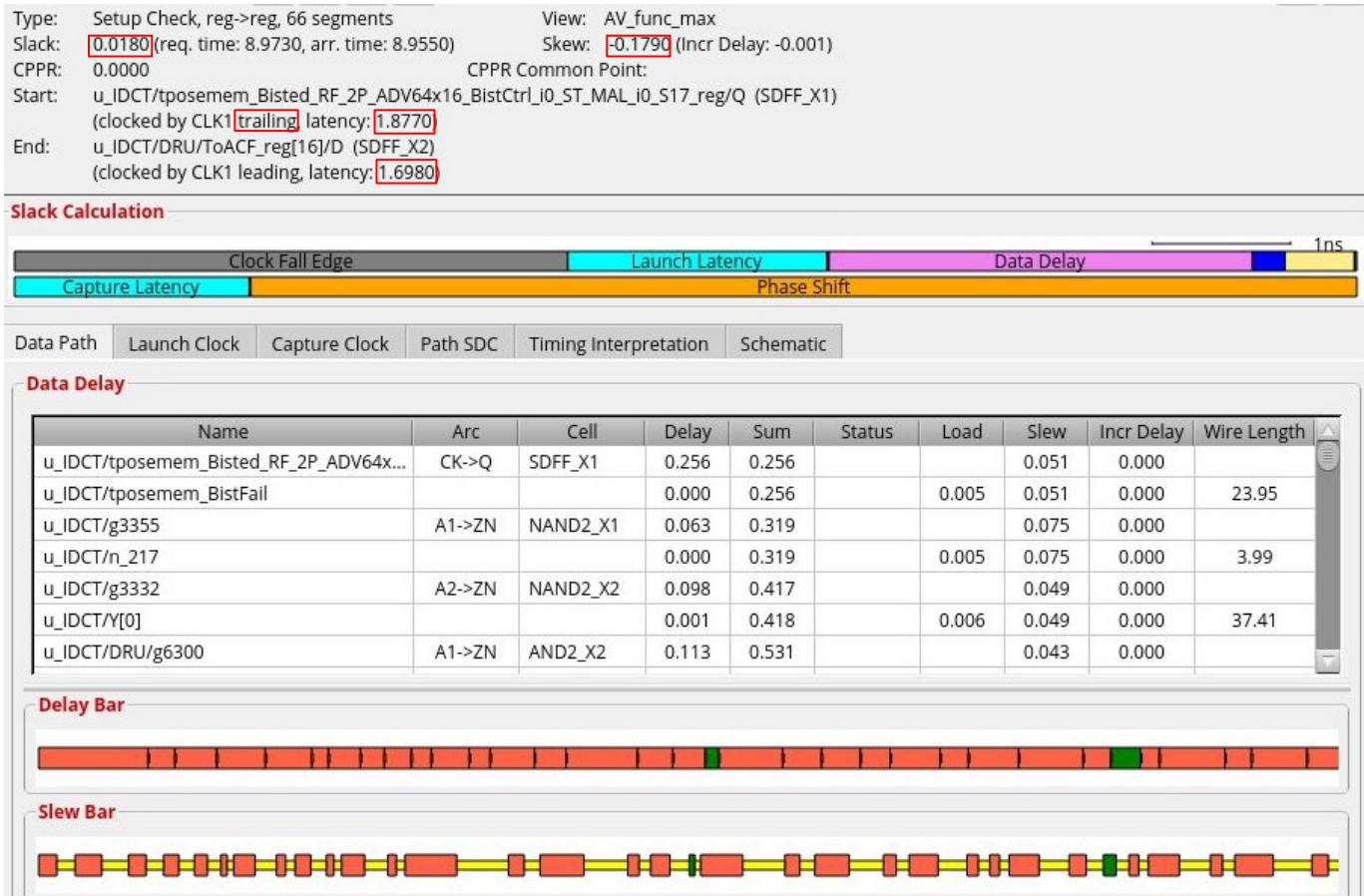
Category: all, Slack Range: all

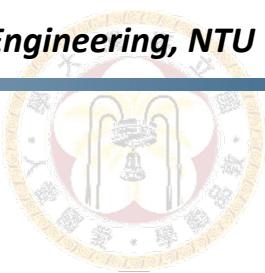
Page: 1 2

H	Path	Clock	ReqTime	Slack	Startpoint Pin	Endpoint Pin
1	CLK1(leading)->CLK1(...)		4.500	-0.364	u_IDCT/Z_reg[1]/Q	Z[1]
2	CLK1(trailing)->CLK1(l...)		9.137	-0.091	u_DCT/tposemem_Bi...	u_DCT/DRU/ToACF_reg[...
3	CLK1(trailing)->CLK1(l...)		9.066	-0.072	u_IDCT/tposemem_Bi...	u_IDCT/DRU/ToBDEG_re...
4	CLK1(trailing)->CLK1(l...)		9.115	-0.069	u_DCT/tposemem_Bi...	u_DCT/DRU/ToBDEG_re...
5	CLK1(trailing)->CLK1(l...)		9.112	-0.036	u_DCT/tposemem_Bi...	u_DCT/DRU/ToBDEG_re...



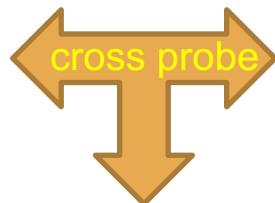
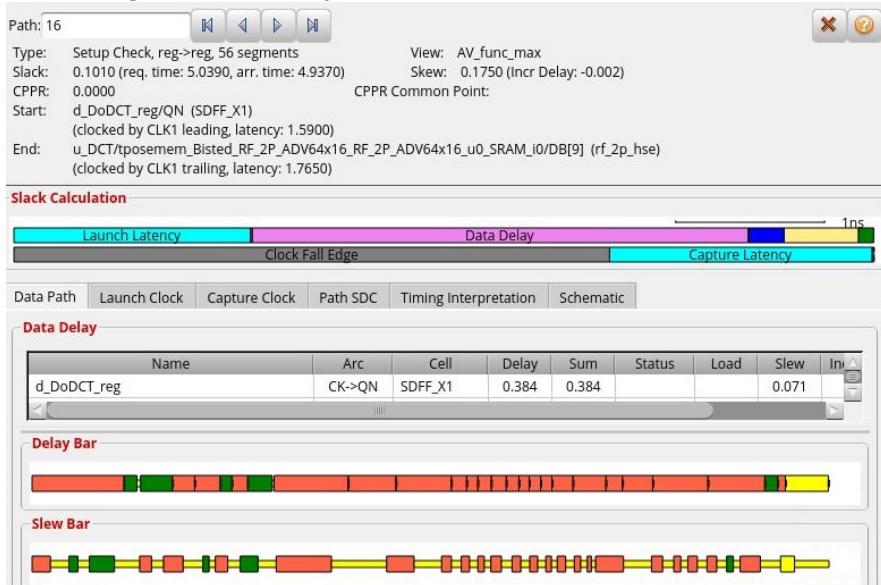
Timing Path Analyzer



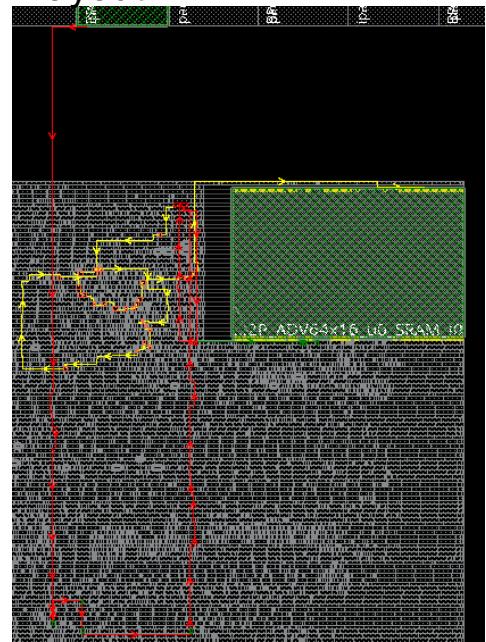


Cross Probing

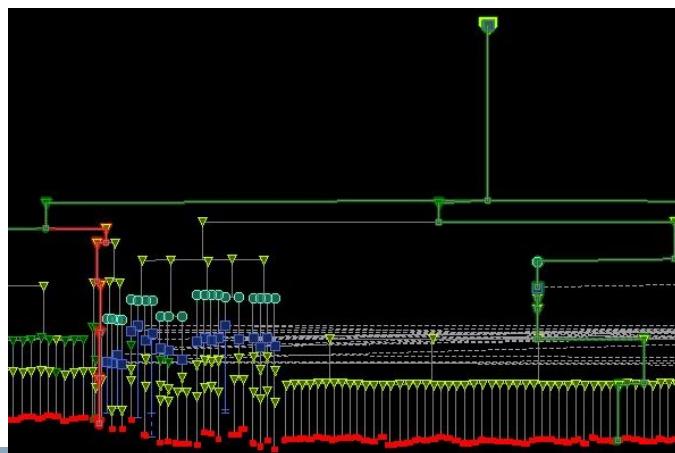
Timing path analyzer

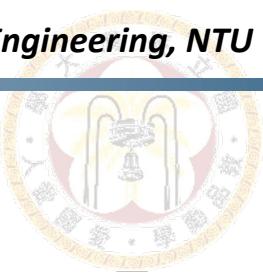


layout

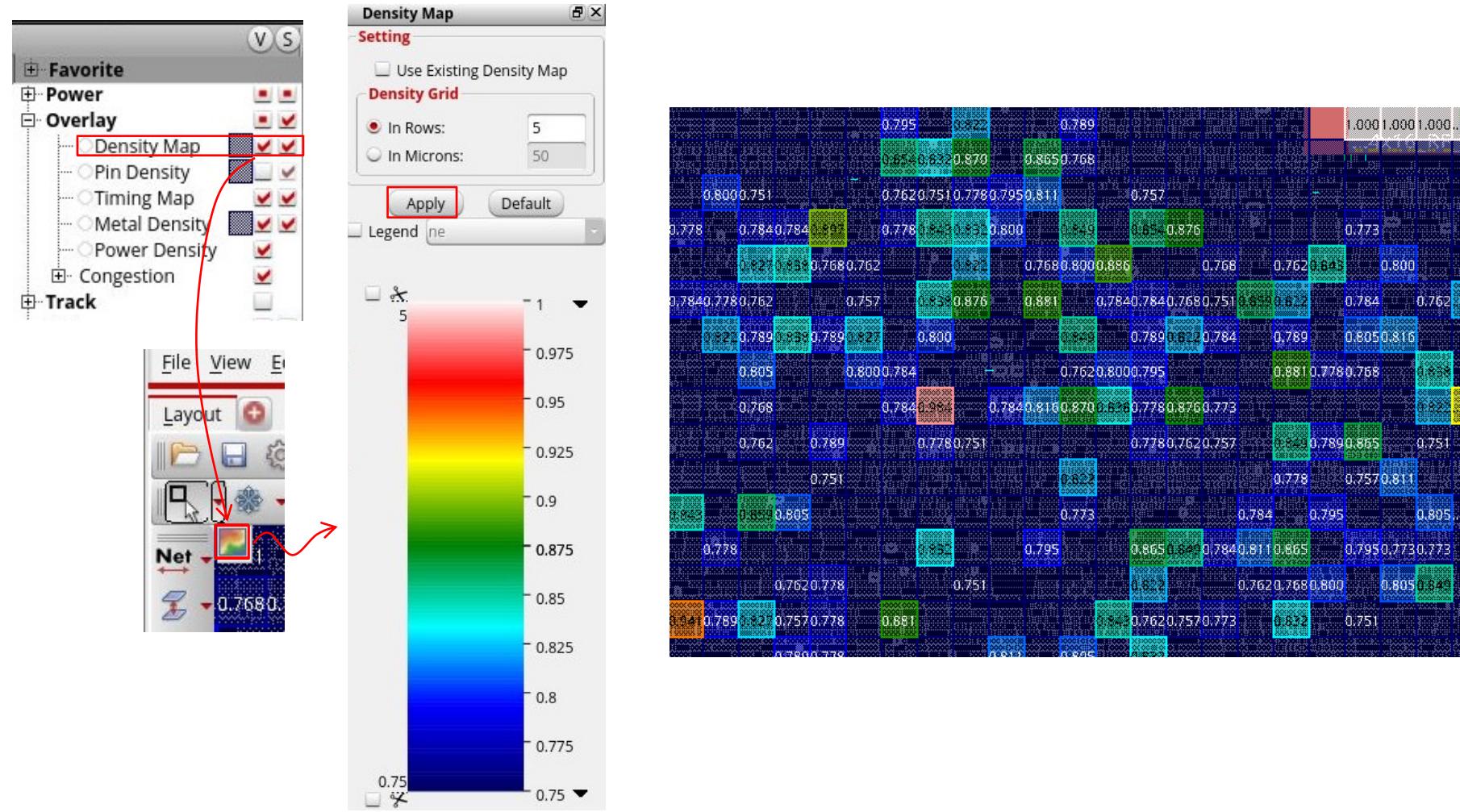


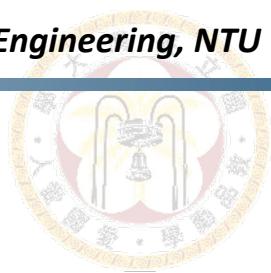
Clock Tree Debugger



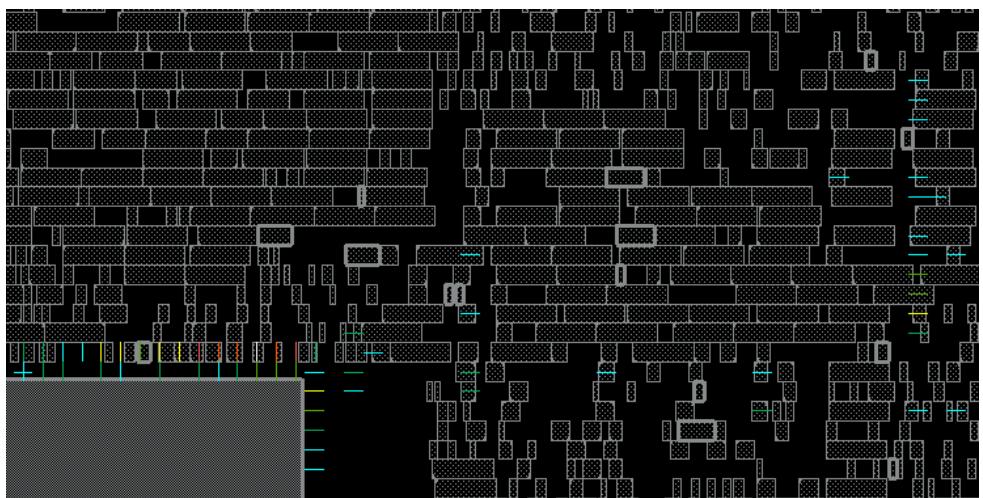
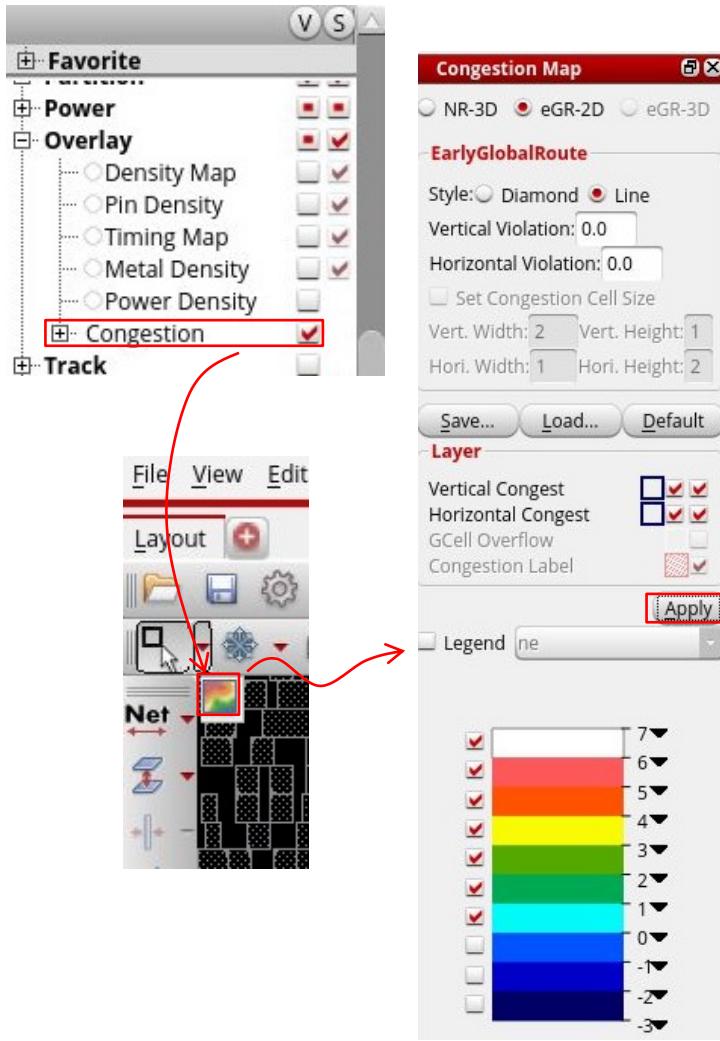


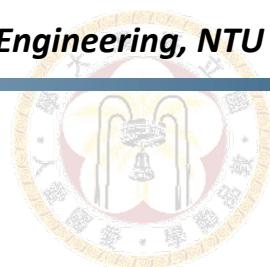
Density map





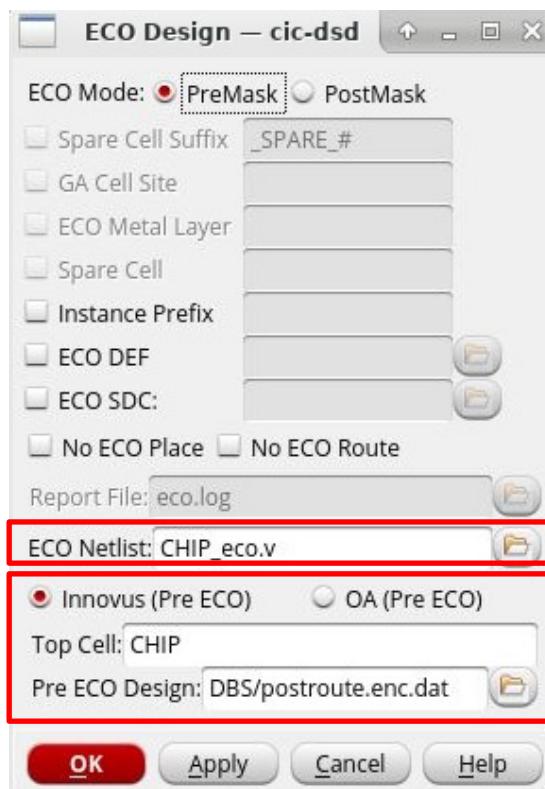
Congestion map

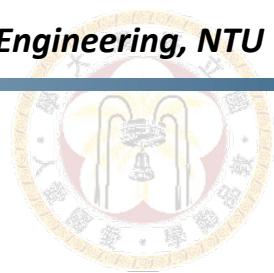




ecoDesign

- ***File → ECO Design...***
 - Take an Innovus database and a modified netlist as input and performs ECO operation
- ***ecoDesign***





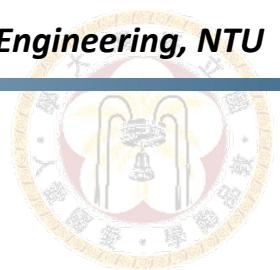
ECO Command

ECO command

```
ecoAddRepeater  
ecoDeleteRepeater  
ecoChangeCell  
ecoPlace  
ecoRoute  
addInst  
deleteInst  
addNet  
deleteNets  
attachTerm  
detachTerm
```

Set ECO mode

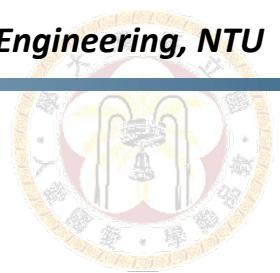
```
setEcoMode -LEQCheck true  
setEcoMode -refinePlace false  
setEcoMode -updateTiming false  
setEcoMode -batchMode true
```



Interactive ECO

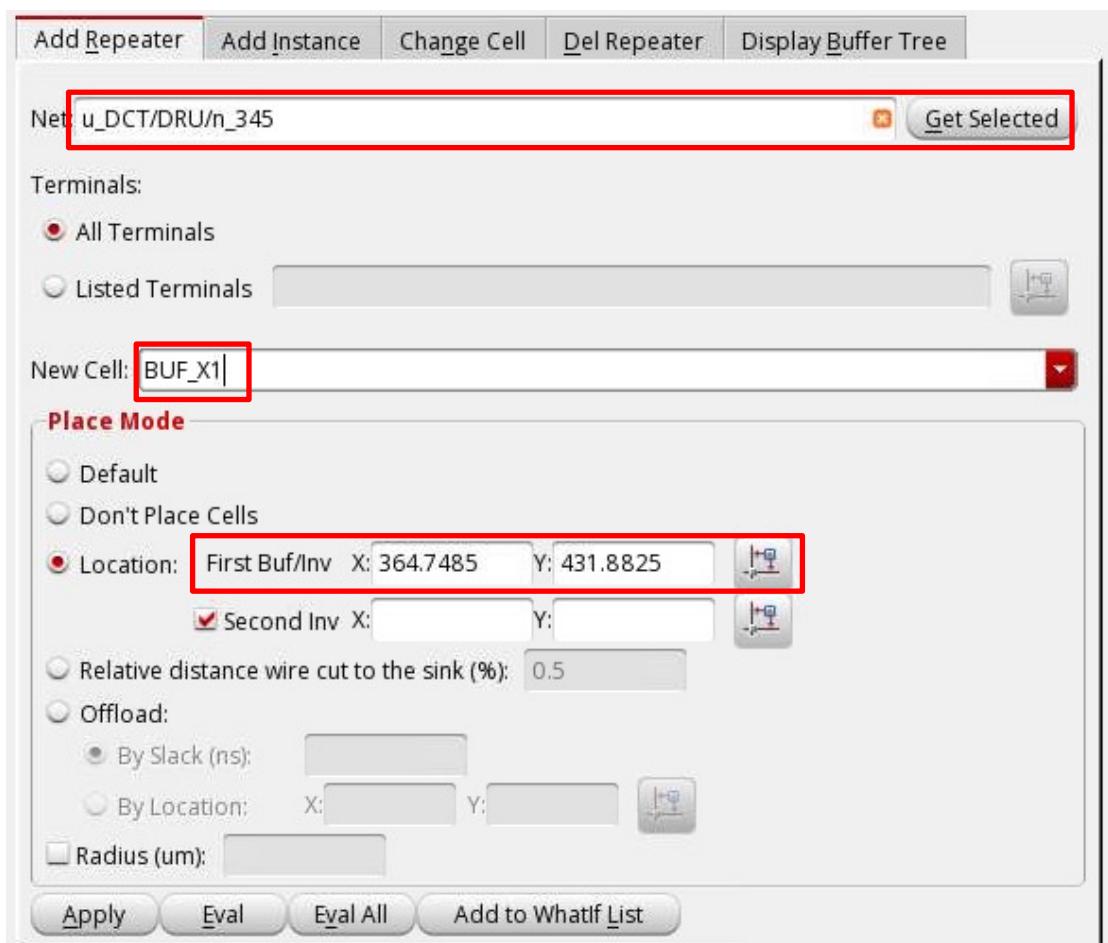
- **ECO → Interactive ECO...**
 - *ecoChangeCell*

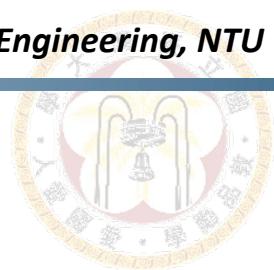




Interactive ECO

- **ECO → Interactive ECO...**
 - **ecoAddRepeater**

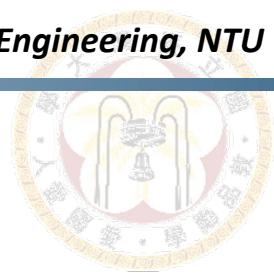




Interactive ECO

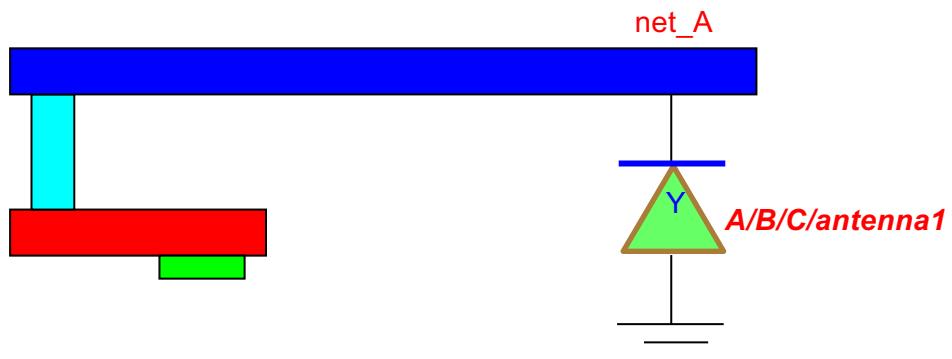
- **ECO → Interactive ECO...**
 - *ecoDeleteRepeater*

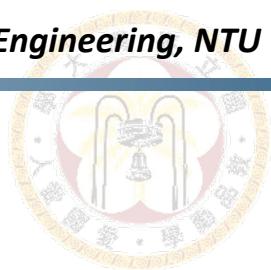




Manual Insert Antenna Diode

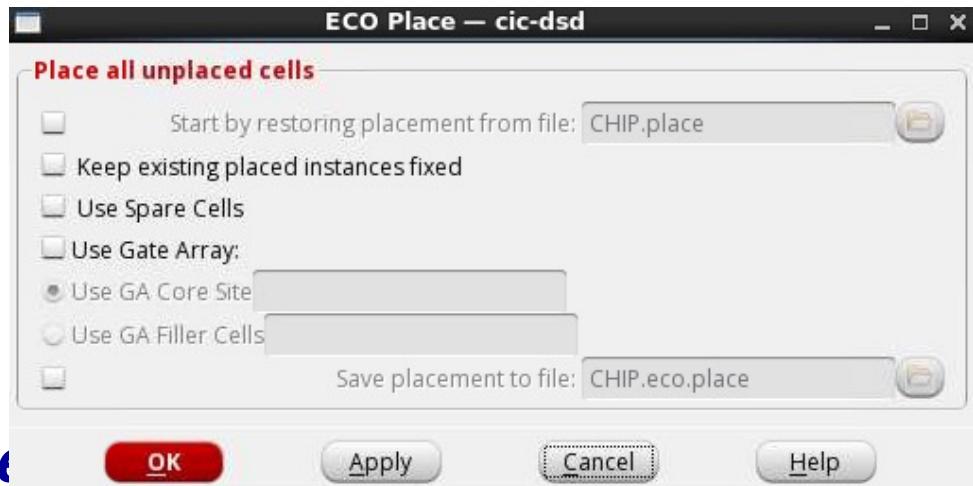
- Adds an antenna diode to a post-routed design.
 - *addInst -cell diodeCellName -inst {A/B/C/antenna1} -location 100 200*
 - *attachTerm A/B/C/antenna1 Y net_A*

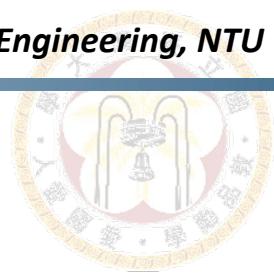




ECO Placement

- **Place → ECO Placement...**
 - Incrementally places unplaced standard cells

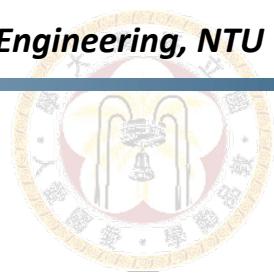




ECO Routing

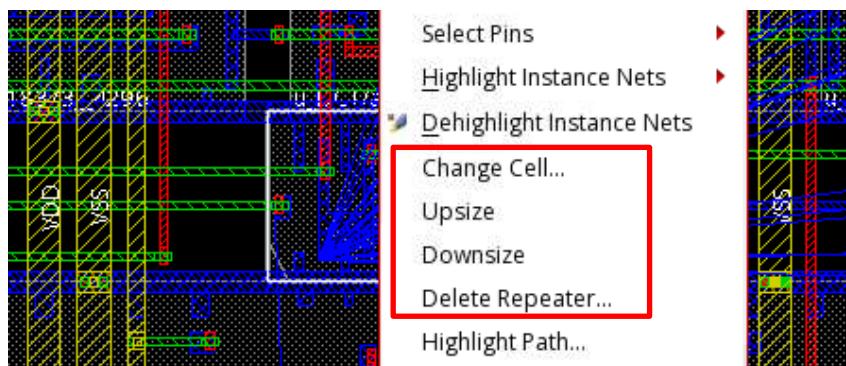
- **Route → NanoRoute → Route**
 - Performs incremental ECO routing on newly placed ECO cells.



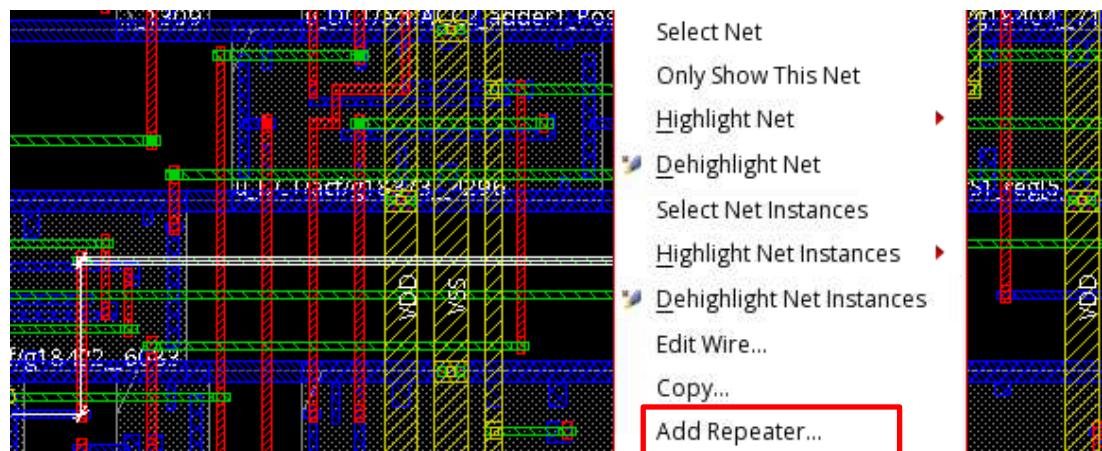


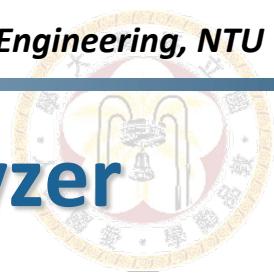
Interactive ECO from design area

- right-click on Instance



- right-click on Net





Interactive ECO from Timing Path Analyzer

- right-click on net or instance

The screenshot shows a software interface for a timing path analyzer. At the top, there is a navigation bar with tabs: Data Path, Launch Clock, Capture Clock, Path SDC, and Timing Interpretation. Below the navigation bar, the title "Data Delay" is displayed in red. A table lists various timing arcs with their corresponding cells and delays. One specific row, "u_IDCT/Y[0]", is highlighted with a gray background. A context menu is open over this row, with several options visible: Copy Cell, Interactive ECO/Whatif (which is highlighted with a red border), Save For Target Based Opt, View in Design Browser, Edit Table Column, Get Attribute, Get Net Wire Length, Report Net Parasitics, and Report Net. To the right of the table, a vertical "Hierarchy View" pane shows a tree structure with the root node "u_IDCT".

Name	Arc	Cell	Delay
u_IDCT/tposemem_Bisted_RF_2P_ADV64x...	CK->Q	SDFF_X1	0.220
u_IDCT/tposemem_BistFail			0.000
u_IDCT/g3355	A1->ZN	NAND2_X1	0.055
u_IDCT/n_217			0.000
u_IDCT/g333	A2->ZN	NAND2_X1	0.082
u_IDCT/Y[0]			0.000