

# Computer-Aided VLSI System Design

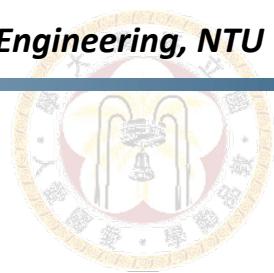
## Chapter 7. Cell-based APR Flow Part1

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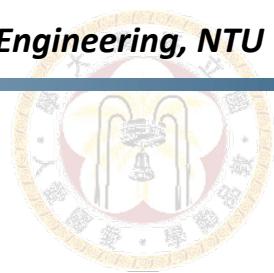


NTU GIEE

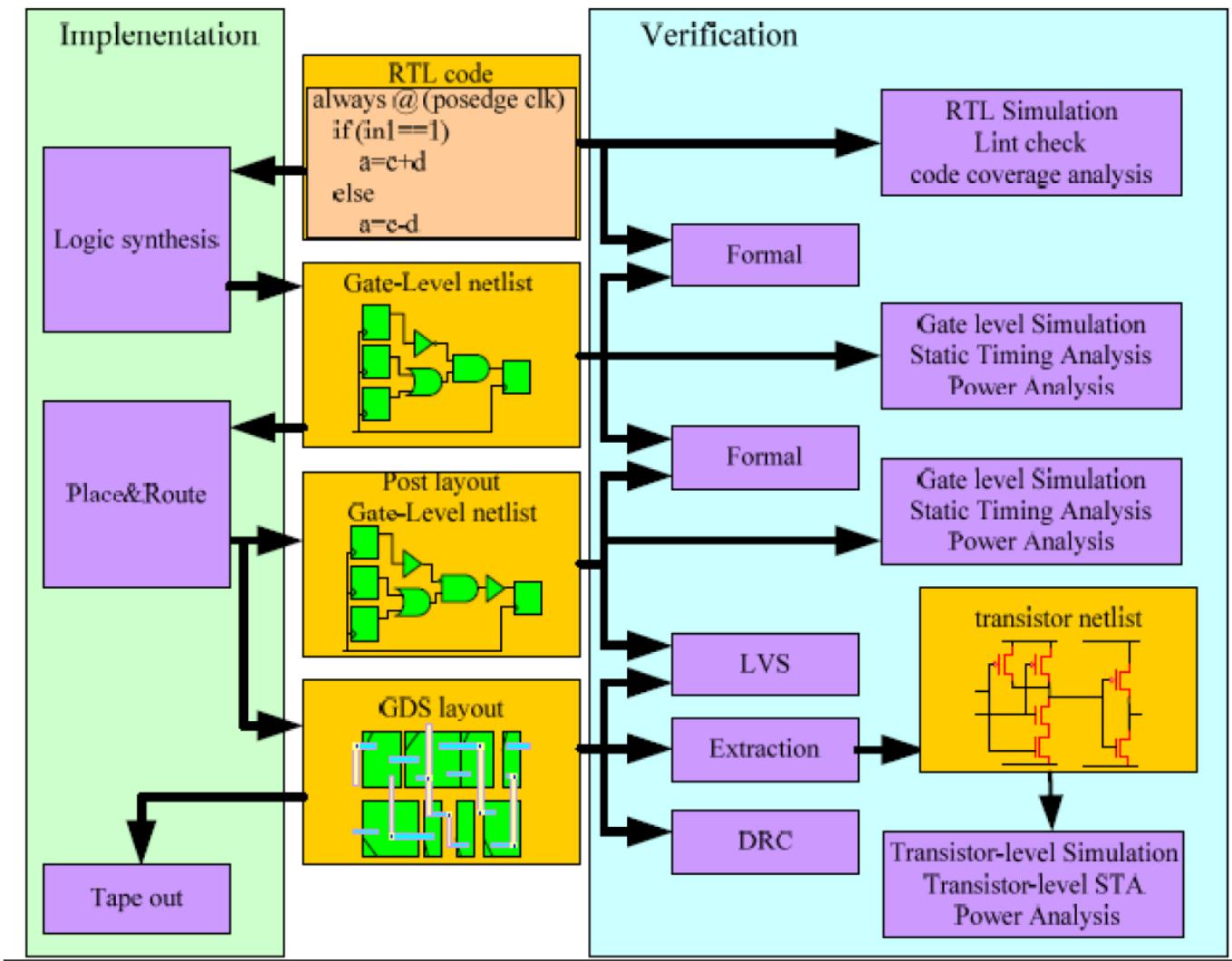


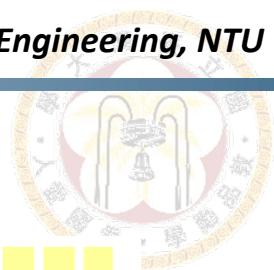
# Outline

- **Introduction**
- **Data Preparation**
- **Automatic Place & Route – Innovus**
  - Design Import
  - Floorplan Specification



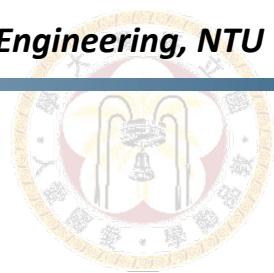
# Cell-Based Design Flow



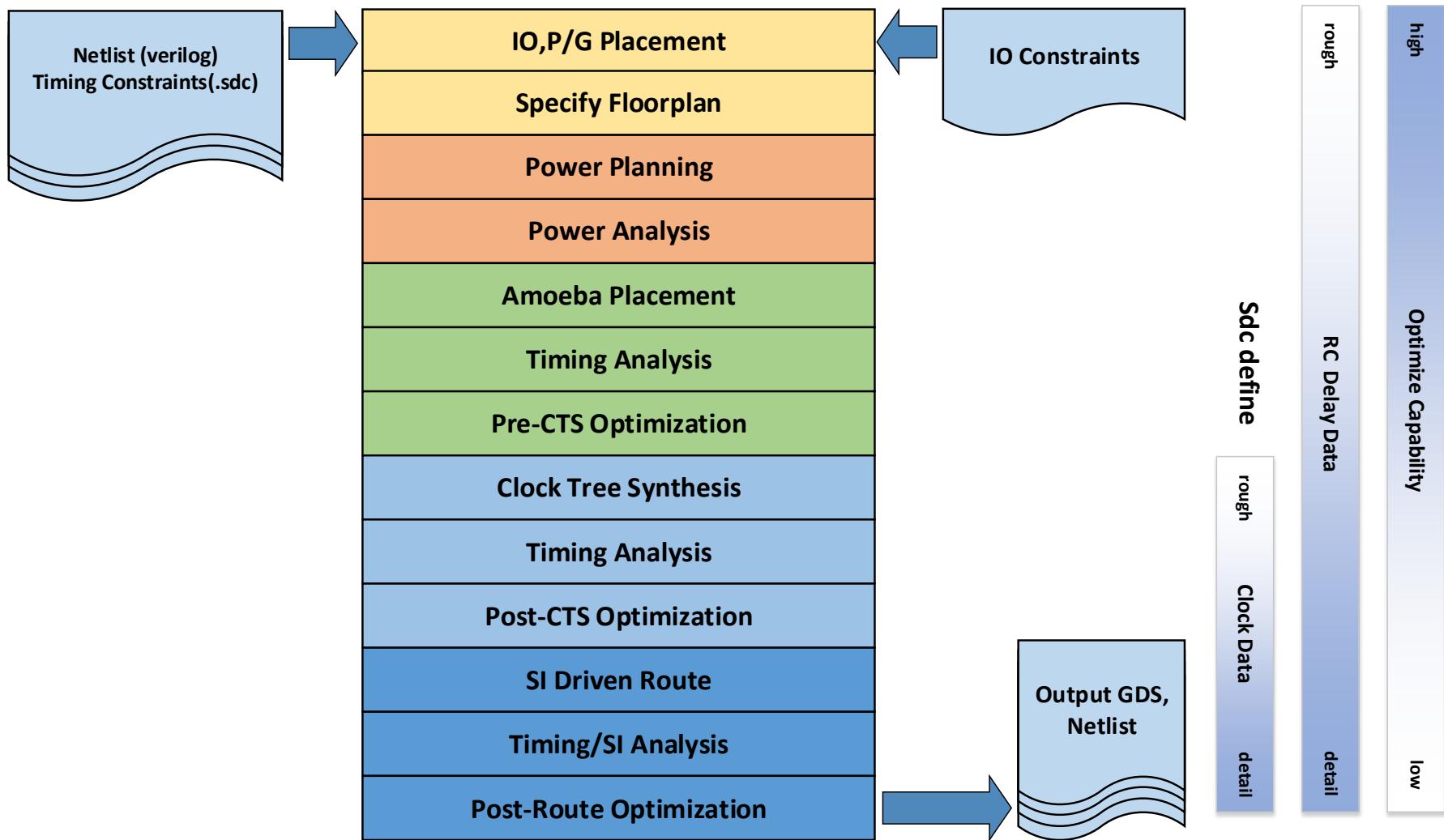


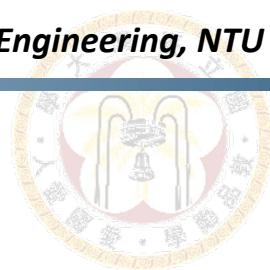
# Cell Library

function	NAND	NOR	XOR	INV	ADD	FF	.....
schematic							
layout							
symbol			.....	.....	.....	.....	.....
timing	A1→O 0.1ns A2→O 0.2ns	A1→O 0.1ns A2→O 0.2ns					
power	A1→O 0.1pw A2→O 0.2pw	A1→O 0.1pw A2→O 0.2pw					
abstract							



# Innovus P&R Flow





# Elements In the Design

## ■ Design element

### — IO Pad

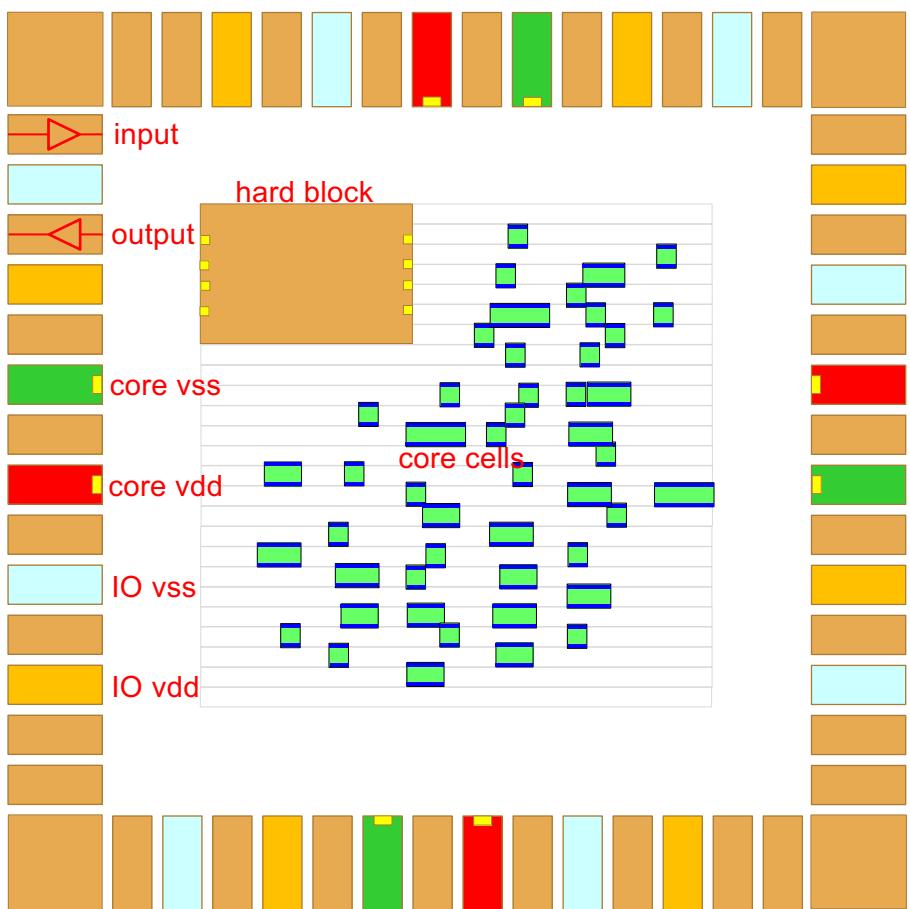
- Input/Output/Bidir Pad
- Core Power/Ground Pad
- IO Power/Ground Pad
- Analog Power/Ground Pad
- Corner/IO filler/pwrcut ...

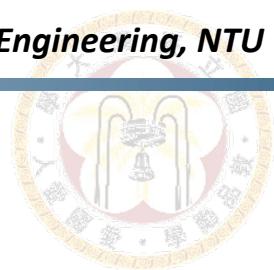
### — Standard Cell

- Logic Cell, AND/OR/XOR ...
- FlipFlop
- filler/antenna/welltap ...

### — Hard Block

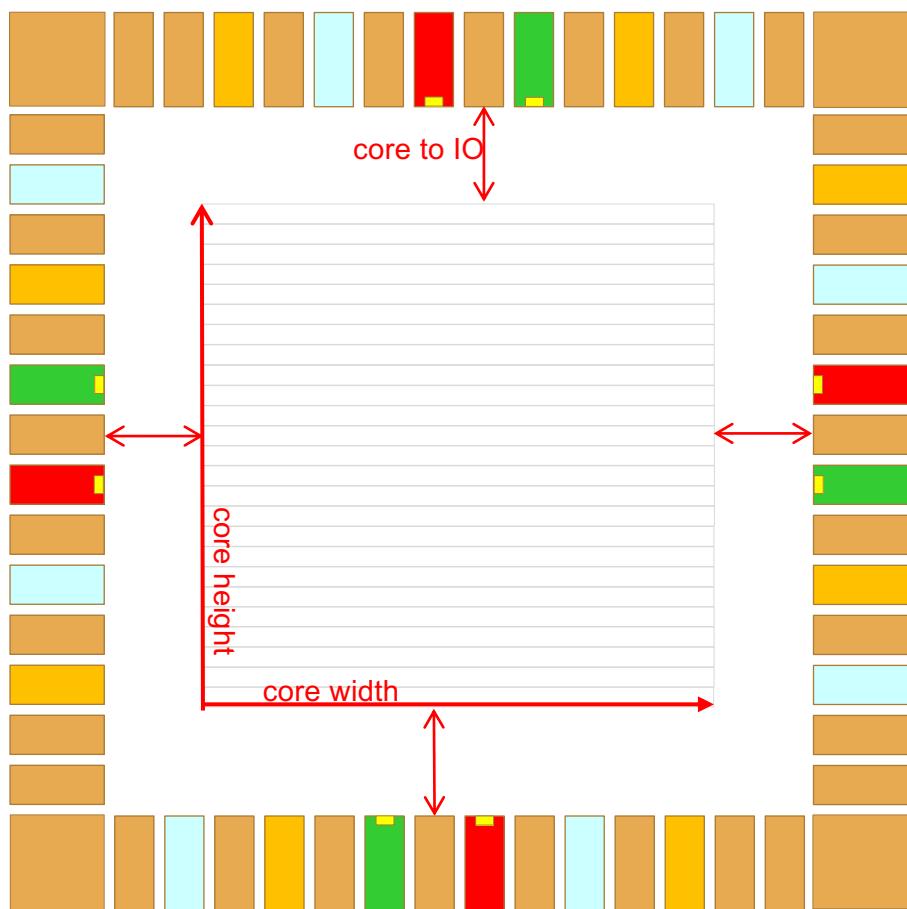
- SRAM
- PLL
- DDR/USB/MIPI ...

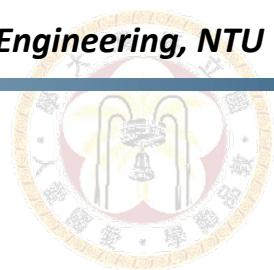




# Initial Floorplan

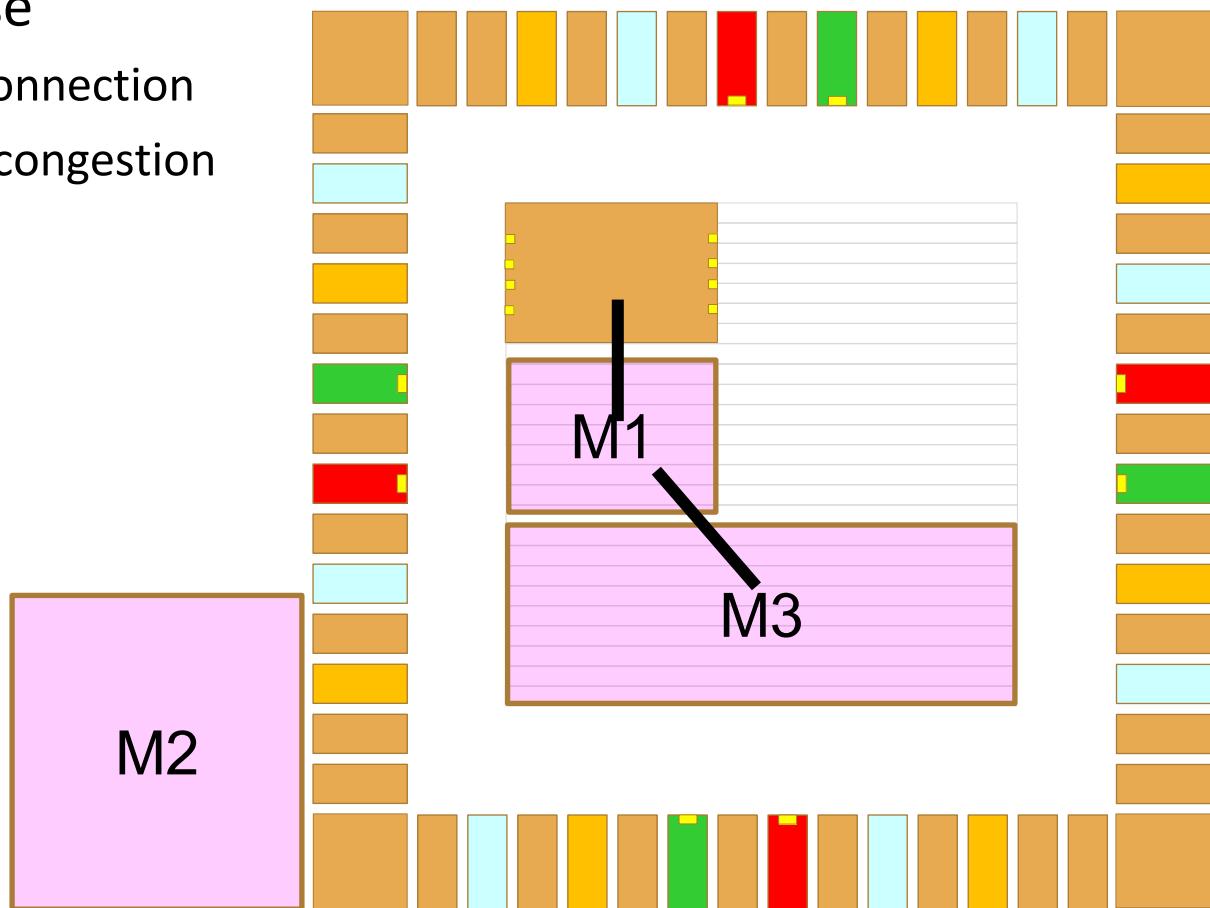
- Floorplan options
  - Channel width for power ring
  - Core utilization
  - Core area width/height
- Adjust IO ring
  - Signal pad order
  - Number of core PG pad
  - Number of IO PG pad
- Chip area is fixed after initial floorplan

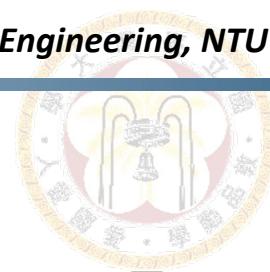




# Block and Module Floorplan

- Floorplan purpose
  - Robust power connection
  - Reduce routing congestion
  - Timing closure



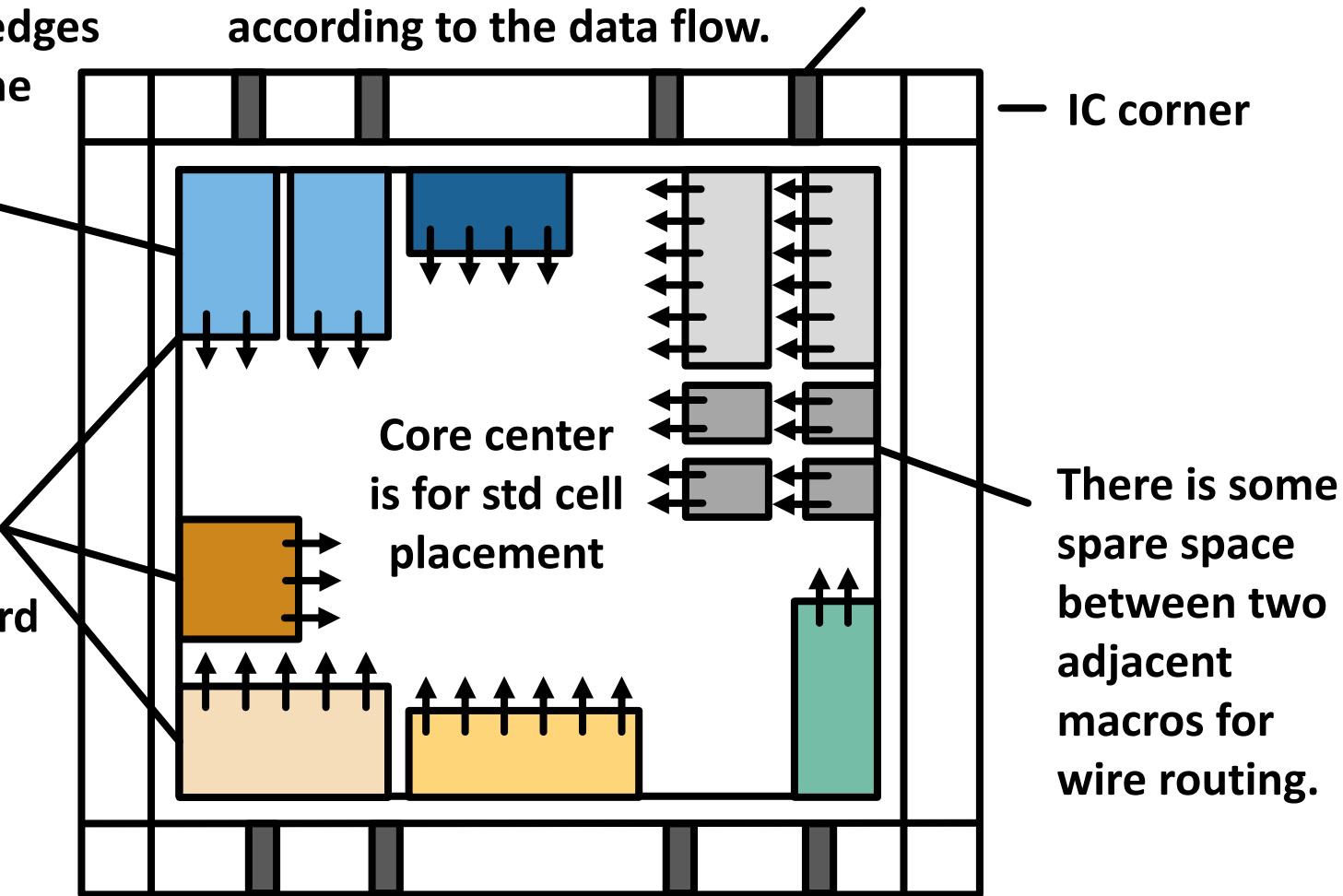


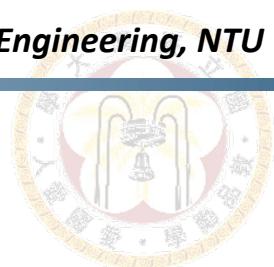
# Floorplan: How to Place Macros

All macros are placed on the edges or corners of the core region.

Macros are placed in groups, I/O pad according to the data flow.

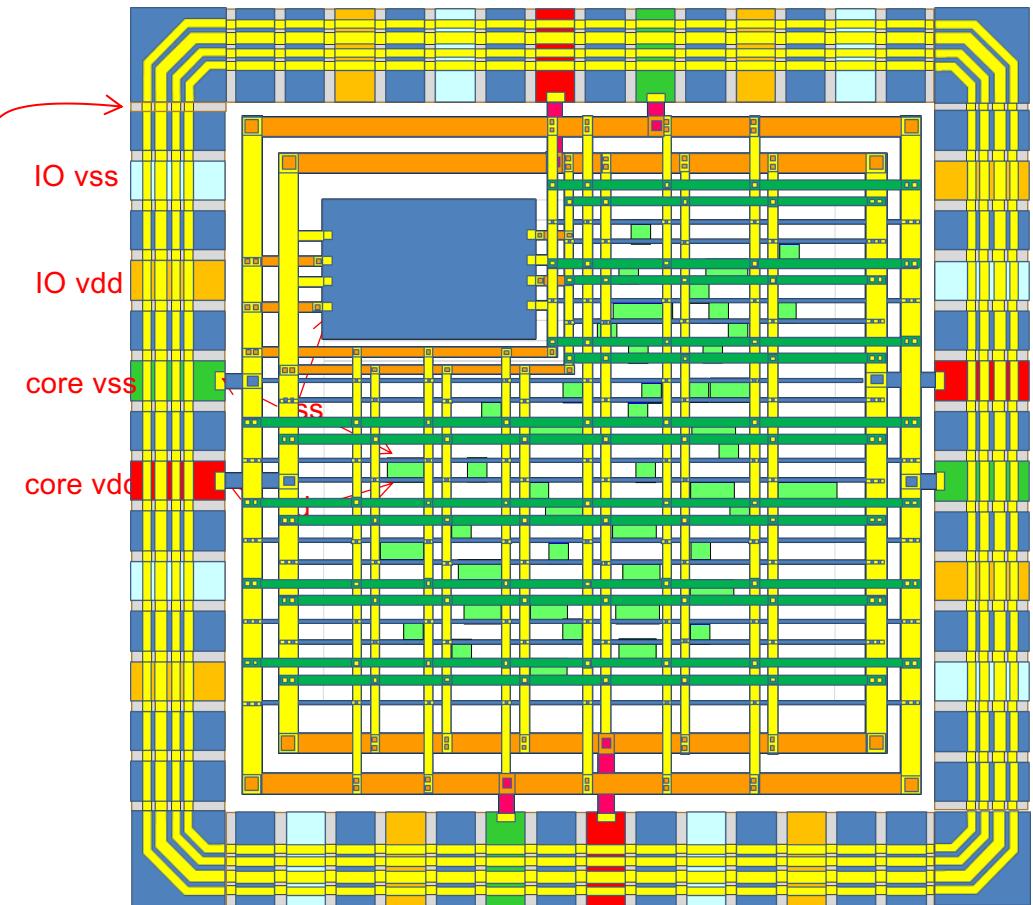
Directions of all output pins of macros are toward the core region.

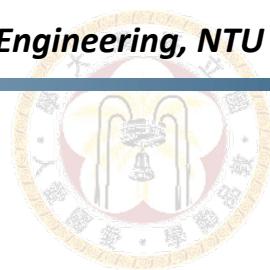




# Powerplan

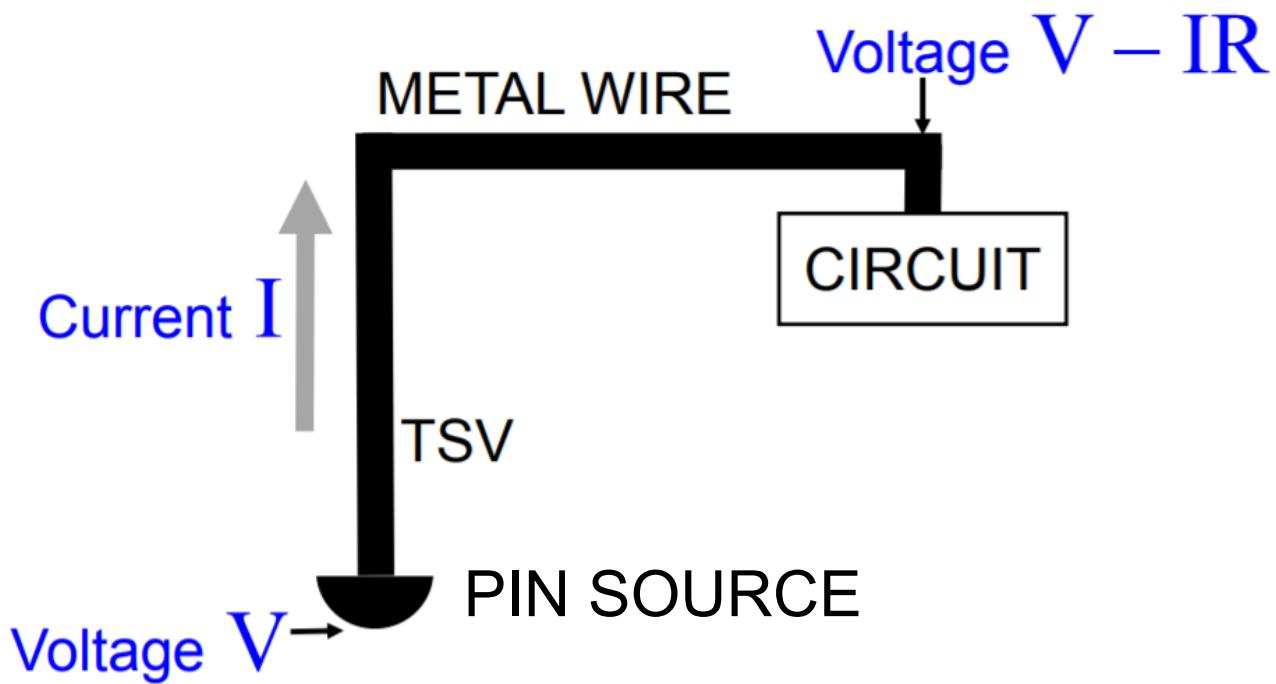
- Connect
  - IO pad power with
    - IO Corner
    - IO pad filler
  - Standard Cell with
    - Power ring
    - Power mesh
    - Follow pin
  - Hard Block with
    - Block ring if needed

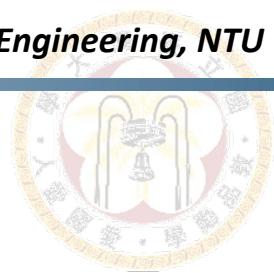




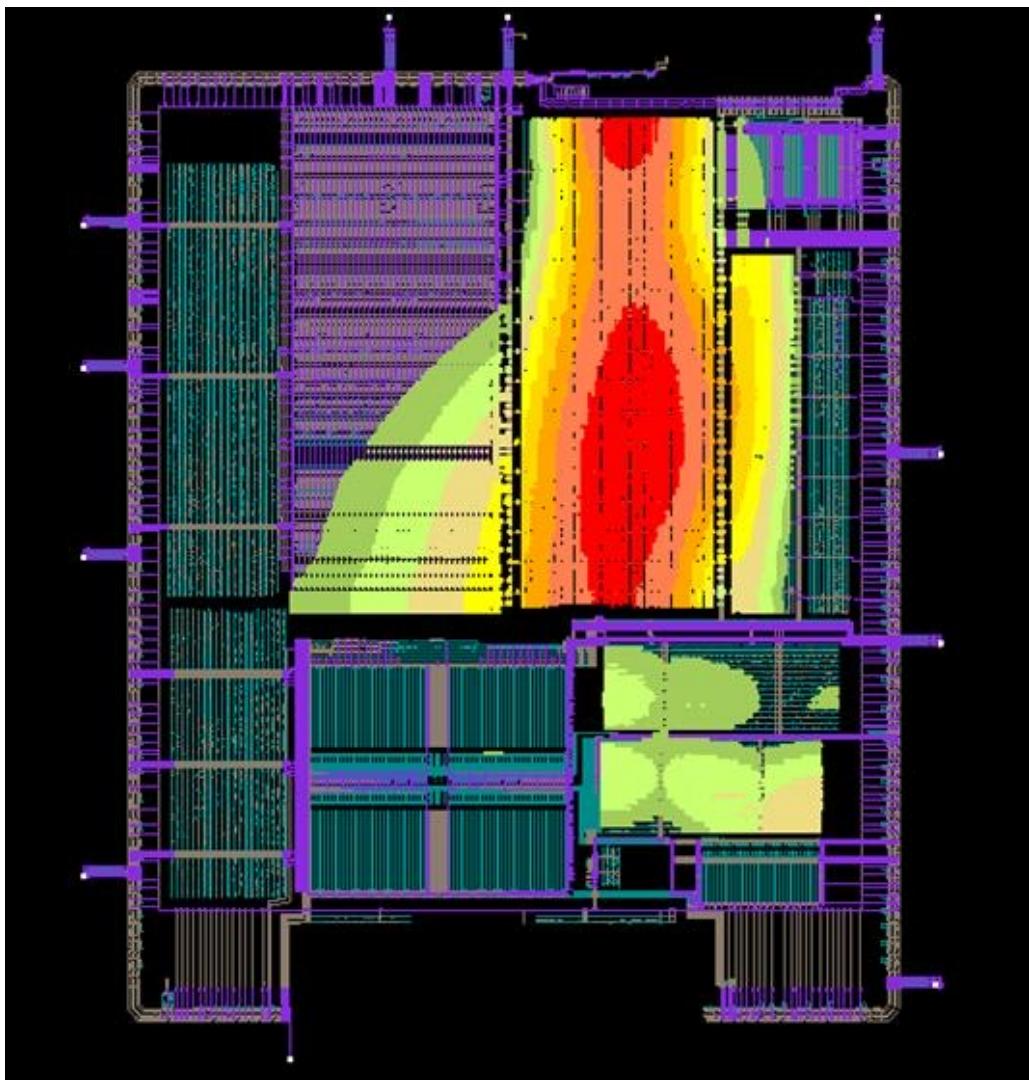
# IR Drop Issue

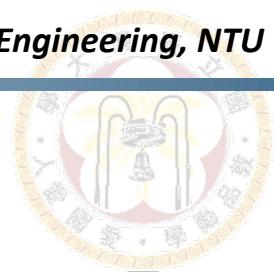
- A phenomenon that voltage drops in an integrated circuit due to the resistance of the metal wire interconnect
- Delay will increase and violate timing constraints w/ IR drop





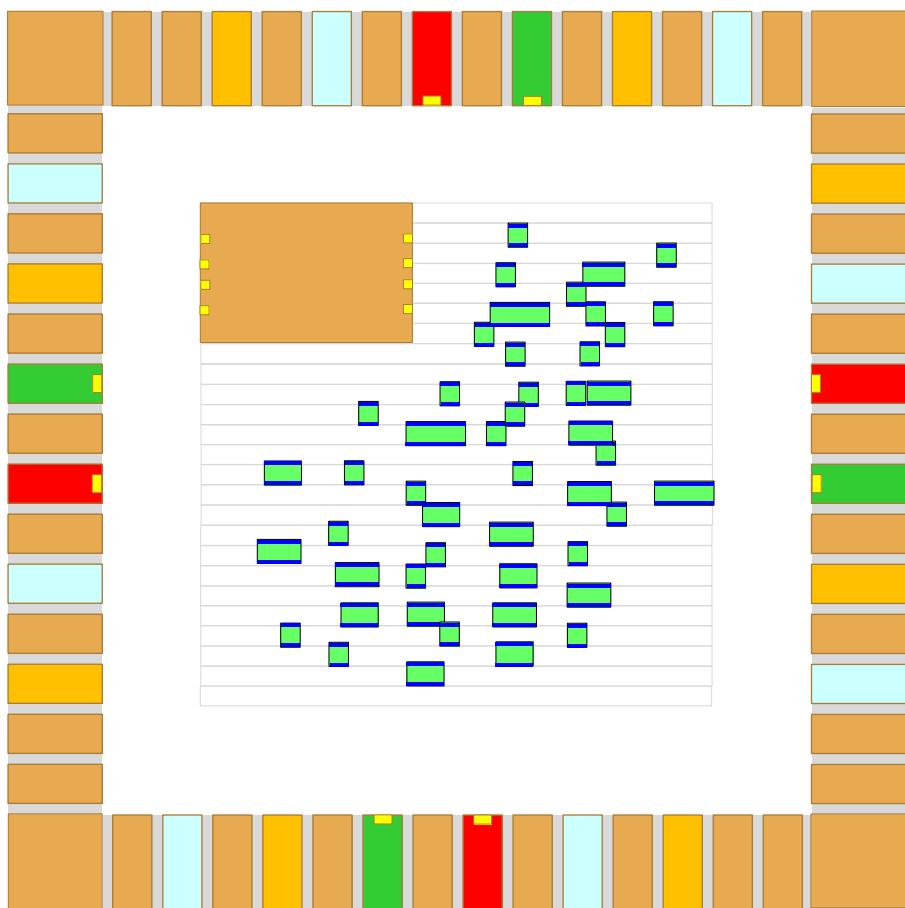
# IR Drop Plot

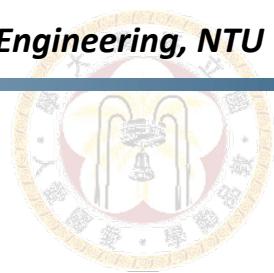




# Placement & optimization

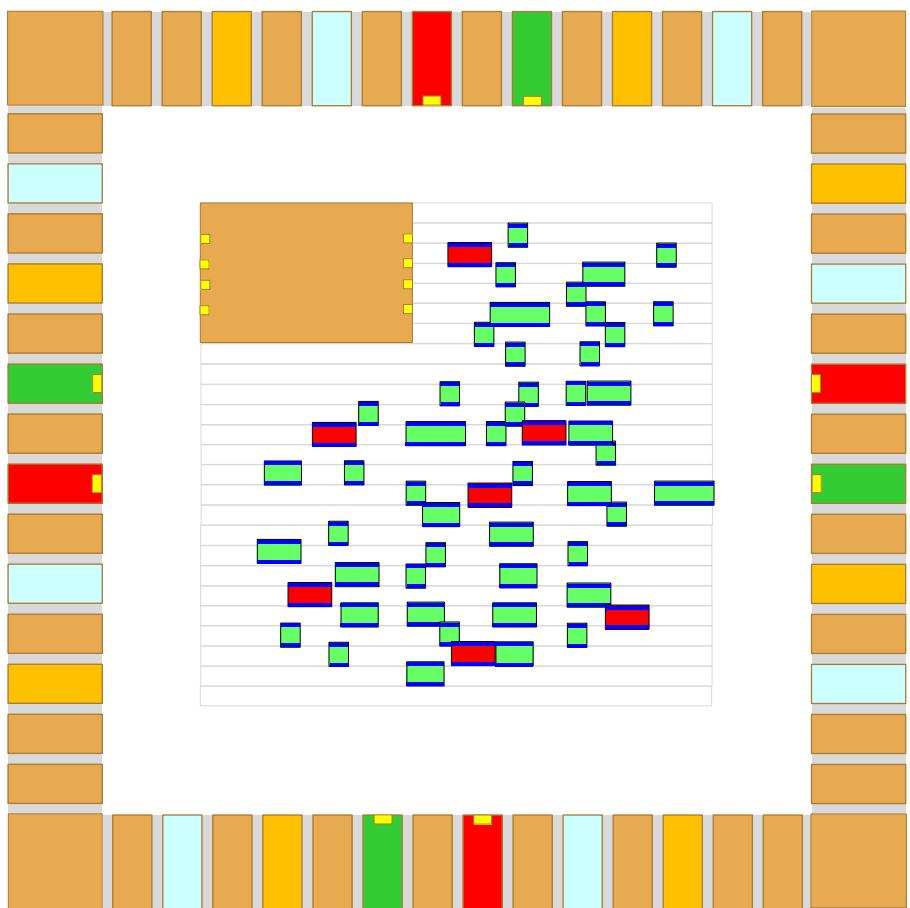
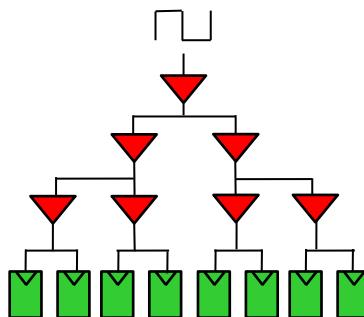
- Placement & Opt
  - Module plan
  - Congestion effect
  - Setup/Hold slack
  - Clock gating aware
  - Power driven
  - DRV

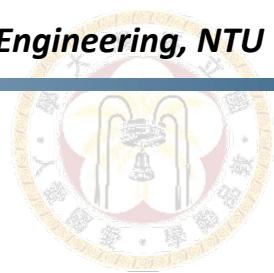




# Clock Tree Synthesis

- Clock is Ideal before CTS
- CTS goal
  - Balance clock
  - Meet Setup/Hold timing

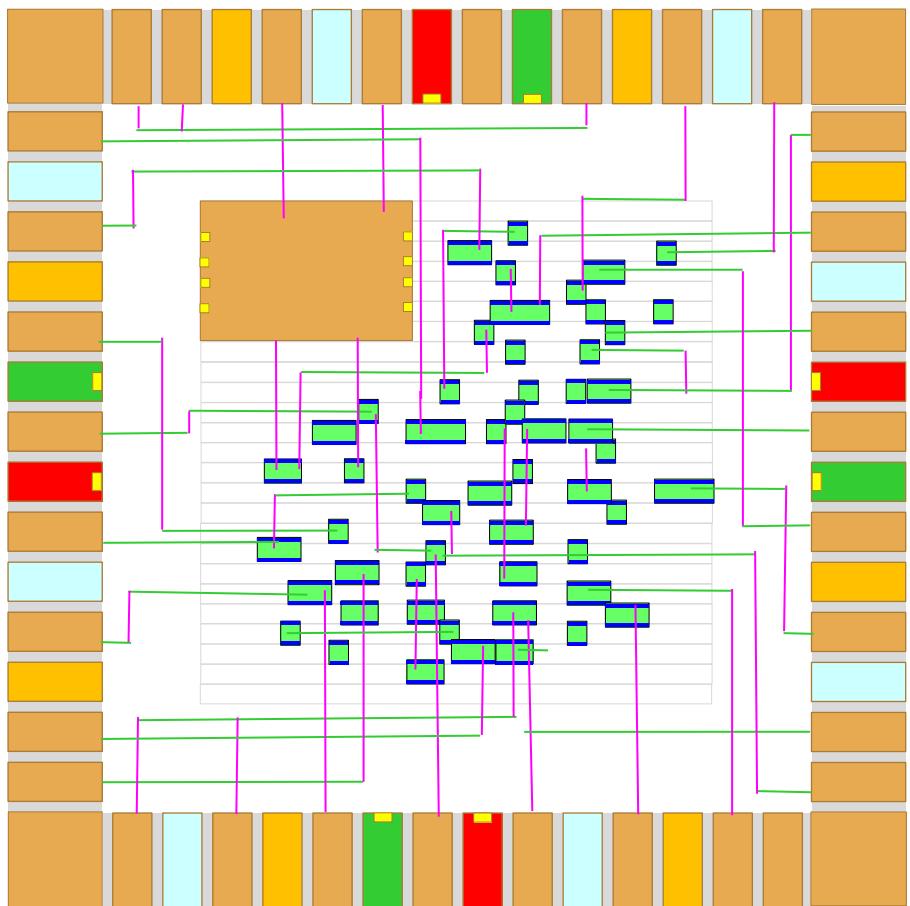


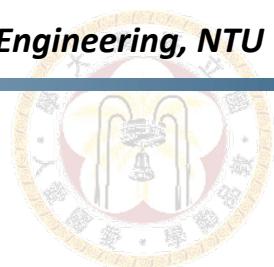


# Routing

## ■ Routing feature

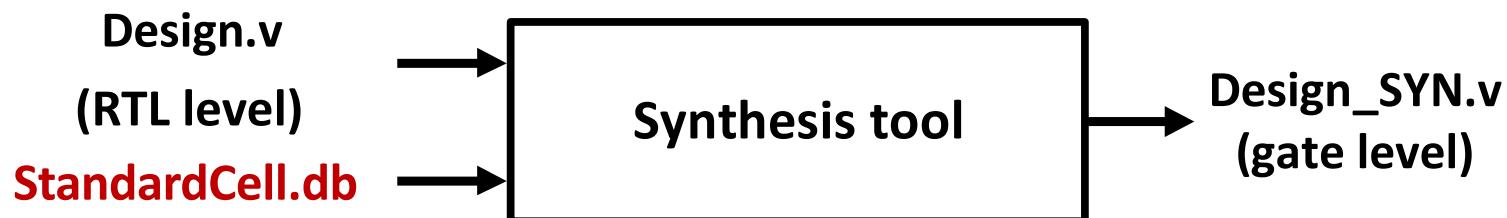
- Timing driven
- Signal Integrity
- Antenna repair
- Non default rule
- Shielding
- Via optimization
- Layer aware
- Double pattern





# Review Cell-based Design Flow

- RTL coding
- Synthesis



- Physical implementation



- Tool: Innovus, IC compiler ...

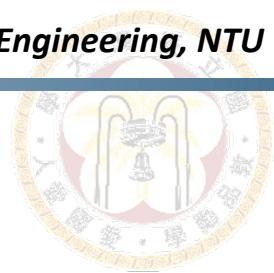
# Prepare Data

## ■ Library

- Physical Library (.lef)
- Timing Library (.lib)
- Capacitance Table (.capTbl)
- Celtic Library (noise information)

## ■ User Data

- Gate-level Netlist (verilog)
- SDC Constraints
- IO Constraints
- Scan def



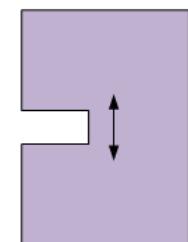
# DRC & LVS (1/2)

## ■ Design Rule Checking (DRC)

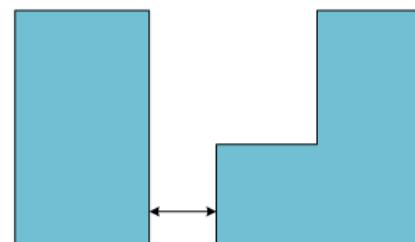
- Verify a specific design meets the constraints imposed by the process technology to be used for its manufacturing

- For examples

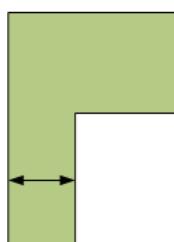
- Minimum spacing
- Minimum width
- Minimum edge length
- Encapsulation of Layer



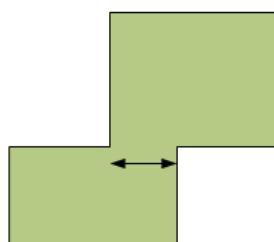
Edge  
Violation



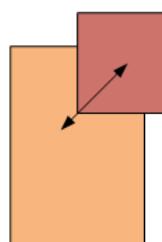
Spacing Violation



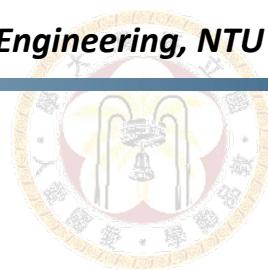
Width Violations



Width Violations



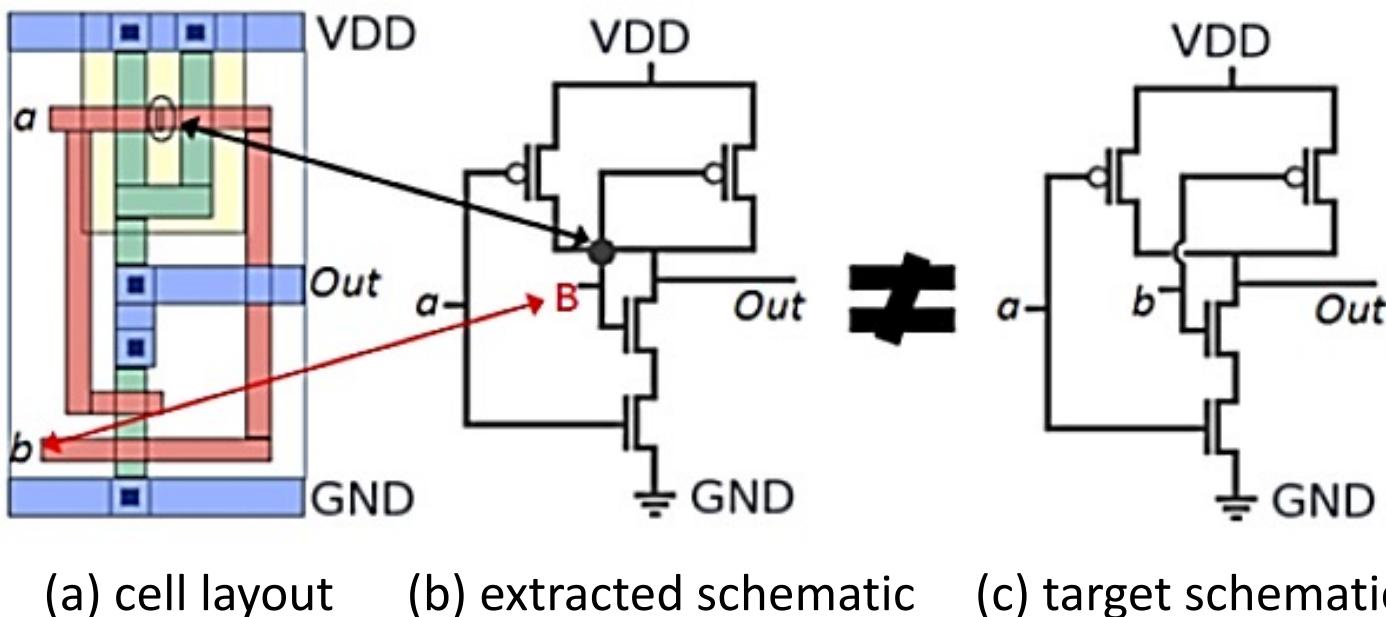
Encapsulation  
Violation

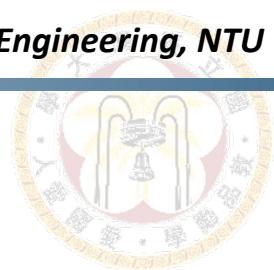


## DRC & LVS (2/2)

### ■ Layout Versus Schematic (LVS)

- Check the extracted netlist from the layout to the original schematic netlist to determine if they match





# LEF Format: Process Technology

## Layers

POLY

◆ Contact

Metal1

◆ Via1

Metal2

## Design Rule

Net width

Net spacing

Area

Enclosure

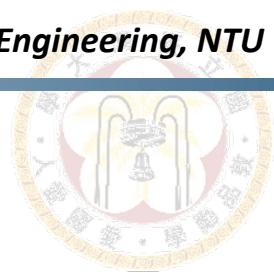
Wide metal slot

Antenna

Current density

## Parasitic

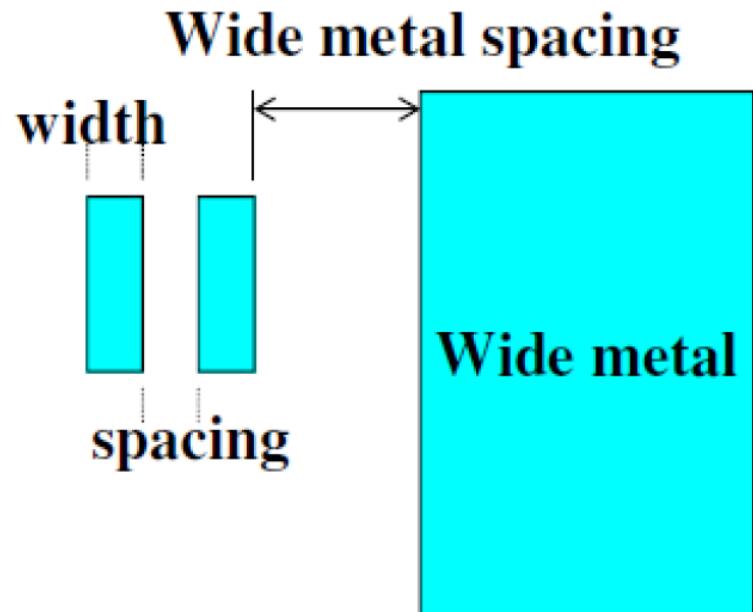
Resistance  
Capacitance

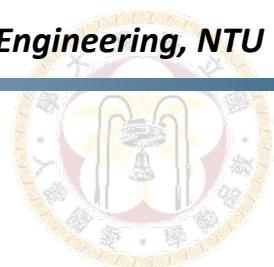


# LEF Format: Layer Definition

Layer Metal1

```
TYPE ROUTING ;
WIDTH 0.28 ;
MAXWIDTH 8 ;
AREA 0.202 ;
SPACING 0.28 ;
SPACING 0.6 RANGE 10.0 10000.0 ;
PITCH 0.66 ; // metal 1 to via
DIRECTION VERTICAL ;
THICKNESS 0.26 ;
ANTENNACUMDIFFAREARATIO 5496 ;
RESISTANCE RPERSQ 1.0e-01 ;
CAPACITANCE CPERSQDIST 1.11e-04 ;
EDGECAPACITANCE 9.1e-05 ;
END Metal1
```

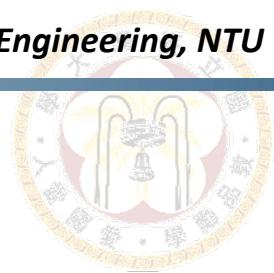




# LEF Format: APR Technology

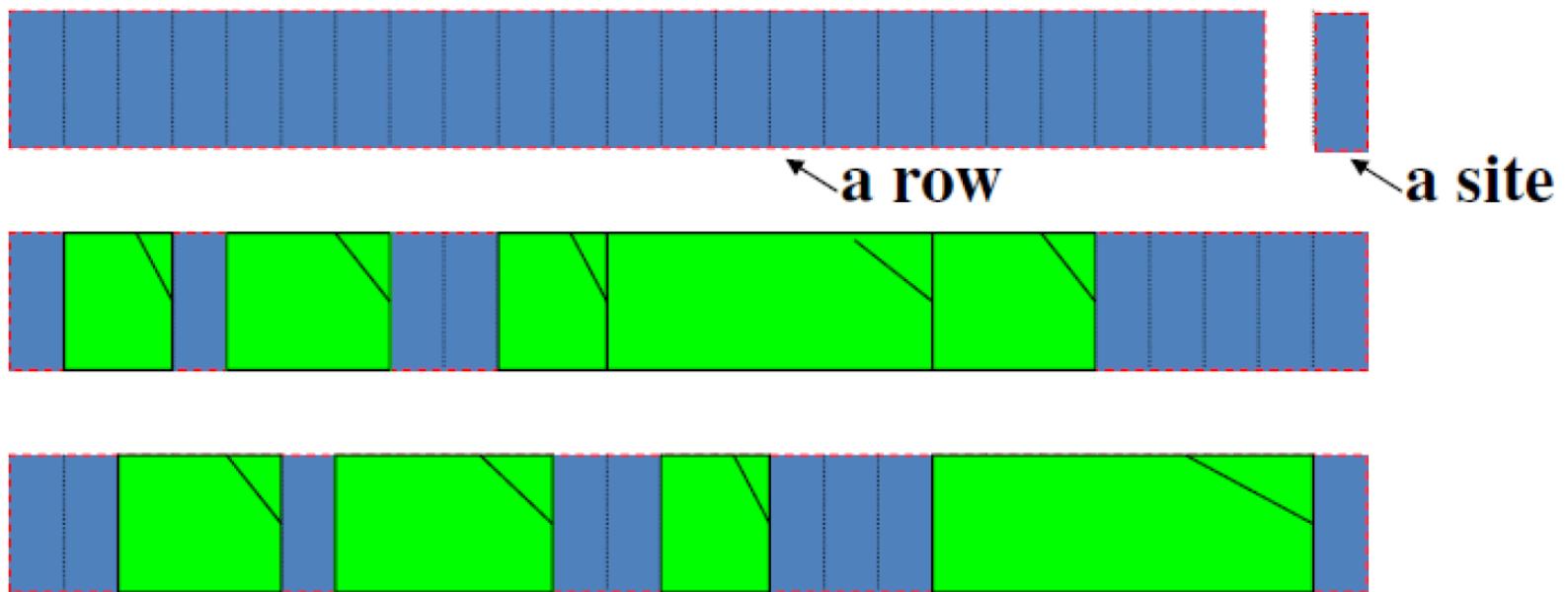
- Unit
- Site
- Routing pitch
- Default direction
- Via rule
  
- More information

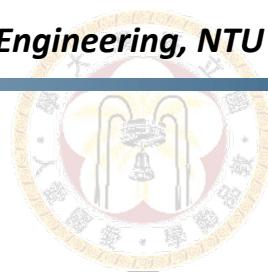
<http://www.ispd.cc/contests/18/lefdefref.pdf>



# LEF Format: Definition of SITE

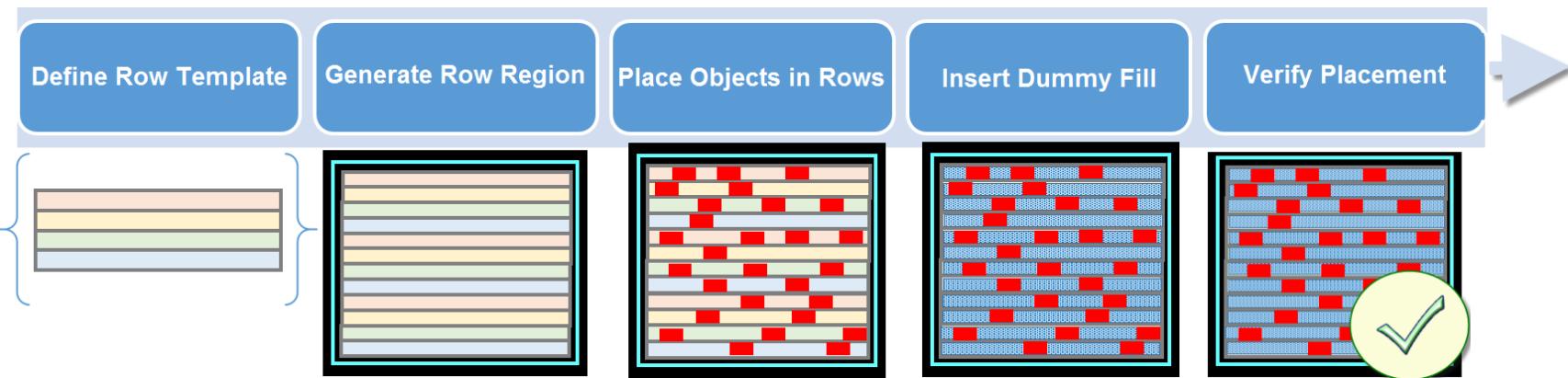
- A placement **SITE** gives the placement grid for a family of macros
  - E.g. I/O, core, block, analog, digital, short, tall, and so forth
- Can be used in DEF ROW statements

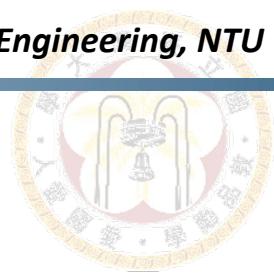




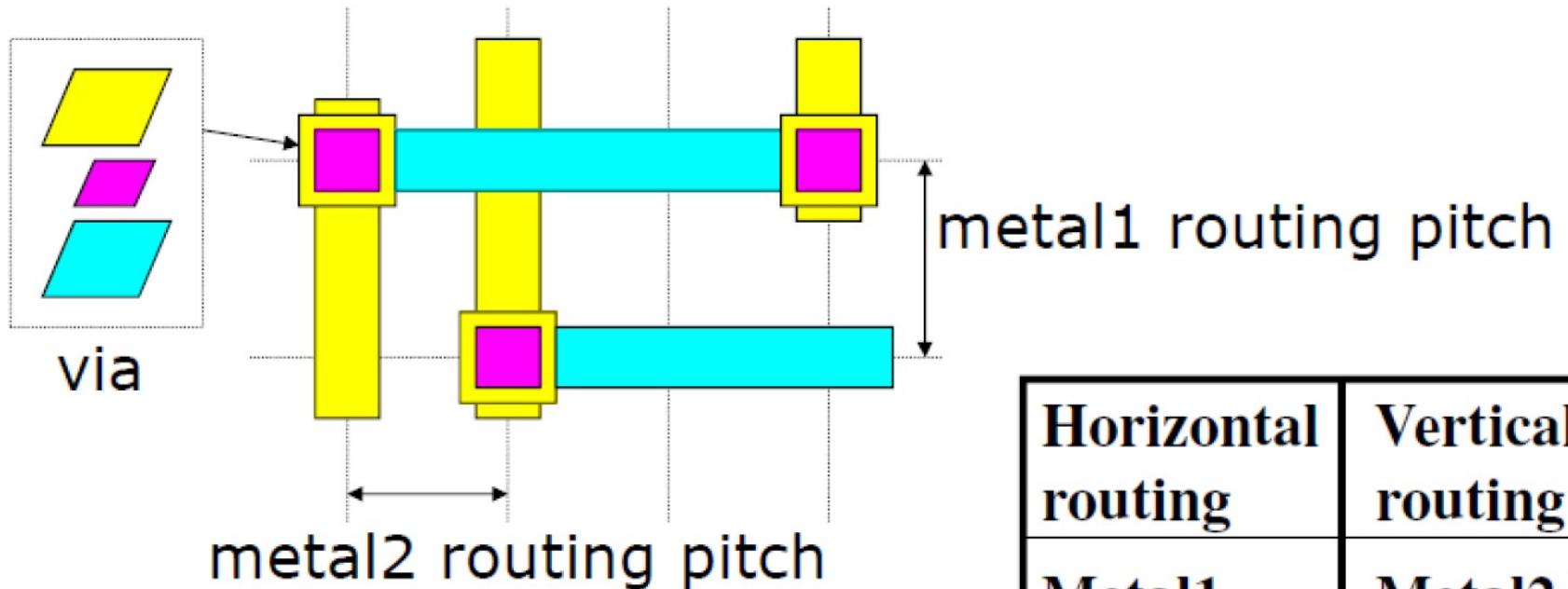
# Row-Based Place & Route

- **Deterministic layout**
  - Poly and active density is better controlled
  - More predictable layout-dependent effects (LDE)
- **Increased layout efficiency**
  - Reduced number of design-layout cycles
- **Room for automation**

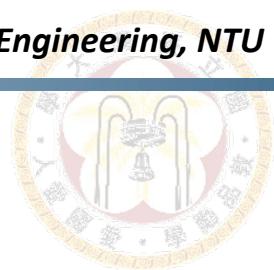




# LEF Format: Routing Pitch

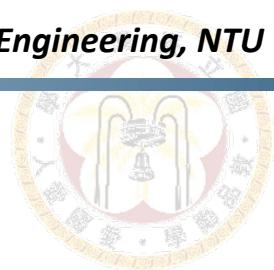


Horizontal routing	Vertical routing
Metal1	Metal2
Metal3	Metal4
Metal5	Metal6



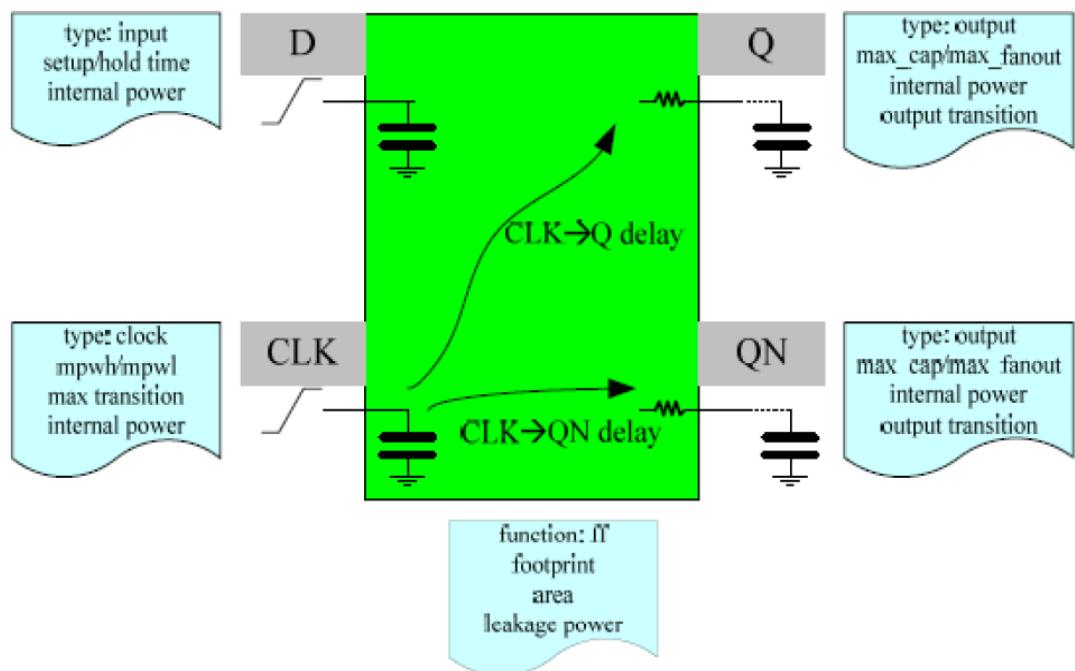
# LEF Format: Physical Macros

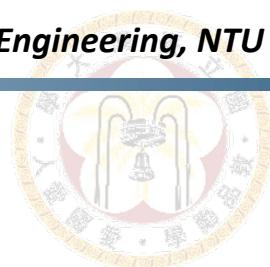
- **Define physical data for**
  - Standard cells
  - I/O pads
  - Memories
  - Other hard macros
- **Describe abstract shape**
  - Size
  - Class
  - Pins
  - Obstructions



# LIB Format (CCS, NLDM, ECSV)

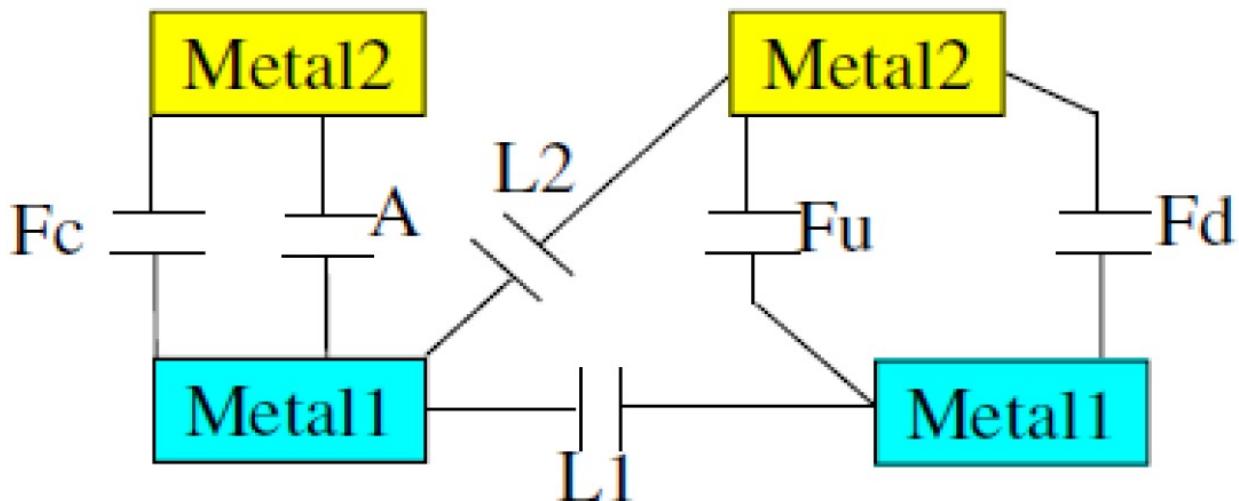
- Operating condition
  - slow, fast, typical
- Pin type
  - input/output/inout
  - function
  - data/clock
  - capacitance
- Path delay/transition
- Internal power
- Timing constraint
  - setup, hold...

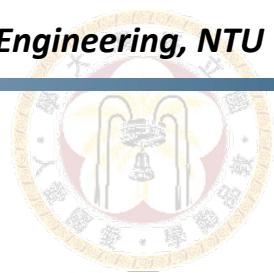




# Capacitance Table

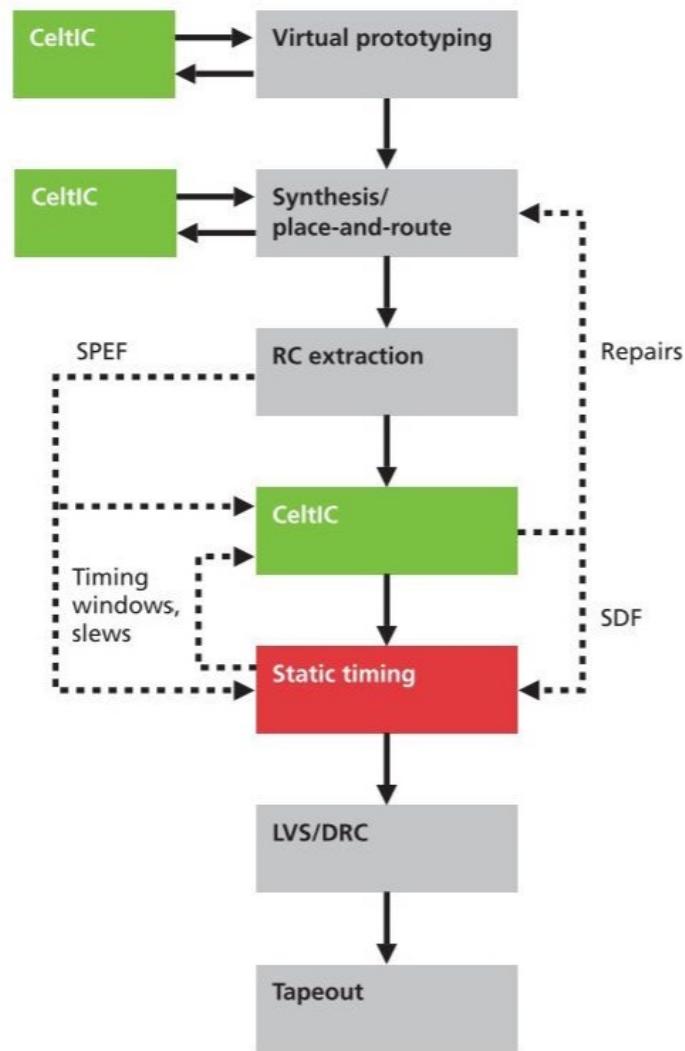
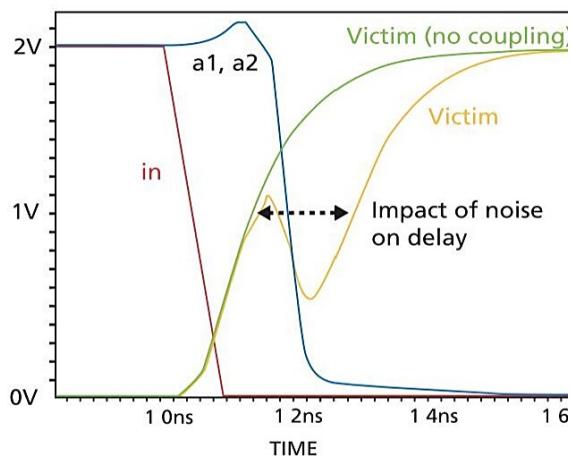
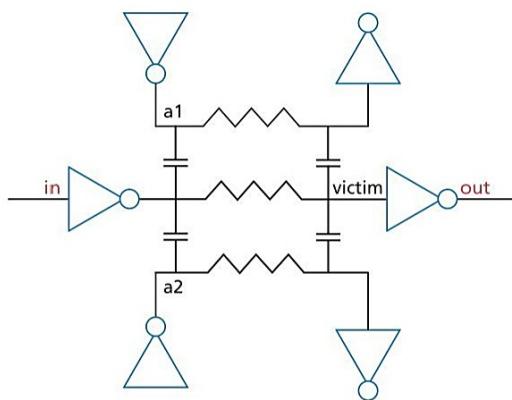
- **CapTable**
  - $\text{cap\_value} = f(\text{configuration}, \text{width}, \text{spacing})$
- **CapModel**
  - CapTable contains the area, fringe and lateral coupling capacitance coefficients organized per layer

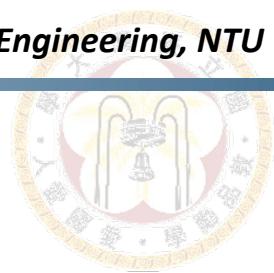




# CeltIC Signal Integrity Analyzer

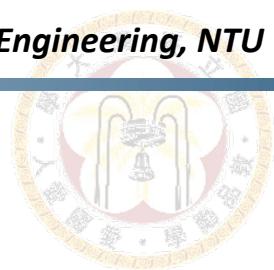
- Identify nets w/ low noise immunity
- Avert noise-related problem & lethal silicon failures before tapeout
- Accurately calculate the impact of noise on delay & functionality of cell-based design





# Generate Gate-Level Netlist

- IO pads should be added before the netlist is imported
- Remove “assign” statement before APR
  - To remove “assign” statement in synthesis tool (in syn.tcl)  
**set\_fix\_multiple\_port\_nets -all -buffer\_constraints**
  - To remove “assign” statement in Innovus  
**Innovus #> set init\_remove\_assigns 1**
- Make sure that there is no “\*cell\*” net name in netlist (in syn.tcl)
  - Use the synthesis commands (DC) below to remove “\*cell\*” cell name  
**define\_name\_rules name\_rule1 -map {{\\*\cell\\*\ cell}}**  
**change\_names -hierarchy -rules name\_rule1**
- Ensure the names of all instantiated cell types are unique  
**Innovus #> set init\_design\_uniquify 1**



# IO Constraints

```
module M (O1, I1, I2);
    output O1;
    input I1;
    input I2;
endmodule;
```

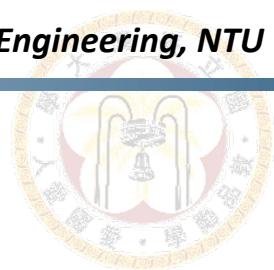
Original design (M.v)



```
module M (O1, I1, I2);
    output O1;
    input I1;
    input I2;
endmodule;

module CHIP (O1, I1, I2); // top module with I/O pads
    output O1;
    input I1, I2;
    wire i_I1, i_I2, i_O1;
    M M (.O1(i_O1), .I1(i_I1), .I2(i_I2));
    PDIDGZ Pad_I1 (.PAD(I1), .C(i_I1));
    PDIDGZ Pad_i2 (.PAD(I2), .C(i_I2));
    PDO12CDG Pad_O1(.PAD(O1), .I(i_O1));
endmodule;
```

Modified design (CHIP\_syn.v)

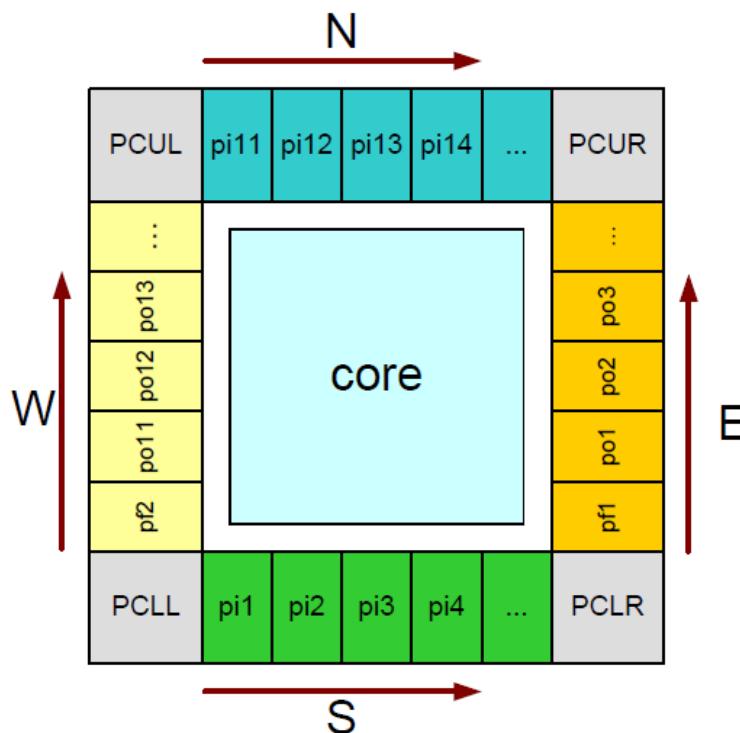


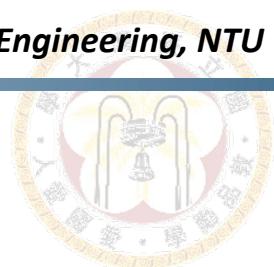
# I/O Files

- Example of IO pad location file

**CHIP.ioc**

Version: 2		
Pad: pi1	S	
Pad: pi2	S	
Pad: pi3	S	
Pad: pi4	S	
.....		
Pad: pf1	E	PFILL
Pad: po1	E	
Pad: po2	E	
Pad: po3	E	
.....		
Pad: pi11	N	
Pad: pi12	N	
Pad: pi13	N	
Pad: pi14	N	
.....		
Pad: pf2	W	PFILL
Pad: po11	W	
Pad: po12	W	
Pad: po13	W	
.....		
Pad: PCLL	SW	PCORNER
Pad: PCLR	SE	PCORNER
Pad: PCUL	NW	PCORNER
Pad: PCUR	NE	PCORNER





# Getting Started for Innovus

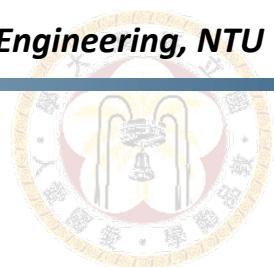
- Source the Innovus environment (at command line)

```
source /usr/cad/innovus/CIC/license.cshrc  
source /usr/cad/innovus/CIC/ innovus.cshrc
```

- Invoke Innovus (at command line)

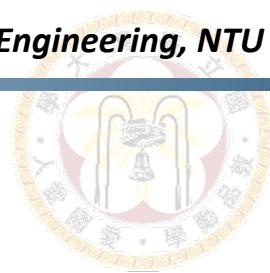
```
innovus
```

- Do not run in background mode (no &)
  - The terminal become the interface of command input while running Innovus



## Innovus Tips

- The executed command is saved in **innovus.cmd#**
- The executed log file is saved in **innovus.log#**
  
- Restart from each step by freeing/reloading design
  - Save design  
**Innovus #> saveDesign xxx**
  - Free Design  
**Innovus #> freeDesign**
  - Restore Design  
**Innovus #> innovus xxx.dat CHIP**



# GUI of Innovus

Menu

Tool  
widgets

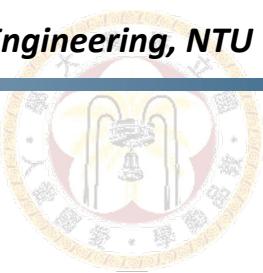


Design  
views

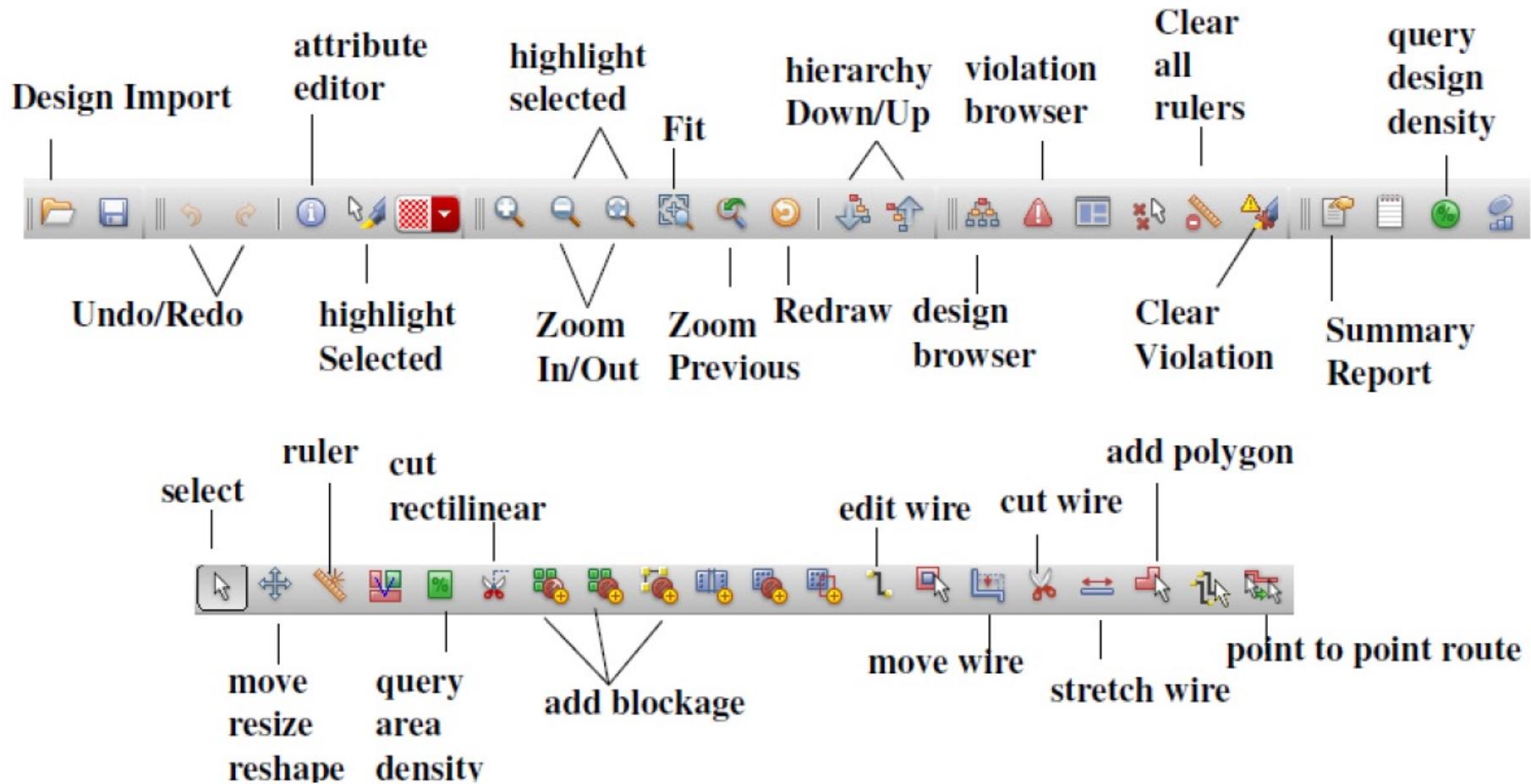
Display  
control

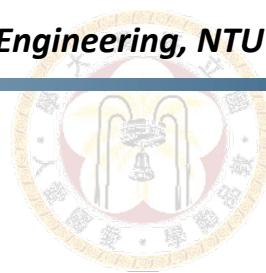
Selected  
objects

Cursor  
coordinates



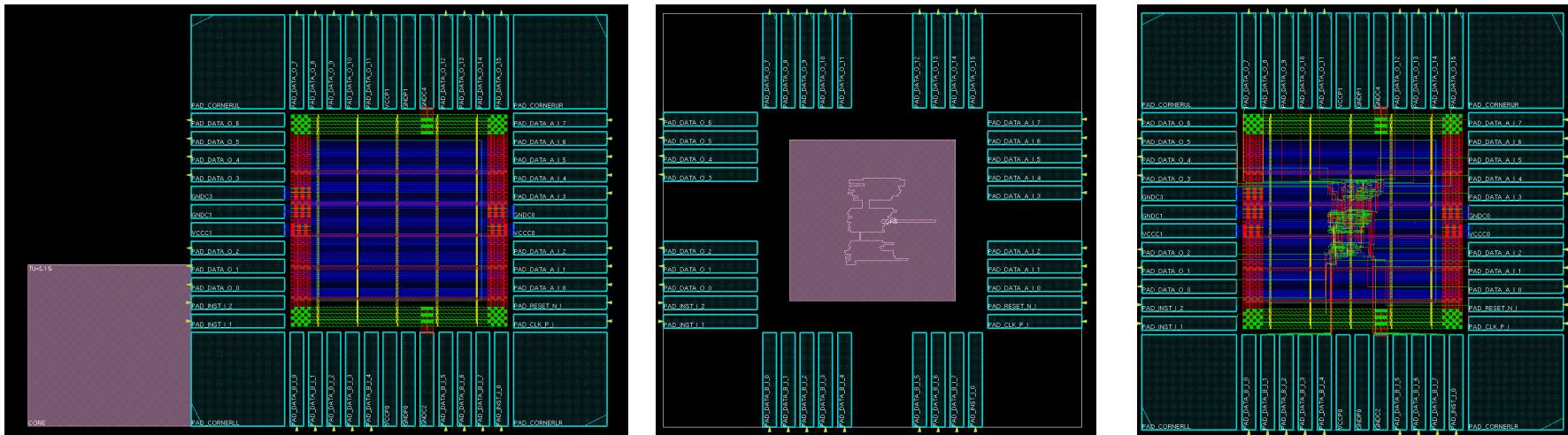
# Tool Widgets

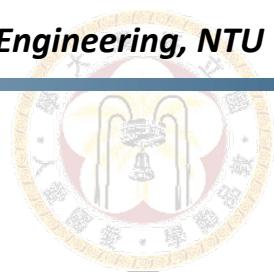




# Design Views

- **Floorplan View**
  - Display the hierarchical module and block guides, connection flight lines and floorplan objects
- **Amoeba View**
  - Display the outline of modules after placement
- **Physical View**
  - Display the detailed placements of cells, blocks





# Display Control

All Colors	V	S
<input type="checkbox"/> Instance	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Instance	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Block	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Std. Cell	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Cover Cell	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Physical Cell	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
IO Cell	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Area IO Cell	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Black Box	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
<input type="checkbox"/> Module		
Module	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Guide	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Fence	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Region	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Partition	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
<input type="checkbox"/> Net		
Signal	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Special Net	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Power	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Ground	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Shield	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Metal Fill	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Clock	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
<input type="checkbox"/> Cell		
Pin Shapes	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Cell Blockage	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Cell Layout	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
<input type="checkbox"/> Blockage		
Obstruct	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Area Density	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Macro Blkg	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Routing Blkg	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Fill Blkg	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Block Halo	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Routing Halo	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Blockage Link	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>

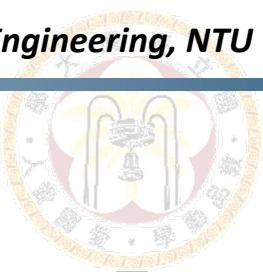
<input type="checkbox"/> Row	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Standard Row	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
IO Row	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Row Pattern	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Macro Pattern	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
<input type="checkbox"/> Floorplan		
Rel. FPlan	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
SDP Group	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
SDP Connect	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
SizeBlkg	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
S. Resize Line	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
E. Resize Line	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
MP CongTag	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
IO Cluster	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Overlap Macro	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Overlap Guide	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Overlap Block	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Datapath	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
<input type="checkbox"/> Partition		
Pin Guide	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Ptn Pin Blk	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Ptn Feedthru	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
<input type="checkbox"/> Bump		
Bump(Normal)	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Bump(Back)	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Bump Connect	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
<input type="checkbox"/> Power		
Power Domain	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Power Graph	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Sub. Noise	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
IR Drop & EM	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>

<input type="checkbox"/> Grid	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Manufacture	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Placement	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
User-defined	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
FinFET	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
GCell	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
<input type="checkbox"/> Track		
Pref Track	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
NPref Track	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
<input type="checkbox"/> Congestion		
Cong. Label	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Congestion	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
GC Overflow	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Channel Cong.	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
H. Congest	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
V. Congest	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
<input type="checkbox"/> Multiple Color		
Density Map	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Pin Density	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Clock Tree	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Thermal	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
MP Checker	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
FL Congest	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
GTD Object	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Double Pattern	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
<input type="checkbox"/> Miscellaneous		
Terminal	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Violation	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Bus Guide	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Aggressor	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Select	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Text	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Pin Text	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Channel	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Flight Line	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
REDUCED	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Port Number	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Grid Resistor	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>

<input type="checkbox"/> Wire&Via	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Metal 0	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Via 01	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Metal 1	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Via 12	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Metal 2	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Via 23	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Metal 3	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Via 34	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Metal 4	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Via 45	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Metal 5	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Via 56	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Metal 6	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Via 67	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Metal 7	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Via 78	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Metal 8	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Via 89	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Metal 9	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Via 910	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Metal 10	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Via 1011	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Metal 11	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Via 1112	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Metal 12	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Via 1213	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Metal 13	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Via 1314	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Metal 14	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Via 1415	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Metal 15	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>

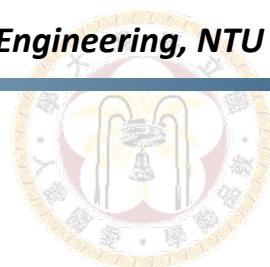


# Commonly-Used Binding keys

Key	Action
q	Edit attribute
f	Fits display
z	Zoom in
Z	Zoom out
Arrows	pans design area in the direction of the arrow
Escape	Cancel
K	Removes all rulers

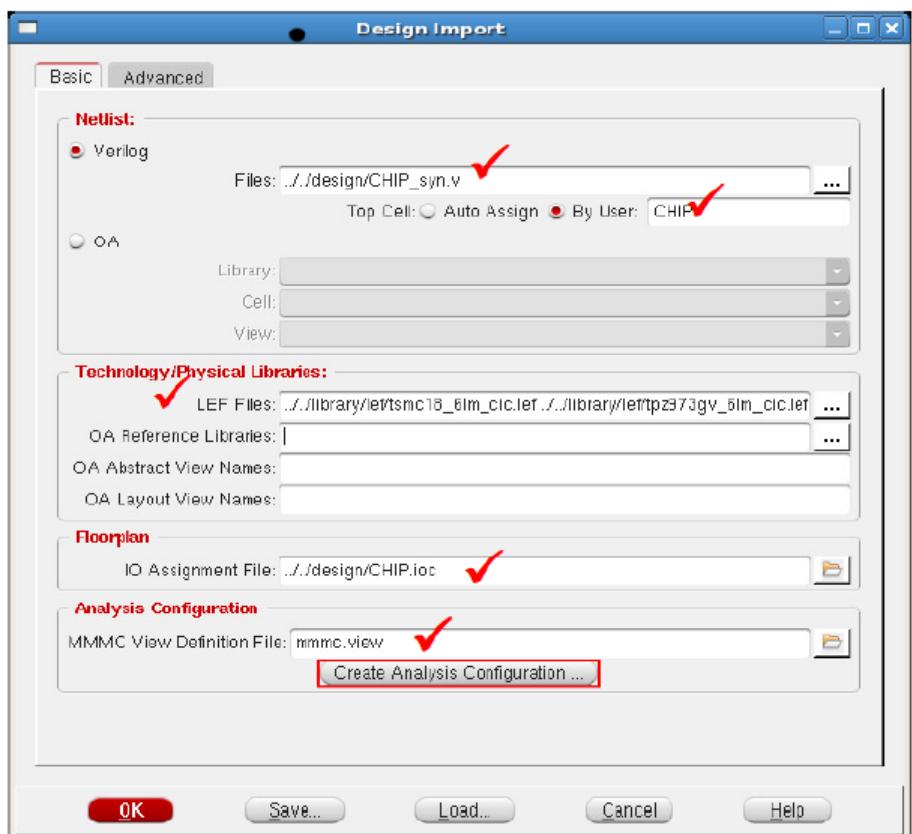
Key	Action
space	Select Next
e	popup Edit
T	editTrim
0-9	toggle layer[0-9] visibility
h/H	hierarchy up/down
x	clear Drc
N	next via

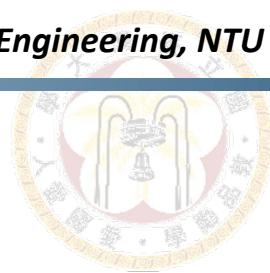
Looking for more bindkey:  
*Options → Set Preference, Binding Key*



# Import Design

- ***File -> Design Import***
- **Import LEF in the order:**
  - Technology first
  - Geometry lef for cell/block
  - Antenna lef for cell/block
- **IO Assignment File**
- **MMMC View Definition File**

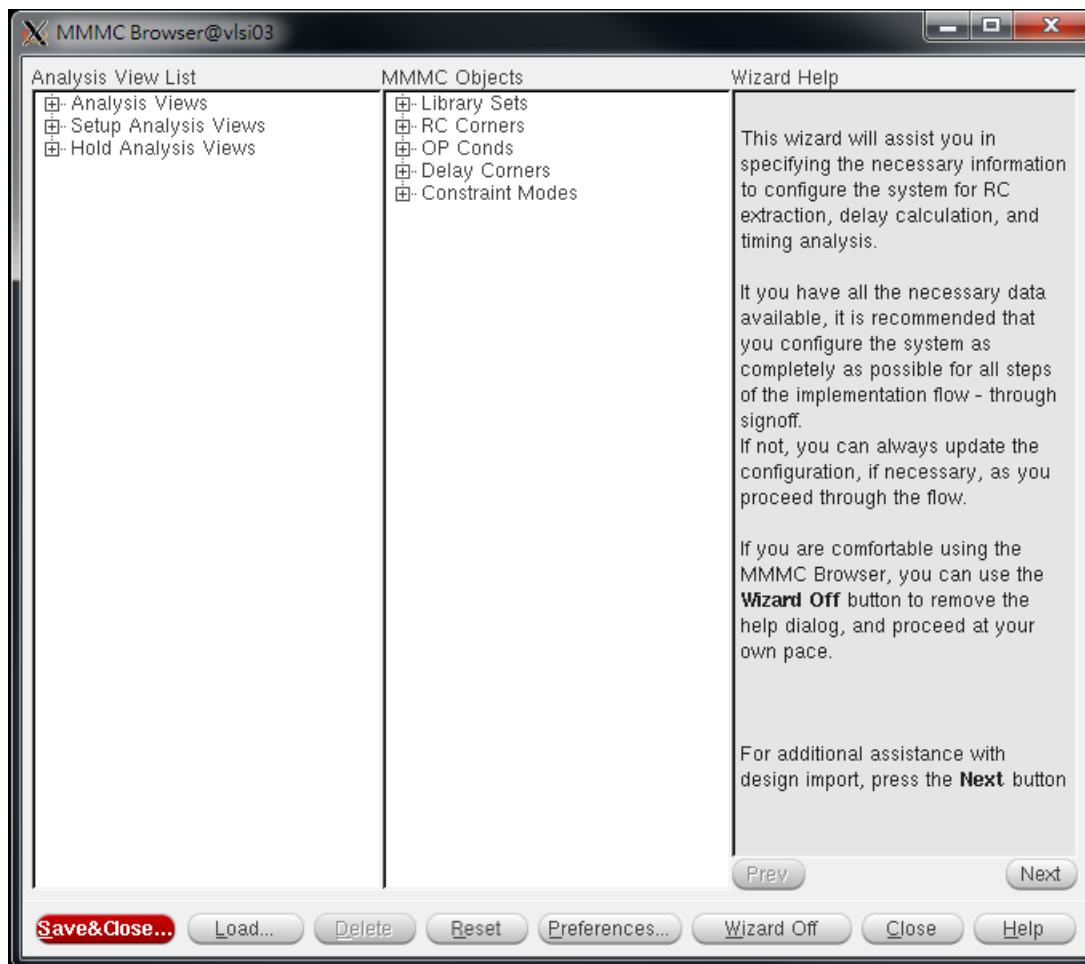


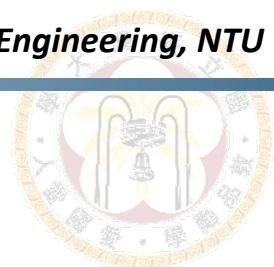


# MMMC Browser

## ■ MMMC: Multi-Mode Multi Corner

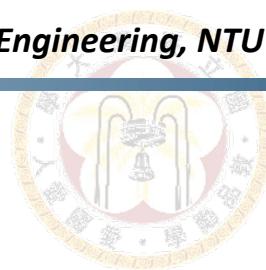
Create Analysis Configuration ...





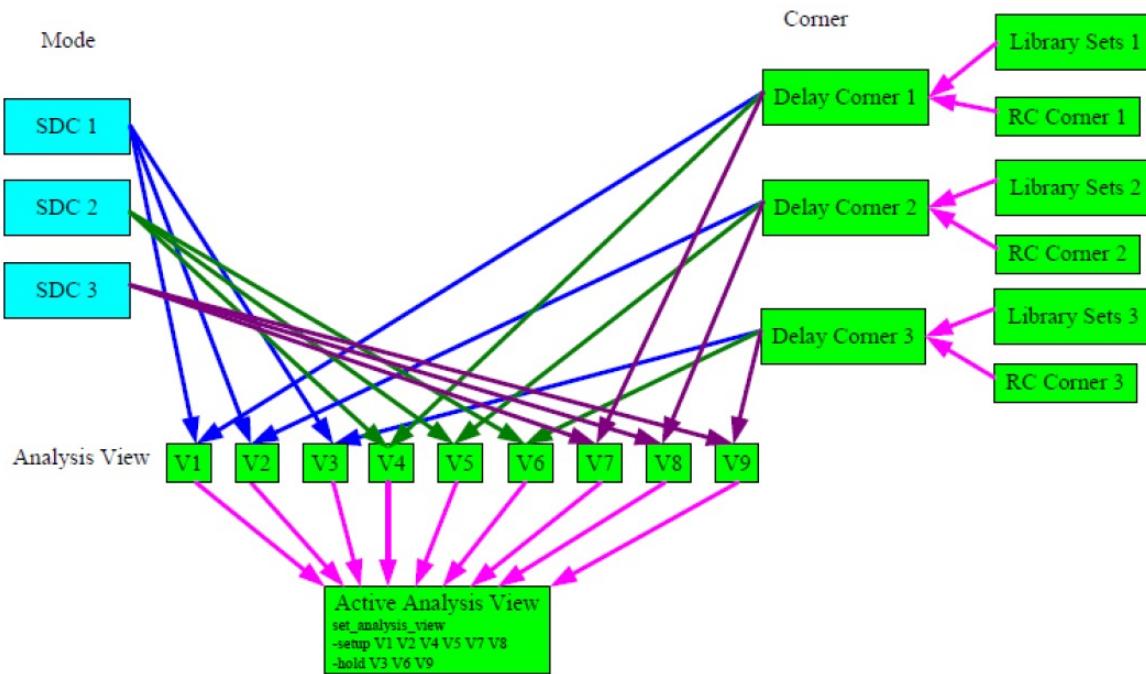
# Traditional Timing Analysis

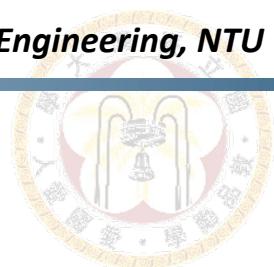
- **One .sdc file**
  - Fit all operation mode in one .sdc file
- **Max Timing Libraries**
  - Worst-case conditions for setup-time analysis
- **Min Timing Libraries**
  - Best-case conditions for hold-time analysis



# Why MMMC

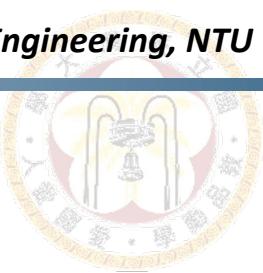
- Example: Design is required to meet 3 operating corners
  - Corner1: 0.81V, 125° C
  - Corner2: 0.9V, 25° C
  - Corner3: 0.99V, -40° C



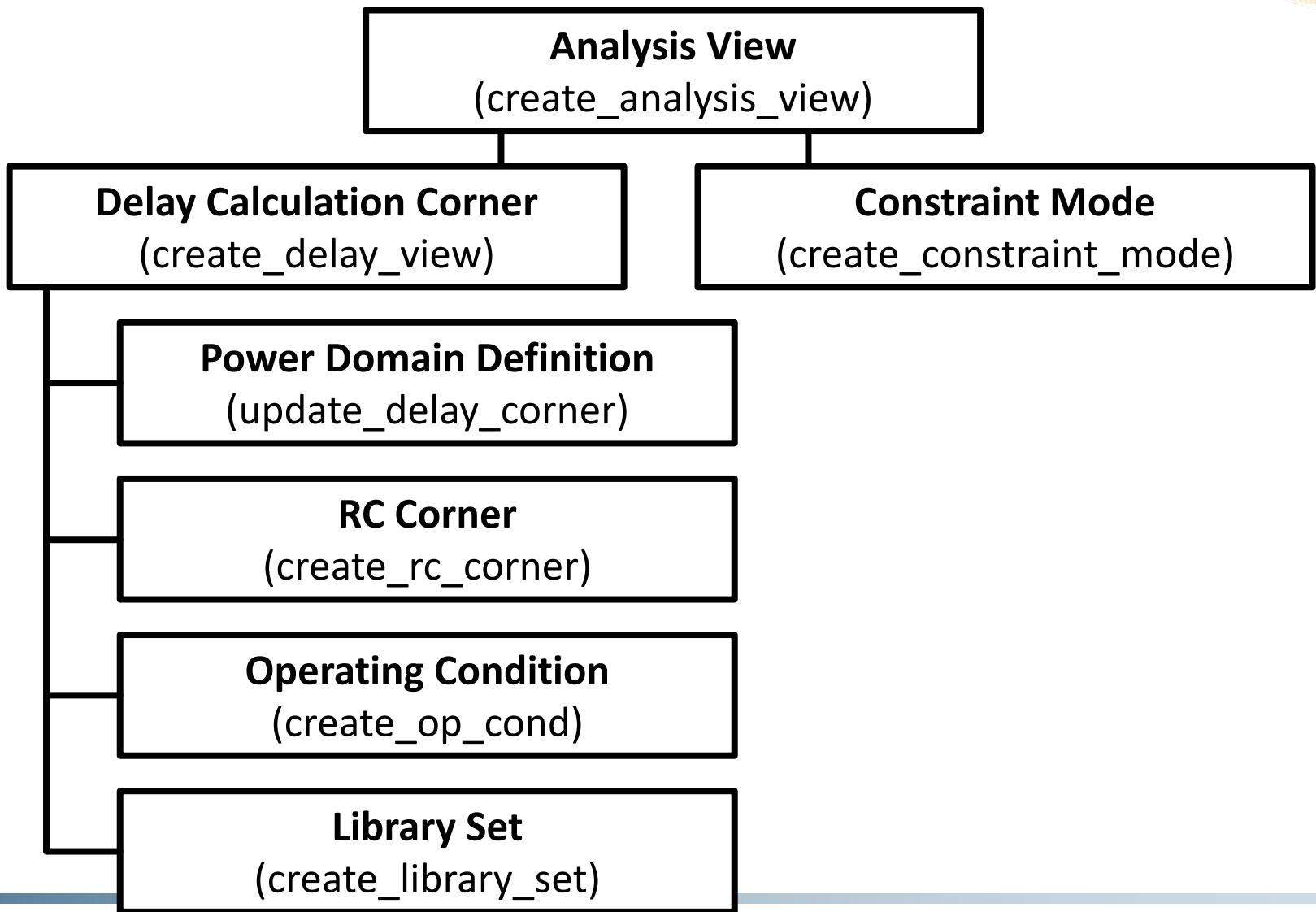


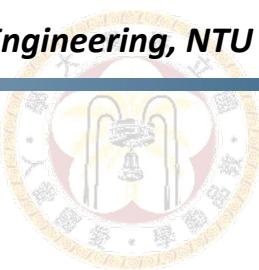
# MMMC Configuration

- Load timing information and .lib/.cdb file for signal integrity (SI) analysis (library setting)
- RC Corners for extracting capacitive parameters
- Operating conditions
- Delay corners
- Add constraint mode and read .sdc file
- Create MMMC analysis views, assign which views are used for setup / hold time analysis and optimization



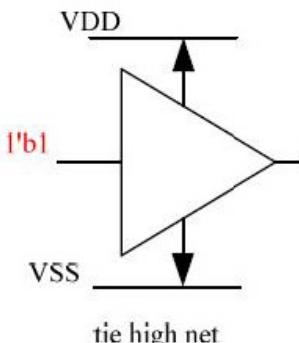
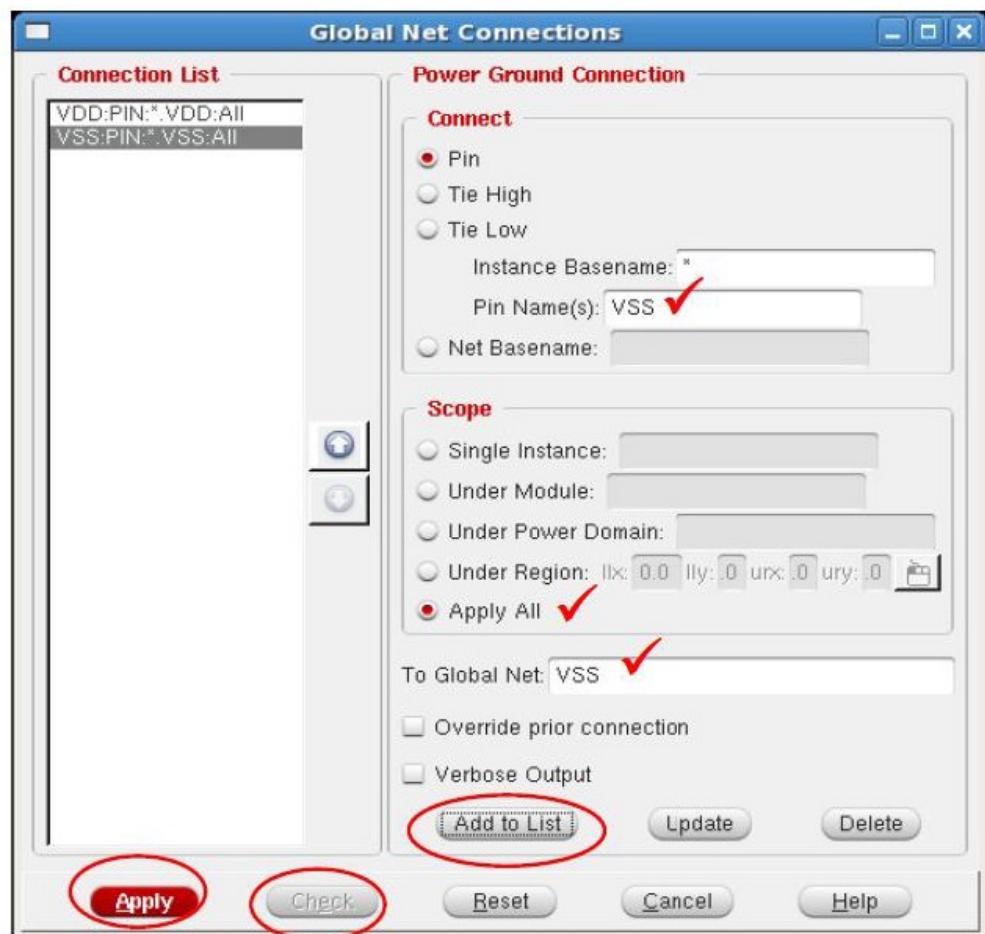
# MMMC Structure



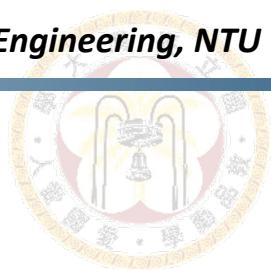


# Global Net Connection

## ■ Power -> Connections Global Nets



INV inv1(.I(1'b1), .O(o));



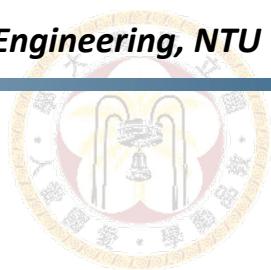
# Set Process Node

*setDesignMode -process 45*

- Process node affect the threshold values to the RC extraction filters

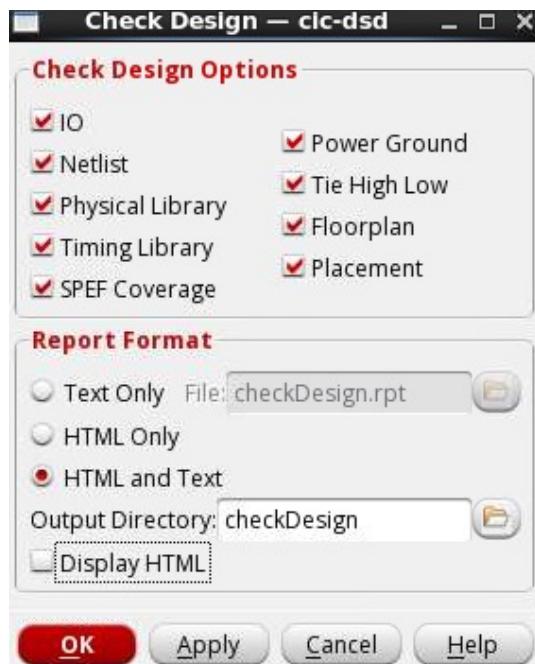
default →

Process Node	Extraction Filters		
	coupling_c_th	relative_c_th	total_c_th
Above 130nm	3.0000	0.03	5.0000
130nm and below	0.4000	1	0.0000
90nm and below	0.2000	1	0.0000
65nm and below	0.1000	1	0.0000
45nm and below	0.1000	1	0.0000



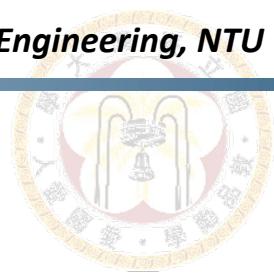
# Check Design

- ***File → Check Design...***
  - Checks for missing or inconsistent library and design data.



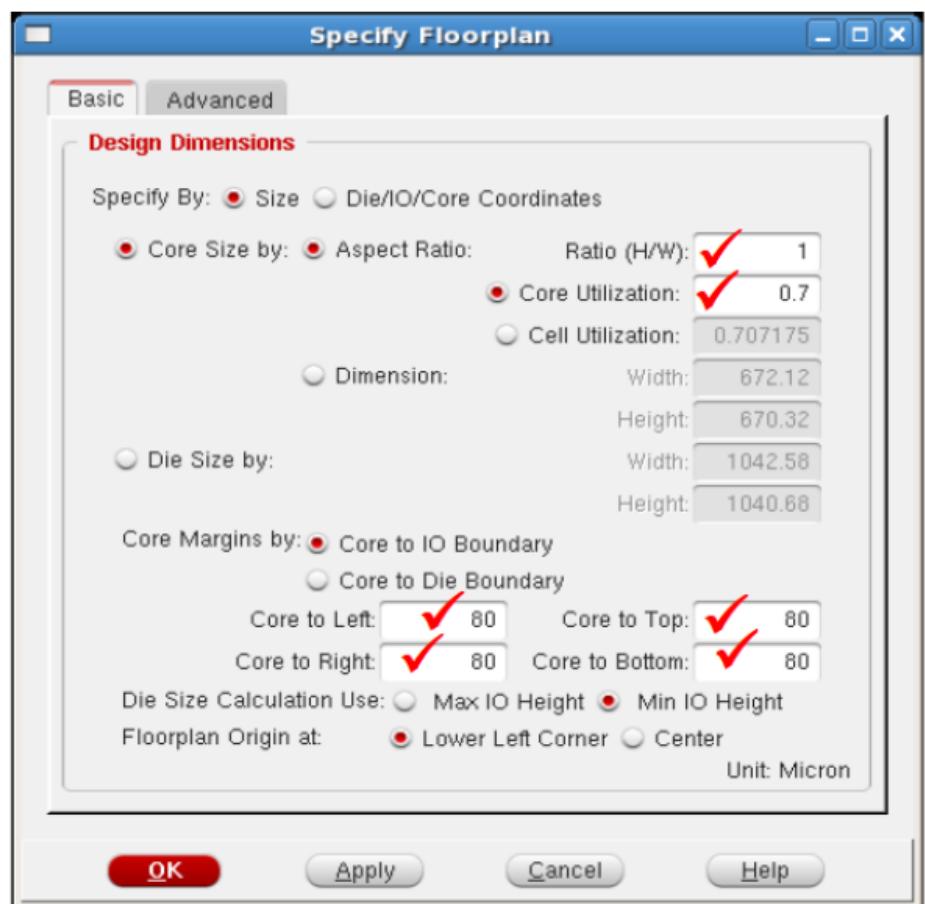
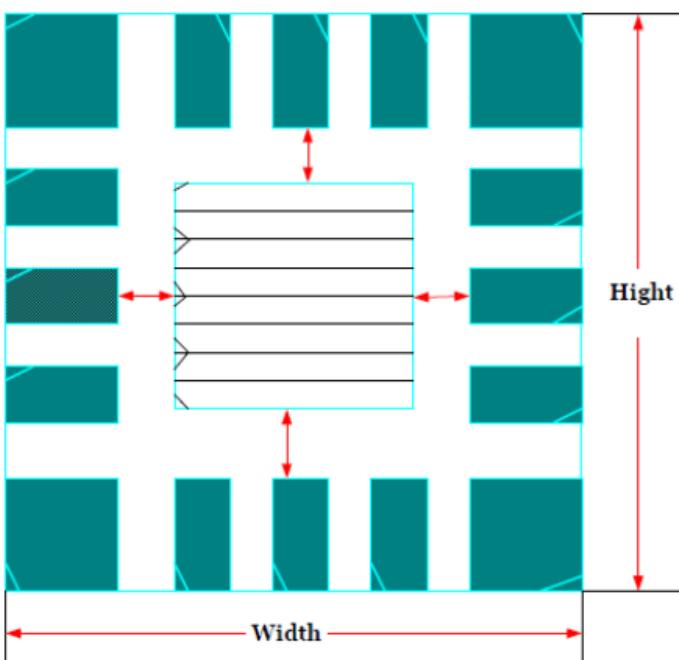
check items:

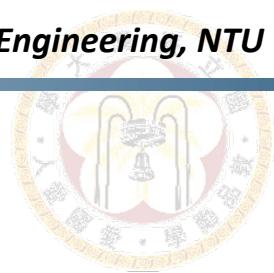
- missing lef
- missing timing data
- pin without shape
- port connect to core
- multiple driver
- no driver
- floating power ground terms
- unplaced IO pad
- .....



# Specify Floorplan

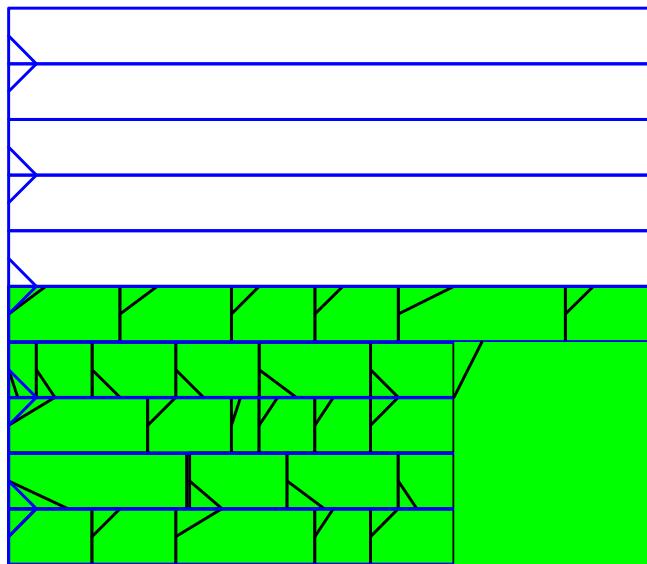
- *Floorplan -> Specify Floorplan*
  - Aspect ratio
  - Utilization (init. usually 0.7)

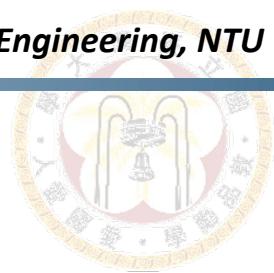




# Initial Floorplan-core utilization

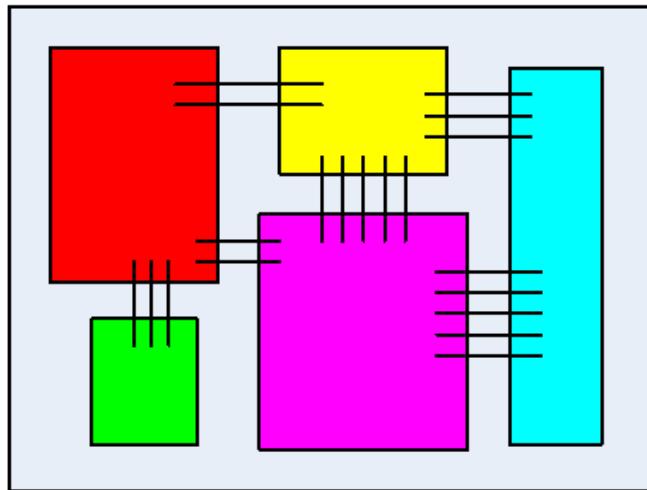
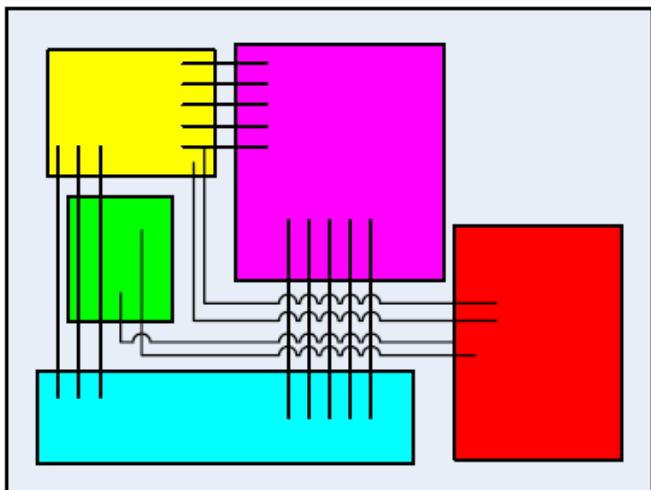
$$\text{core utilization} = \frac{\text{standard cell} + \text{macro cell}}{\text{core area}}$$

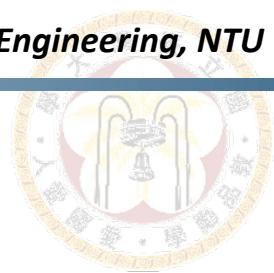




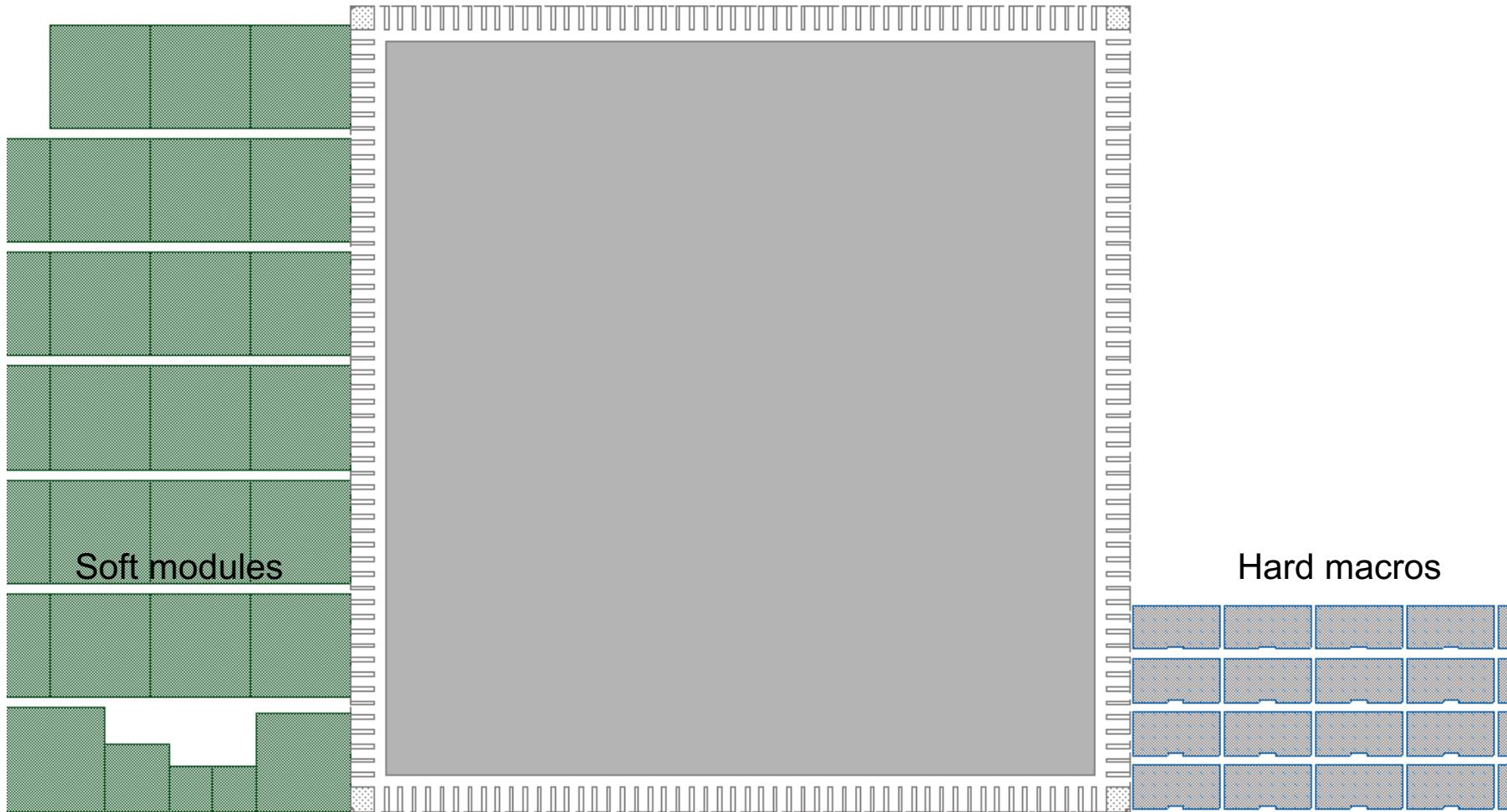
# Goal of Floorplan

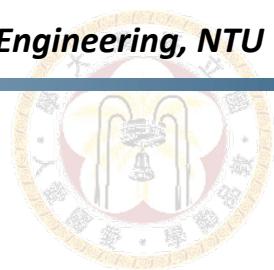
- Early physical layout to ensure design objective can be achieved
  - Minimum area for low cost
  - Minimum congestion for design routable
  - Estimate parasitic for delay calculation
  - Analysis power for reliability
- Difference floorplan, difference performance





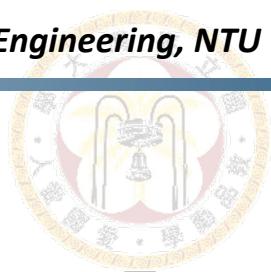
# Soft Module & Hard Macro





# Floor Planning with Hard Macro

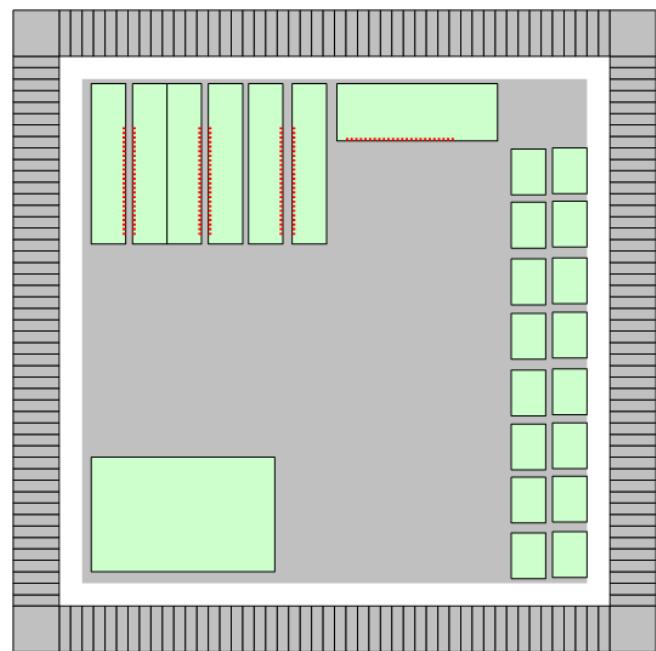
- **Macro Floorplanning**
  - Move macro blocks to proper position
  - Place macro around the corner to improve routability
- **If there are many hard macro, try to use automatic floorplan**
  - *Floorplan -> Automatic Floorplan -> Plan Design*
- **Edit floorplan by functions**
  - *Floorplan -> Edit Floorplan*
- **Block place issue**
  - Power issue
  - Noise issue
  - Route issue

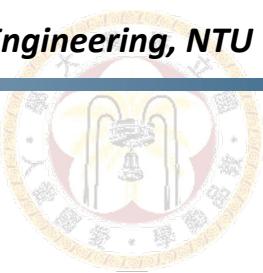


# Macro Placement

## ■ Tip for macro placement

- Place macros around chip periphery
- Consider connections to fixed cells when placing macros
- Orient macros to minimize distance between pins
- Reserve space for power grid and signal routing and possible buffer insertion
- Keep out standard cells with block halo
- Keep random areas continuous to avoid detaches areas
- Keep edges of macros aligned if possible





# Place Macro Block

- ◆ Automatic generate a quick, initial floorplan

**Floorplan → Generate Floorplan → Place Macros**

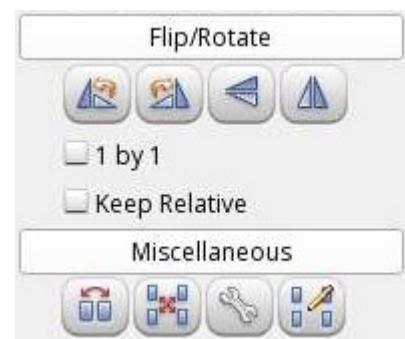
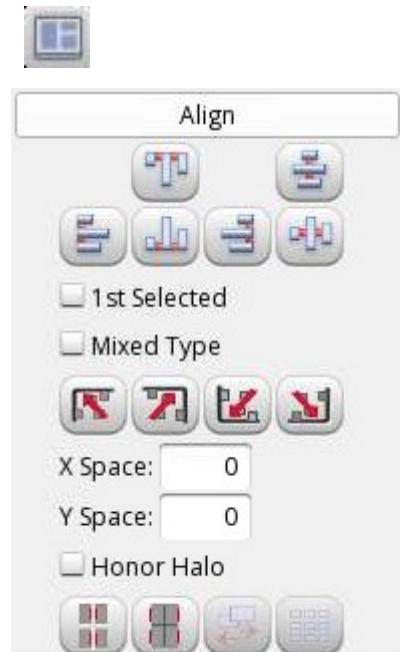
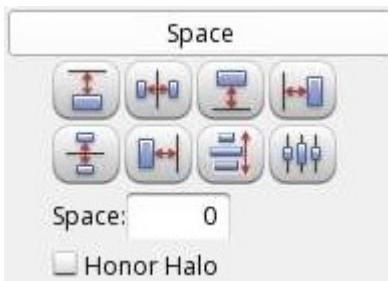
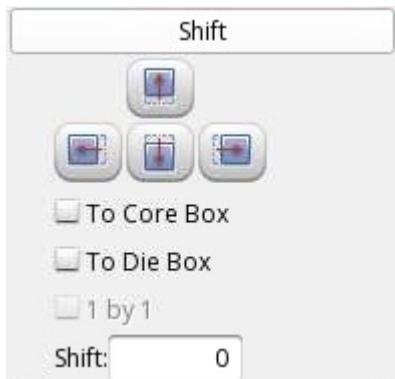
- ◆ Move/Resize/Reshape floorplan object.

- ◆ Fix block placement status

**Floorplan → Edit Floorplan → Set Instance Placement Status**

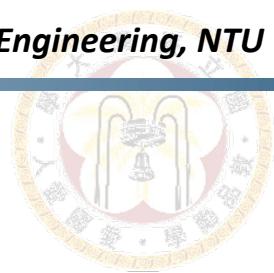
- ◆ Use floorplan toolbox:

**Floorplan → Floorplan Toolbox...**



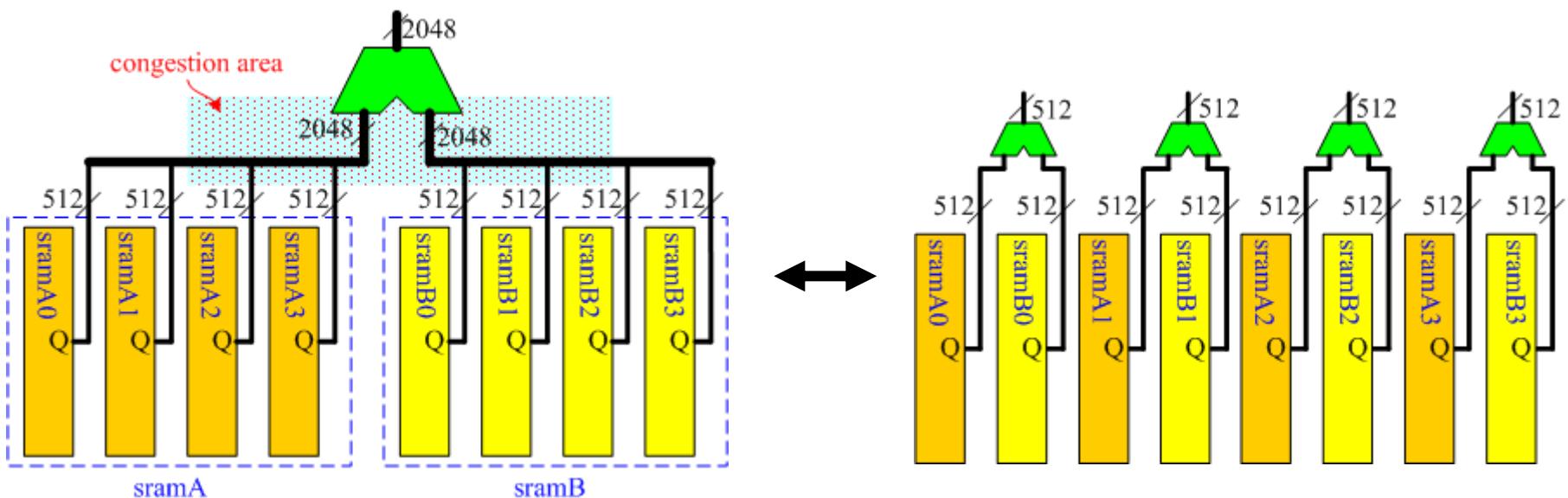
set placement status

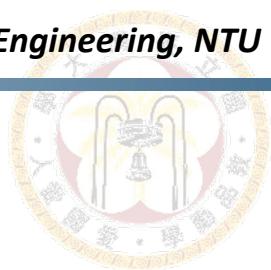




# Tip for Joint Memory

- Wide data width joint with multi SRAM instance



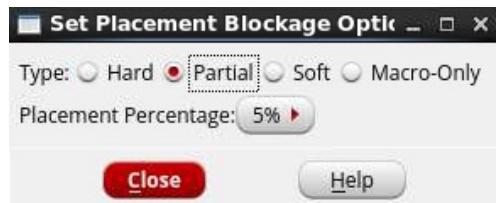


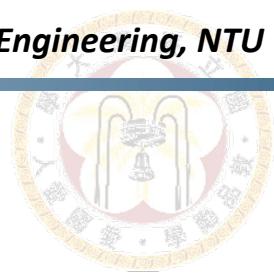
# Placement Blockage



**Floorplan → Edit Floorplan → Create Placement Blockage**

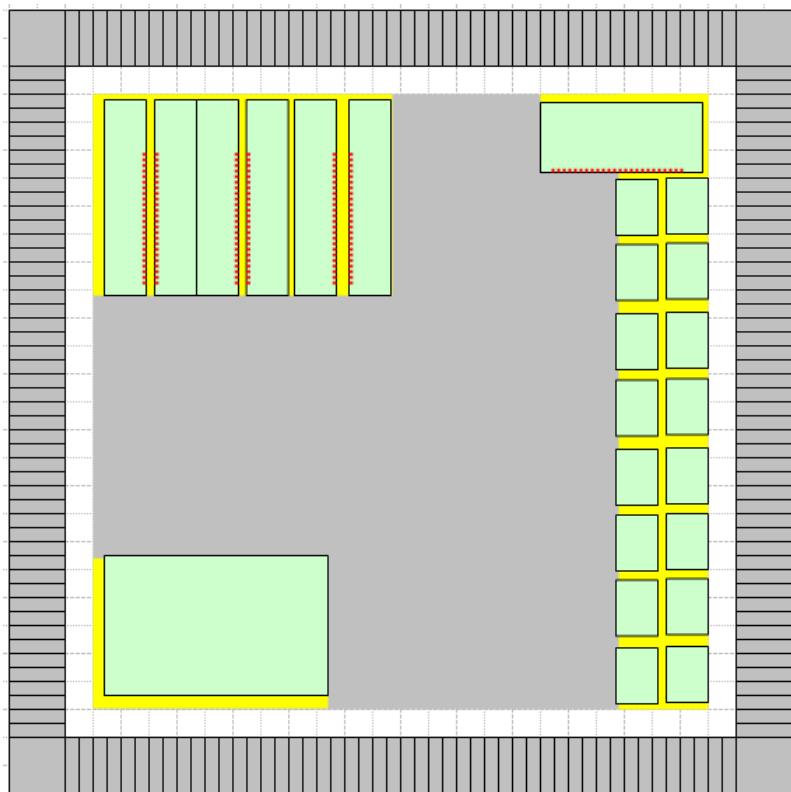
- Hard
  - Prevents cells be placed in this area.
- Partial
  - Sets a percentage of the area that is available for placement.
- Soft
  - The initial placement should not use the area, but later phases, such as optimization or CTS can use the blockage area.
- Macro-Only
  - Enables plan\_design to keep macros out of the placement blockage

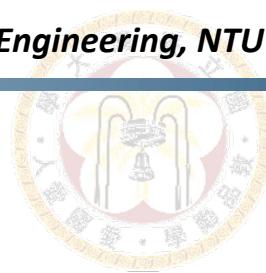




# Soft/Partial Placement Blockage

- Create soft blockage in long thin channel between macros.
- Create partial blockage in long channel if logic cells need to be placed in the channel.





# Routing Blockage

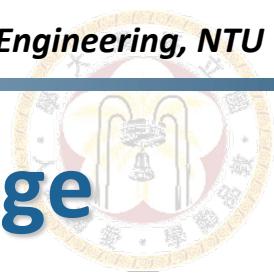
## ■ Routing Blockage

***Floorplan → Edit Floorplan → Create Routing Blockage***

- Blockage on given routing layers

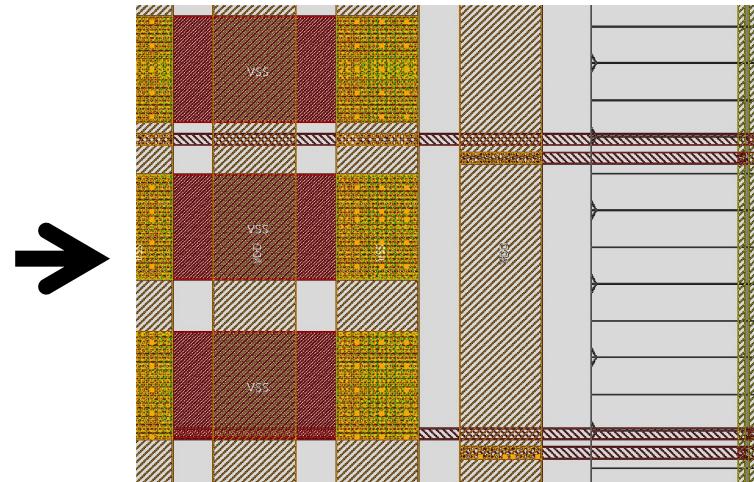
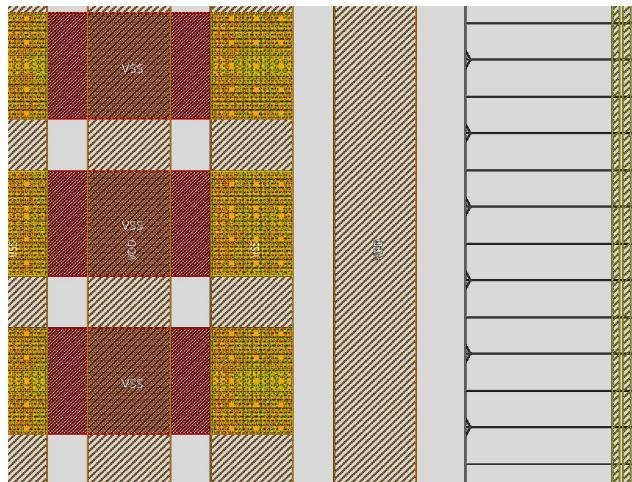
*F3*



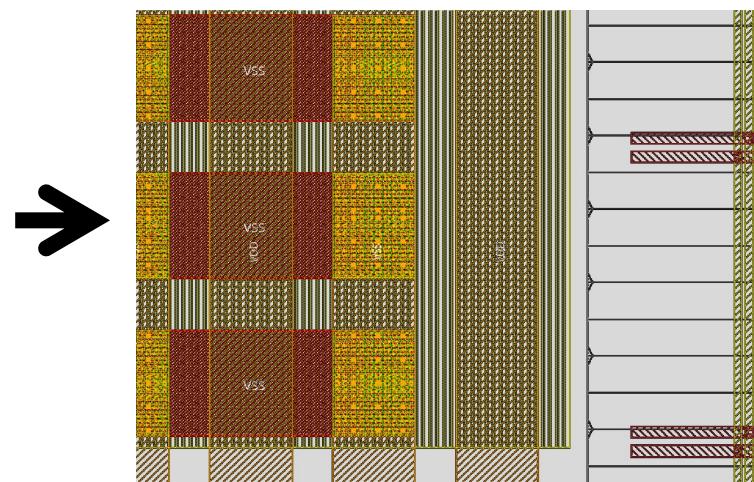
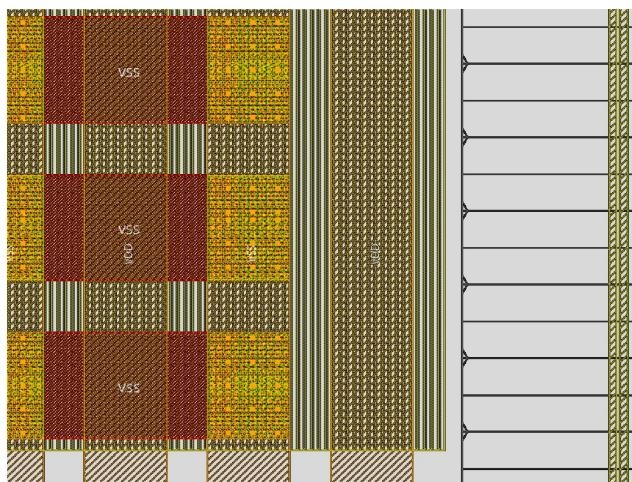


# Keep out Stripe with Routing Blockage

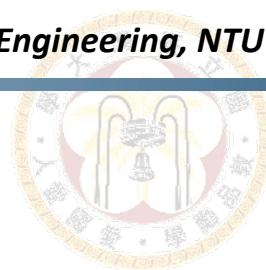
Without  
Blockage



With  
Blockage

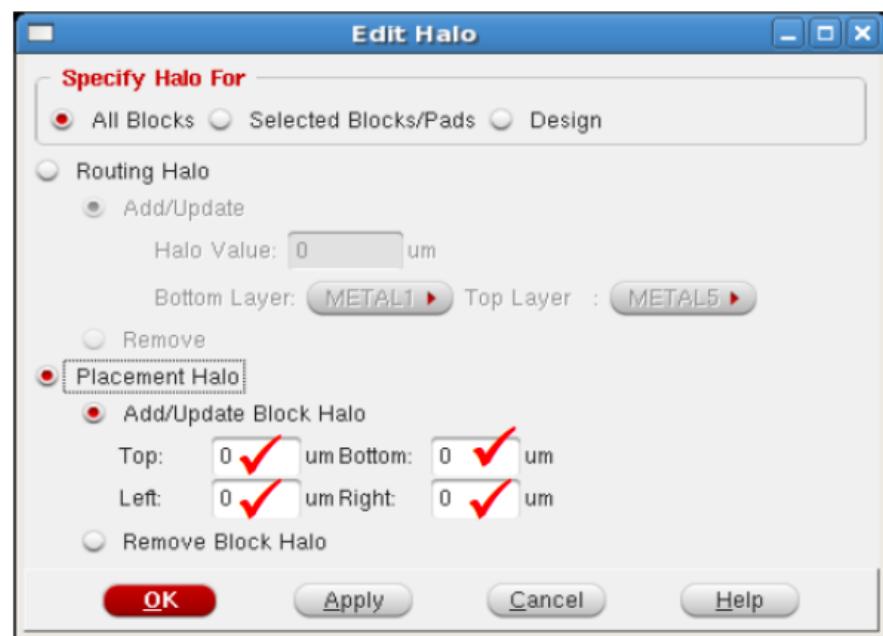
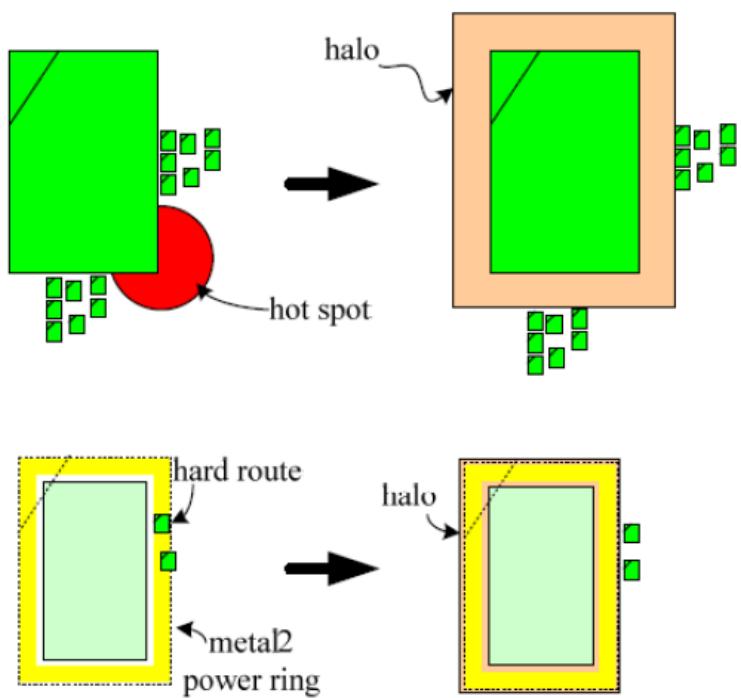


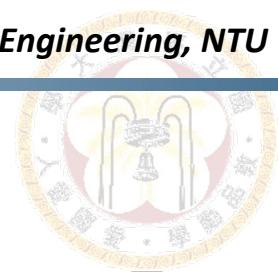
These routing blockages should be removed after powerplan completed



# Add Halo to Block

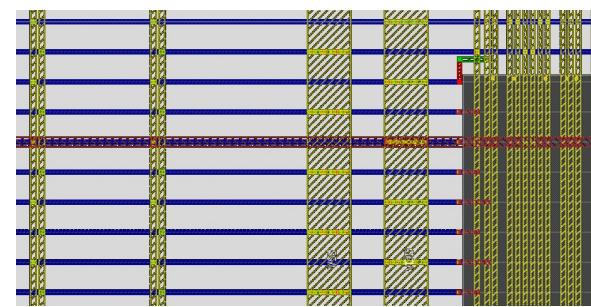
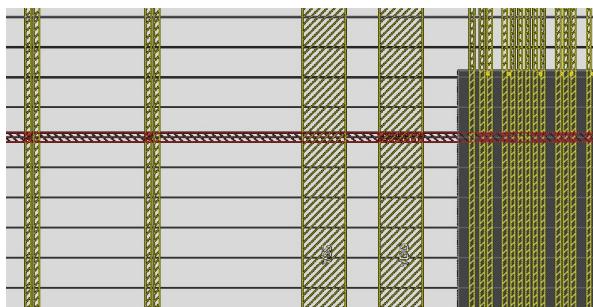
- **Floorplan -> Edit Floorplan -> Edit Halos**
  - Prevent the placement of blocks and standard cells in order to reduce congestion around a block



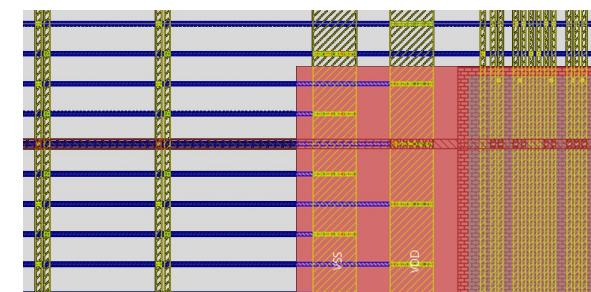
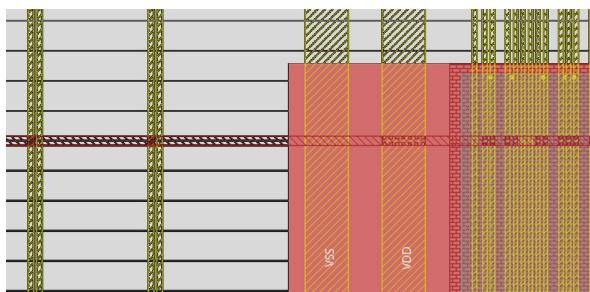


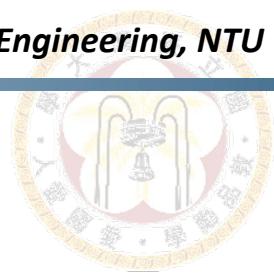
# Placement halo affect followpin

Without  
Halo



With  
Halo





# Module Constraint

- None
- Soft Guide
- Guide
- Region
- Fence

