



Computer-Aided VLSI System Design (EEE5022)

台大電機系/電子所

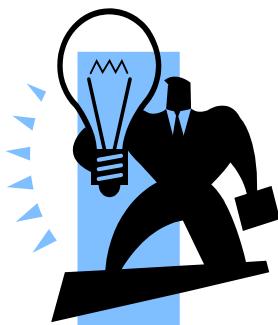
楊家驥教授

2023.9.5

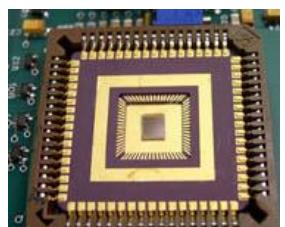
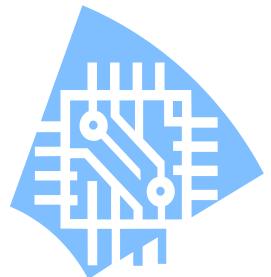


IC Design and Implementation

Idea



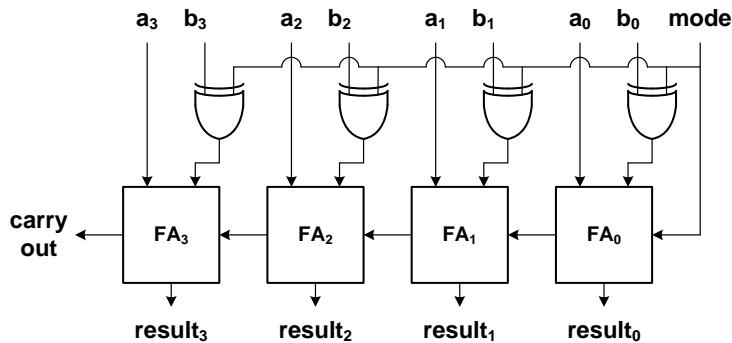
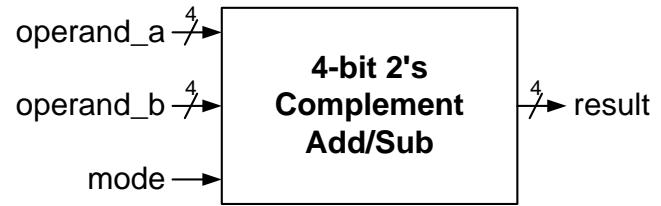
Design





Digital IC Design Flow

1. Concept/Application
2. Function/Spec. definition
3. Algorithm exploration
4. Architecture design
 - ❖ Divide-and-conquer
 - ❖ Sub-module design
 - ❖ Design verification
5. System prototyping
 - ❖ RTL design
 - ❖ Verilog Coding
 - ❖ Cell-based IC design flow



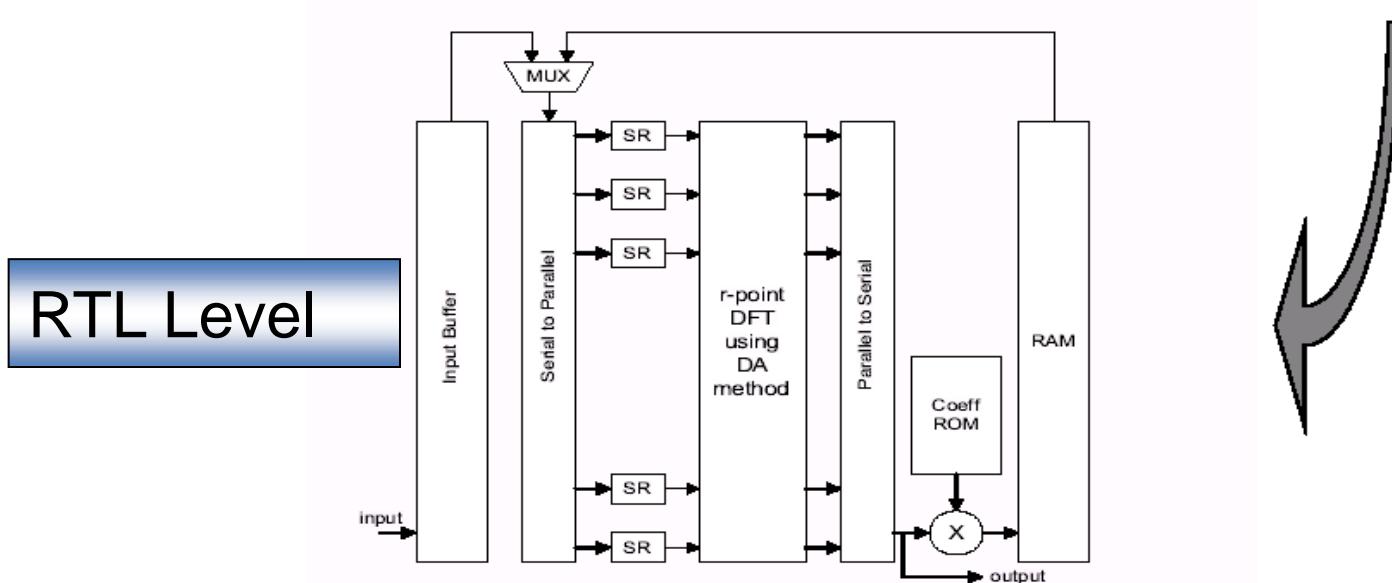
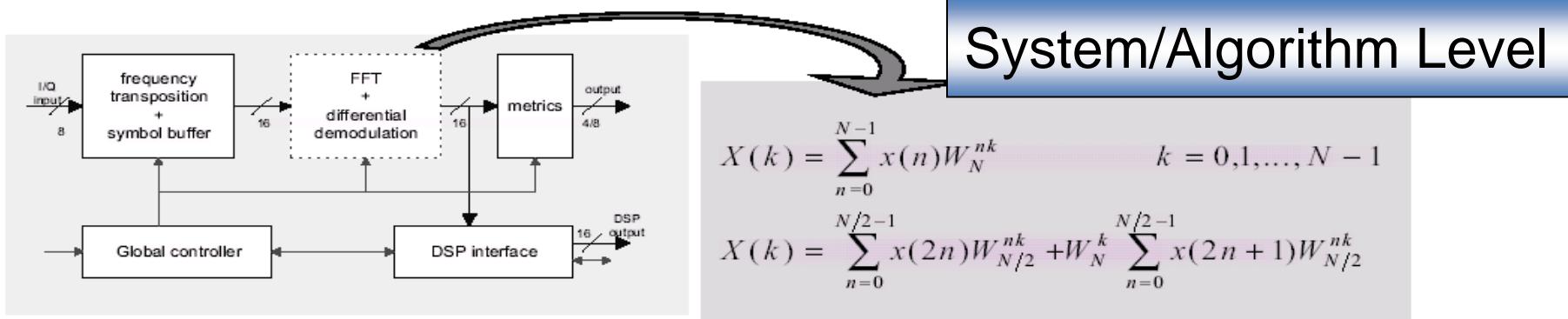
```
module Add_Sub_Unit( result, operand_a, operand_b, mode, detect );
  input [3:0] operand_a, operand_b;
  input mode;
  output [3:0] result;
  output detect; // for question 3
  wire [3:0] xor_b;

  xor g0 ( xor_b[0], operand_b[0], mode );

```

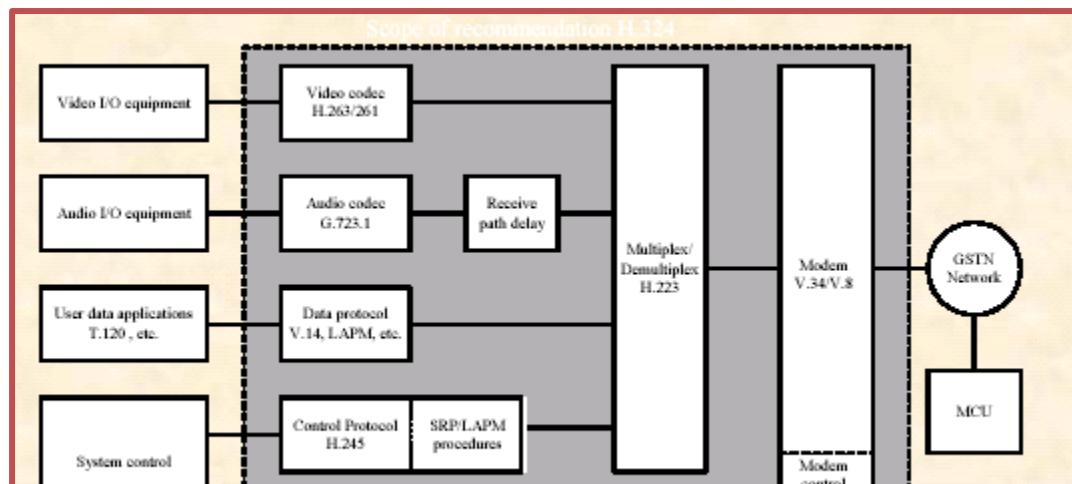


Algorithm Mapping





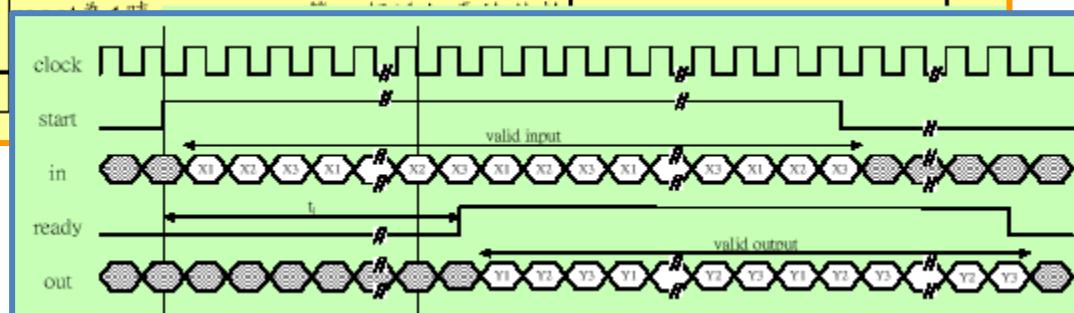
System Specifications



Partition

腳位名稱		描述	Drive Strength/Output Load
clk	輸入	系統時脈	assume infinite
reset	輸入	系統重置訊號，high active	1 ns/pf
din	輸入	每個clock cycle輸入一個16-bit 正整數	1 ns/pf
ready	輸出		
dout	輸出		

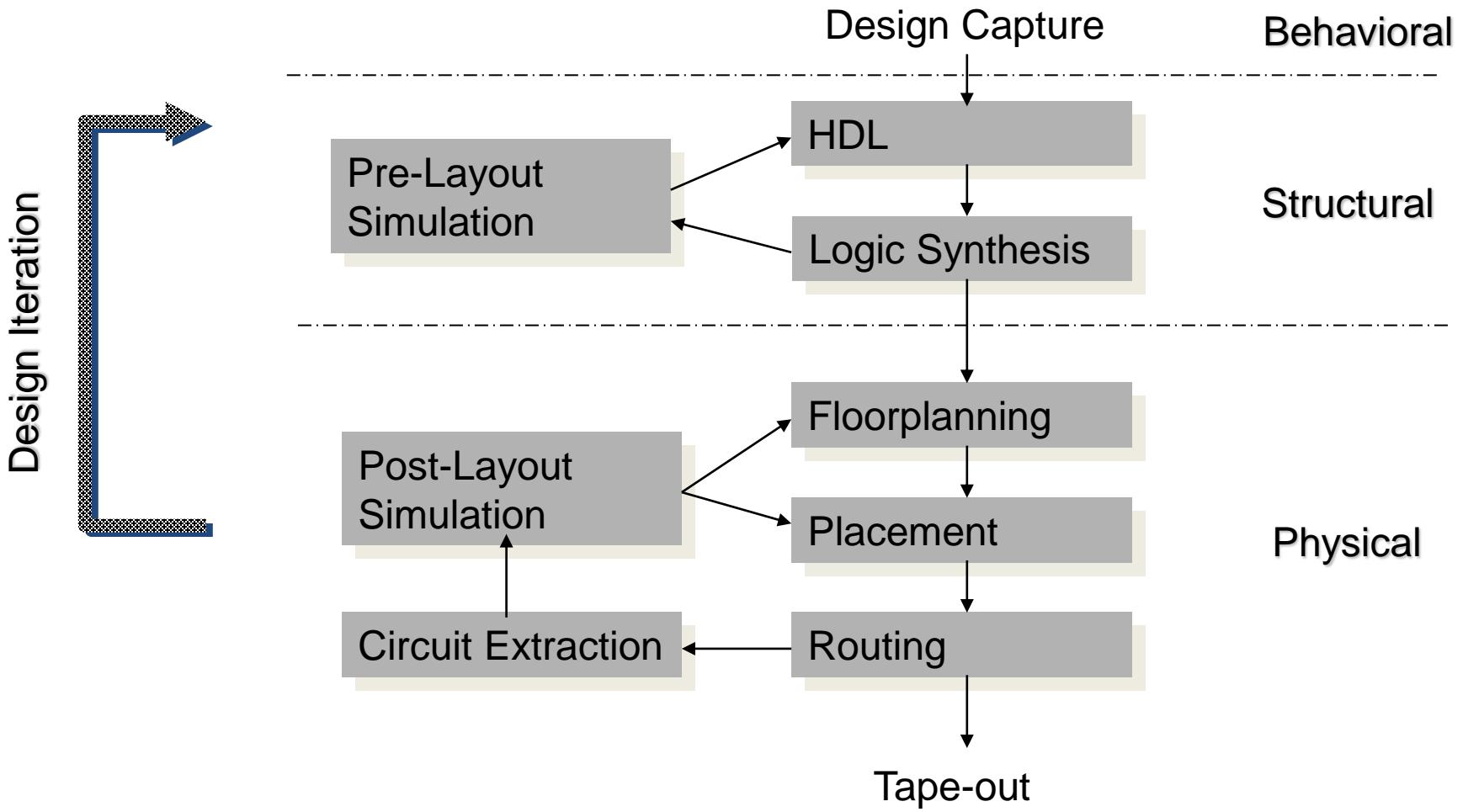
IO Spec.



IO Timing Spec.

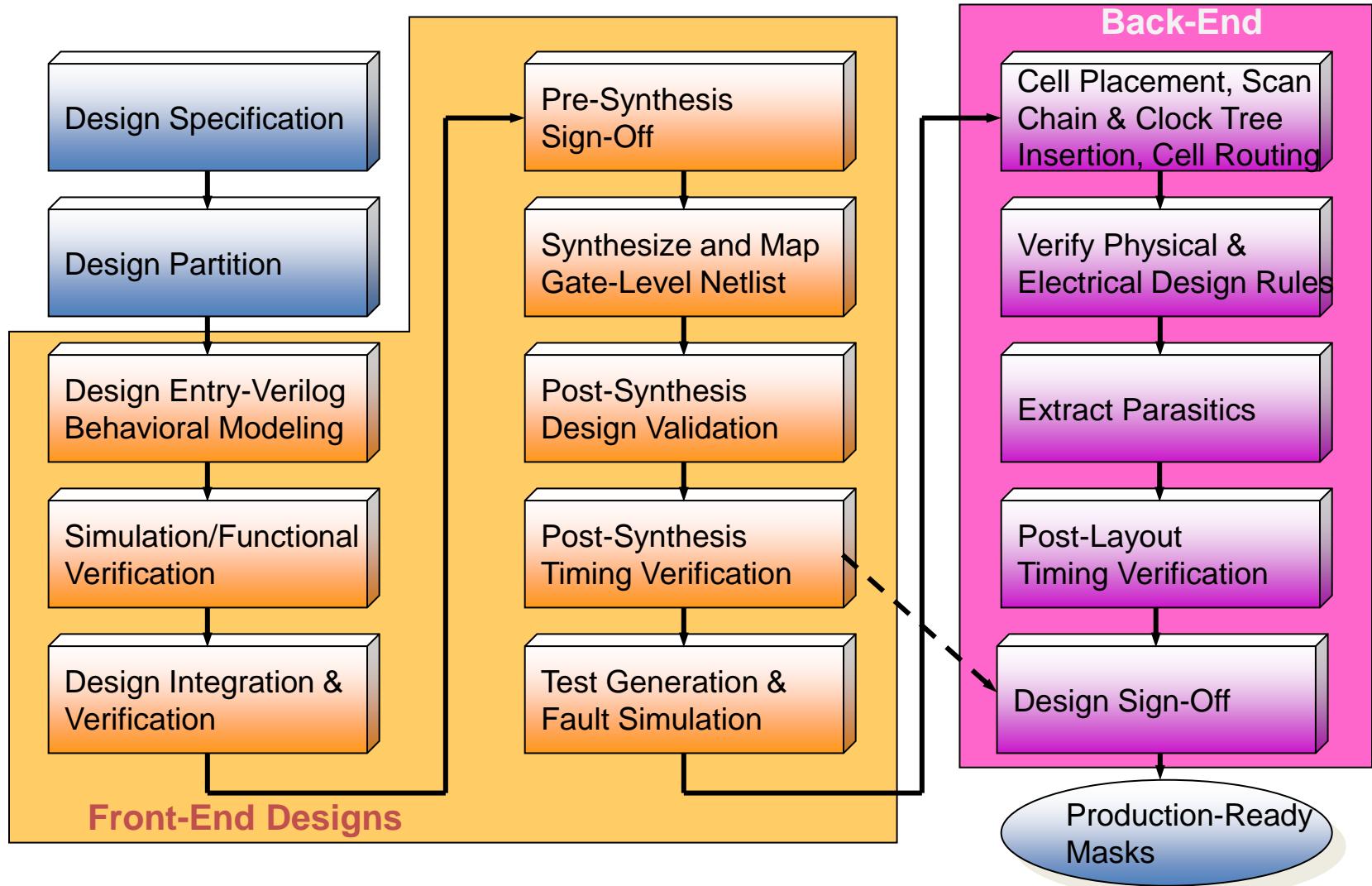


Cell-based Design Flow





Digital IC Design Flow





Introduction

❖ Objective

❖ Students will learn how to design VLSI circuits and systems following a **standard VLSI system design flow**, where various **electronic design automation (EDA) tools** will be used extensively in the semester

❖ Course content

1. Verilog-HDL
2. Synthesis
3. Static Timing Analysis
4. Placement and Routing
5. Verification
6. High-level synthesis
7. Design Rule Check, Layout versus Schematic, Layout Parasitic Extraction



Course Schedule (1)

Week	Date	Lecture	Speaker	Place	Lab	HW assign	HW due
01	09/05	Introduction	楊家驥教授	MD205	Lab0		
02	09/12	Verilog-HDL (1)	張惇宥	Online			
03	09/19	Verilog-HDL (2)	張惇宥	Online	Lab1	HW1	
04	09/26	Verilog-HDL (3)	李晴妍	Online			
05	10/03	Verilog-HDL (4)	李晴妍	Online	Lab2	HW2	HW1
06	10/10	Synthesis (1)	陳世豪	Video	Lab3	HW3	
07	10/17	Synthesis (2)	陳世豪	Online			HW2
08	10/24	Static Timing Analysis	張峻璋	Online	Lab4		
09	10/31	Midterm		MD205			
10	11/07	Midterm Review/ Project Announcement	TA	MD205		HW4	HW3



Course Schedule (2)

Week	Date	Lecture	Speaker	Place	Lab	HW assign	HW due
11	11/14	APR (1)	羅宇呈	Online	Lab5		
12	11/21	APR (2)	羅宇呈	Online	Lab6	HW5	HW4
13	11/28	APR (3)	羅宇呈	Online	Lab7		
14	12/05	Cadence Formal Verification	Cadence	Online	Lab8		HW5
15	12/12	High-Level Synthesis	Cadence	Online	Lab9		
16	12/19	PVS/DRC/LVS	Cadence	Online	Lab10		
17	12/26	Project Presentation	MediaTek	Online			

Acknowledgment:

- Final project: 聯發科技，無線通訊技術本部，晶片開發一處
- Formal verification, HLS, PVS: 益華科技

MEDIATEK

cadence®



NARLabs 國家實驗研究院
台灣半導體研究中心
Taiwan Semiconductor Research Institute



線上課程連結

- ❖ Webex: <https://ntucc.webex.com/meet/yicwu>
- ❖ 登入請用”學號-姓名”供助教確認身份
- ❖ 預設為關閉麥克風，有問題可使用聊天室提出



Contact (1)

- ❖ 大助教: 駱奕霖 f06943176@ntu.edu.tw
- ❖ 小助教: 羅宇呈 f08943129@ntu.edu.tw 、朱怡蓁 r10943012@ntu.edu.tw 、
吳秉陞 r10943007@ntu.edu.tw
- ❖ 授課助教:
 - ❖ Verilog-HDL (1) (2): 張惇宥 r11943017@ntu.edu.tw
 - ❖ Verilog-HDL (3) (4): 李晴妍 r10k41001@ntu.edu.tw
 - ❖ Synthesis (1) (2): 陳世豪 r09943176@ntu.edu.tw
 - ❖ Static Timing Analysis: 張峻瑋 r09943187@ntu.edu.tw
- ❖ Lab助教:
 - ❖ Lab0-Lab10: 朱怡蓁 r10943012@ntu.edu.tw



Contact (2)

❖ HW助教：

- ❖ HW1: 李其祐 r11943123@ntu.edu.tw
- ❖ HW2: 周子皓 r11943133@ntu.edu.tw
- ❖ HW3: 張力元 r11943006@ntu.edu.tw
- ❖ HW4: 陳泰融 r11943024@ntu.edu.tw
- ❖ HW5: 吳秉陞 r10943007@ntu.edu.tw



Course Information

- ❖ Course materials
 - ❖ Lecture notes
 - ❖ Technical documents
- ❖ Course website
 - ❖ <https://cool.ntu.edu.tw/courses/27930>



Grading Policy

- ❖ Participation (Lab): 5%
- ❖ Homework: 30%
 - ❖ Submission to NTU COOL
 - ❖ Deadline: **Tuesday afternoon (13:59 pm)**
- ❖ Midterm Exam: 30%
 - ❖ Closed-book written test
- ❖ Final Project: 35%
 - ❖ A team of 2 students
 - ❖ VLSI design
- ❖ **No late submissions (unless for special cases)**



關於選課

- ❖ 電子所 ICS/EDA 組與重點科技學院 ICDA 組學生可直接加簽
 - ❖ 請寫信給大助教駱奕霖 f06943176@ntu.edu.tw 索取授權碼
- ❖ 如非上述學生但有 Verilog 修課經驗，可向大助教登記，待上述學生加簽完還有名額的話，將依抽簽結果提供授權碼
 - ❖ 不熟悉 Verilog 同學，可先修數位設計相關課程 (e.g., 數位電路實驗、數位系統設計、計算機結構、積體電路設計實驗等)
- ❖ 若因研究需要需修課者，請另外來信說明並 CC 指導教授
- ❖ 課程可旁聽，請寫信給大助教列入旁聽名單
- ❖ 下次開課時間：113 學年上學期



TSRI會員申請 (for 修課學生)

❖ <https://www.tsri.org.tw/main.jsp>

The screenshot shows the 'Member Registration' page for the Taiwan Semiconductor Research Institute (TSRI). The page has a blue header with the TSRI logo and the text '會員註冊'. The main form is titled 'Basic Information' (基本資料) and includes fields for:

- Username (必填前有 * 號，為必須輸入欄位): A text input field.
- Check if registered (檢查是否已註冊?): A button.
- Password (length between 8-16 characters, must contain English and numbers): A text input field.
- Confirm password (密碼確認): A text input field.
- Chinese name (同譯照): A text input field.
- English name (同譯照或格式, 姓名王大中, 名DA-CHUNG, 姓WANG): Two input fields for First Name and Last Name.
- Country: A dropdown menu showing 'Taiwan(台灣)'.
- Contact phone number (聯絡電話): Input fields for area code (區碼), telephone number (電話號碼), extension (分機), and notes (非必填).
- Mobile phone number (手機): An input field.

Deadline: 9/11 23:59

需另外點選指導教授



EE2-231 Server Account (for 修課學生)

❖ <https://reurl.cc/Ny1kk9>

Deadline: 9/11 23:59



IC設計實驗室伺服器帳號申請表

實驗室規則：

1. 請勿任意 reboot 主機，破壞系統或做出對系統有害之行為，或將帳號借予他人使用，否則
若經查獲，立即刪除帳號，並交由教授處理。
2. 硬碟使用空間以大學部 1G、碩士班 5G、博士班 10G 為限。
3. 個人資料請隨時自行備份，並於隔年9/1前將個人目錄下的檔案清理乾淨，不保證檔案完整性。
4. 帳號預設期限為一學年，每年9/1將停止上學年申請之帳號，新的學年度請重新申請。
5. 其它注意事項請參閱本實驗室內的實驗室公布欄與實驗室網頁 <http://cad.ee.ntu.edu.tw>。
6. 本伺服器帳號需使用"校內IP"登入，如果是校外IP，請參考 <https://ccnet.ntu.edu.tw/vpn>。



個資同意書 (on NTU COOL)

❖ 只需簽名！

❖ 日期年用日不用填

Deadline: 9/11 23:59

經濟部工業局 蒐集個人資料告知事項暨個人資料提供同意書

版本：P-V5x-DTRI

經濟部工業局（以下簡稱本局）為遵守個人資料保護法令及本局個人資料保護政策、規章，於向您蒐集個人資料前，依法向您告知下列事項，敬請詳閱。

一、 蒐集目的及類別

本局因辦理或執行**公私(產學)共育國內外高階人才計畫**業務、活動、計畫、提供服務及供本局關於內部行政管理、陳報主管機關或其他合於本局所定業務，寄送本局或產業相關活動訊息之蒐集目的，而需獲取您下列個人資料類別：**姓名、性別、學校、系所、年級、國籍**。
當您日後如不願再收到本局所寄送之行銷訊息，可於收到前述訊息內拒絕接受之連結。

二、 個人資料利用之期間、地區、對象及方式

除涉及國際業務或活動外，您的個人資料僅供本局於中華民國領域，在前述蒐集目的之必要範圍內，以合理方式利用至蒐集目的消失為止。

三、 告知人權利

您可依前述業務、活動所定規則或以電子郵件聯繫(ici@iii.org.tw)向本局行使下列權利：

- (一) 查詢或請求閱覽。
- (二) 請求製給複製本。
- (三) 請求補充或更正。
- (四) 請求停止蒐集、處理及利用。
- (五) 請求刪除您的個人資料。

四、 不提供個人資料之權益影響

若您未提供正確或不提供個人資料，本局將無法為您提供蒐集目的相關服務。

五、 您瞭解此一同意書符合個人資料保護法及相關法規之要求，且同意本局留存此同意書，供日後取出查驗。

個人資料之同意提供：

- 一、本人已充分獲知且已瞭解上述經濟部工業局告知事項。
- 二、本人同意經濟部工業局於所列蒐集目的之必要範圍內，蒐集、處理及利用本人之個人資料。

立同意書人：

中　　華　　民　　國　　年　　月　　日



簽到表 (實體，線上請登入時用學號-姓名)



112 年經濟部工業局
公私(產學)共育國內外高階人才計畫
表格二：潛力學程-簽到表(實體活動)



日期		112 年 月 日		時間	00:00~00:00
主題				地點	
專家(顧問/講師) 簽名					
項次	就讀學校	科系	就讀年級 (如：碩一、大四...)	姓名	簽名 (中文正楷)
1.					
2.					
3.					
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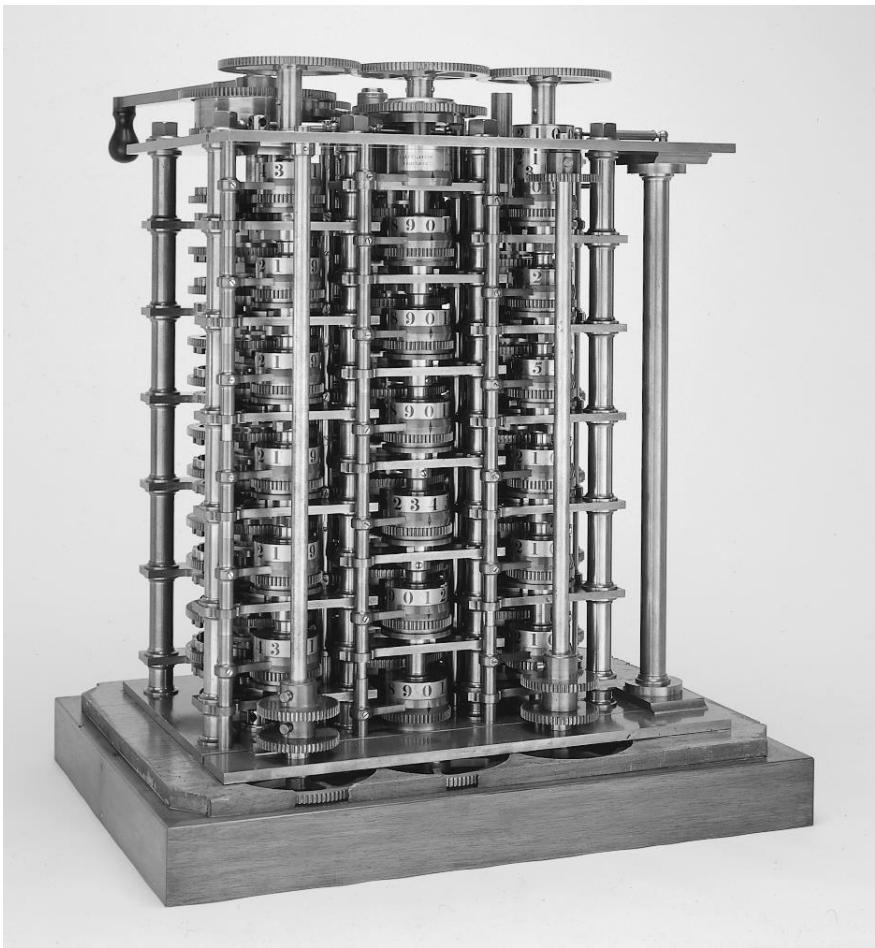


Digital Design Using Integrated Circuits (IC)

& Very Large-Scale IC (VLSI)



The First Computer



**The Babbage
Difference Engine
(1832)**

25,000 parts
Cost: 17,470 Pounds
in Year 1832

Use Relays as switching components

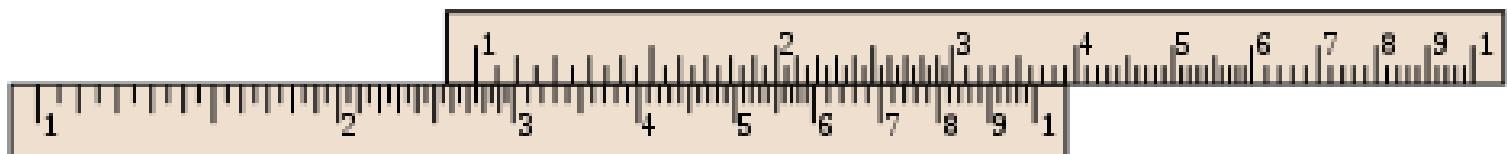


Slide Rule



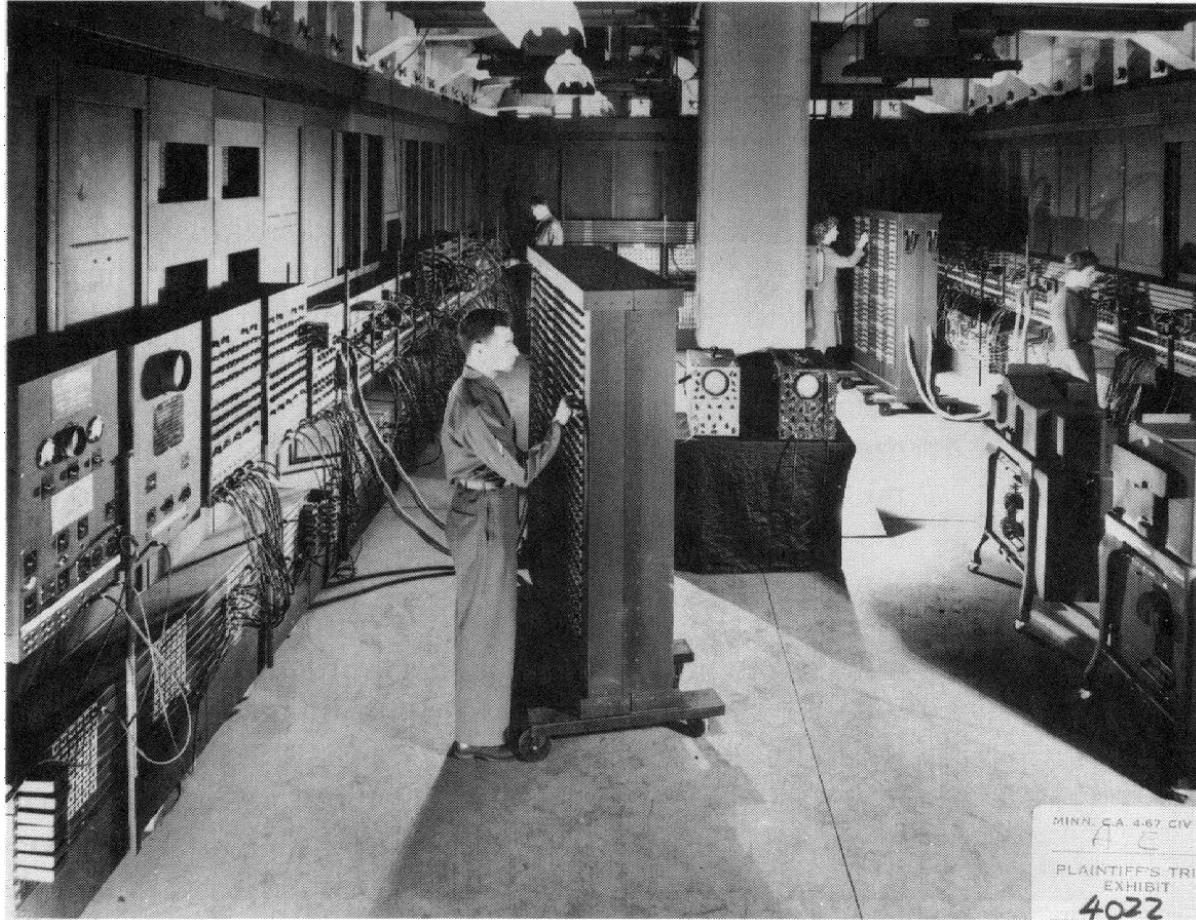
http://en.wikipedia.org/wiki/Slide_rule

The illustration below demonstrates the computation of $5.5/2$. The 2 on the top scale is placed over the 5.5 on the bottom scale. The 1 on the top scale lies above the quotient, 2.75.





ENIAC - The first electronic computer (1946)



Use Vacuum Tubes as switching components



Technologies for Building Processors & Memories

❖ Vacuum tube

- ❖ An electronic component, predecessor of the transistor, that consists of a hollow glass tube about 5 to 10 cm long from which as much air has been removed as possible and which uses an electron beam to transfer data

❖ Transistor

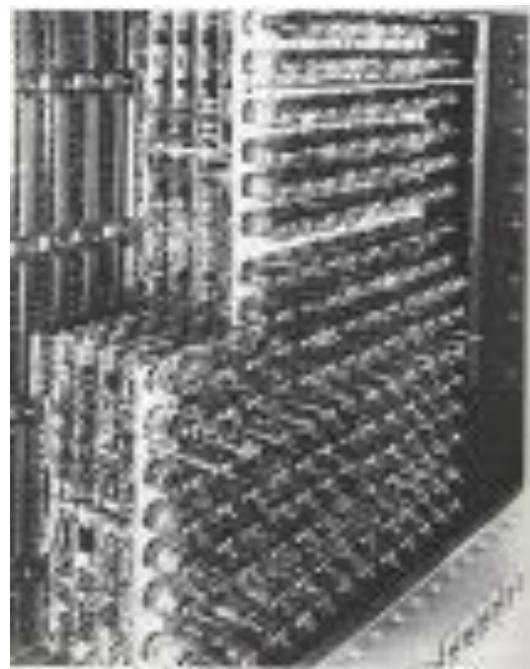
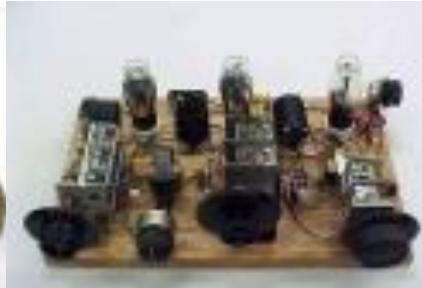
- ❖ An ON/OFF switch controlled by an electric signal

❖ Very large scale integrated (VLSI) circuit

- ❖ A device containing hundreds of thousands to millions of transistors

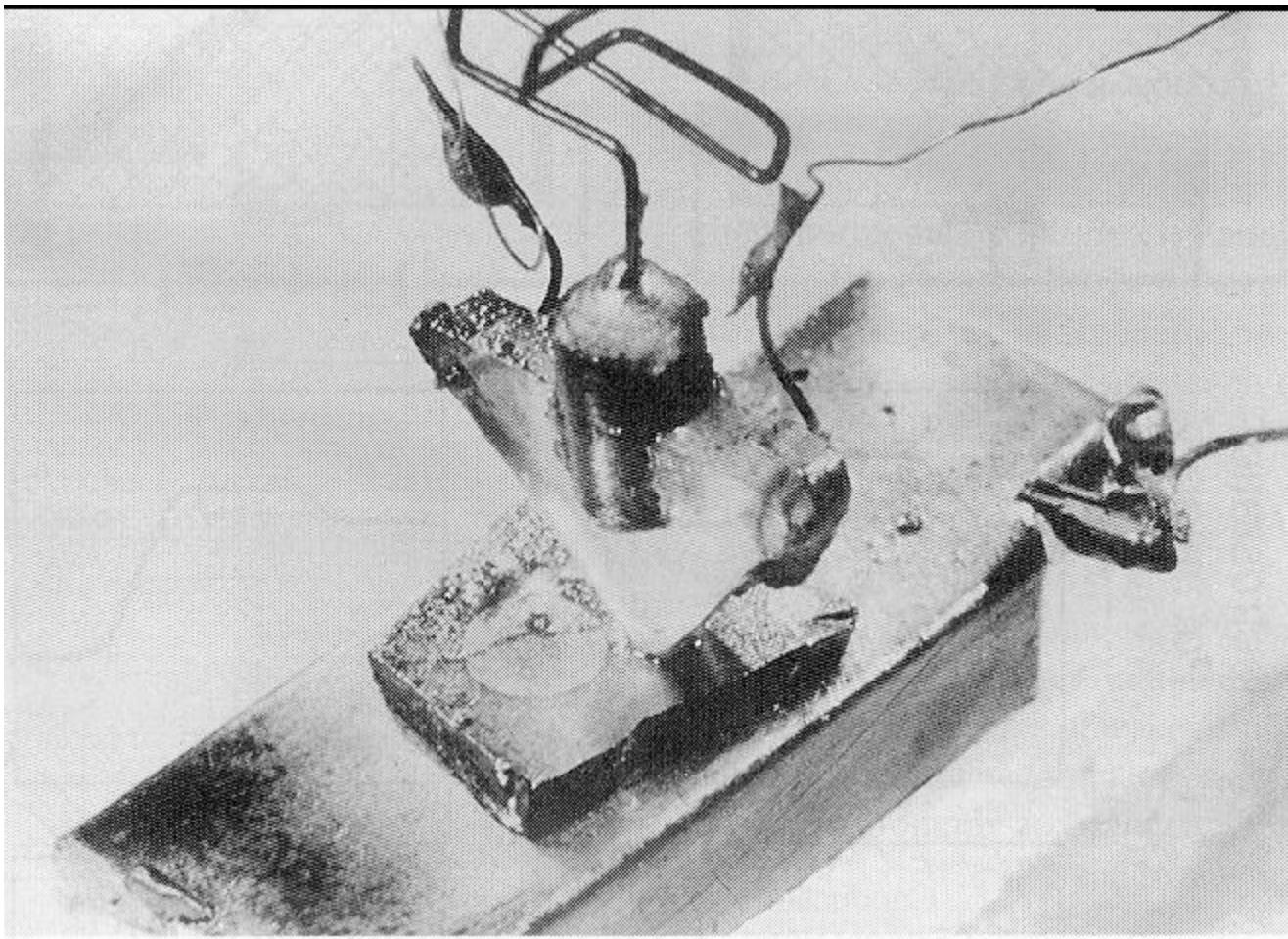


Vacuum Tube





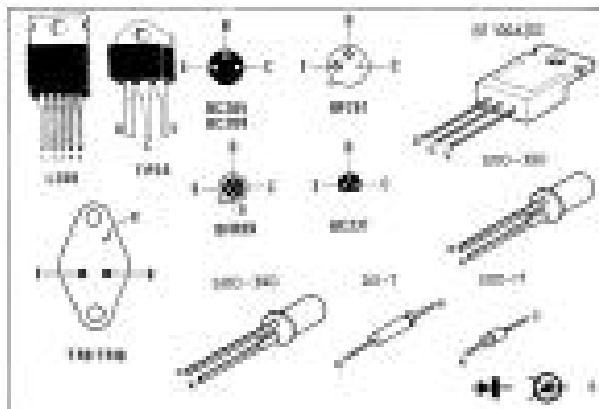
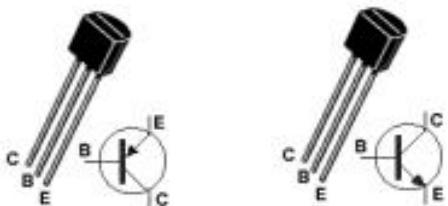
The Transistor Revolution



First transistor
Bell Labs, 1948

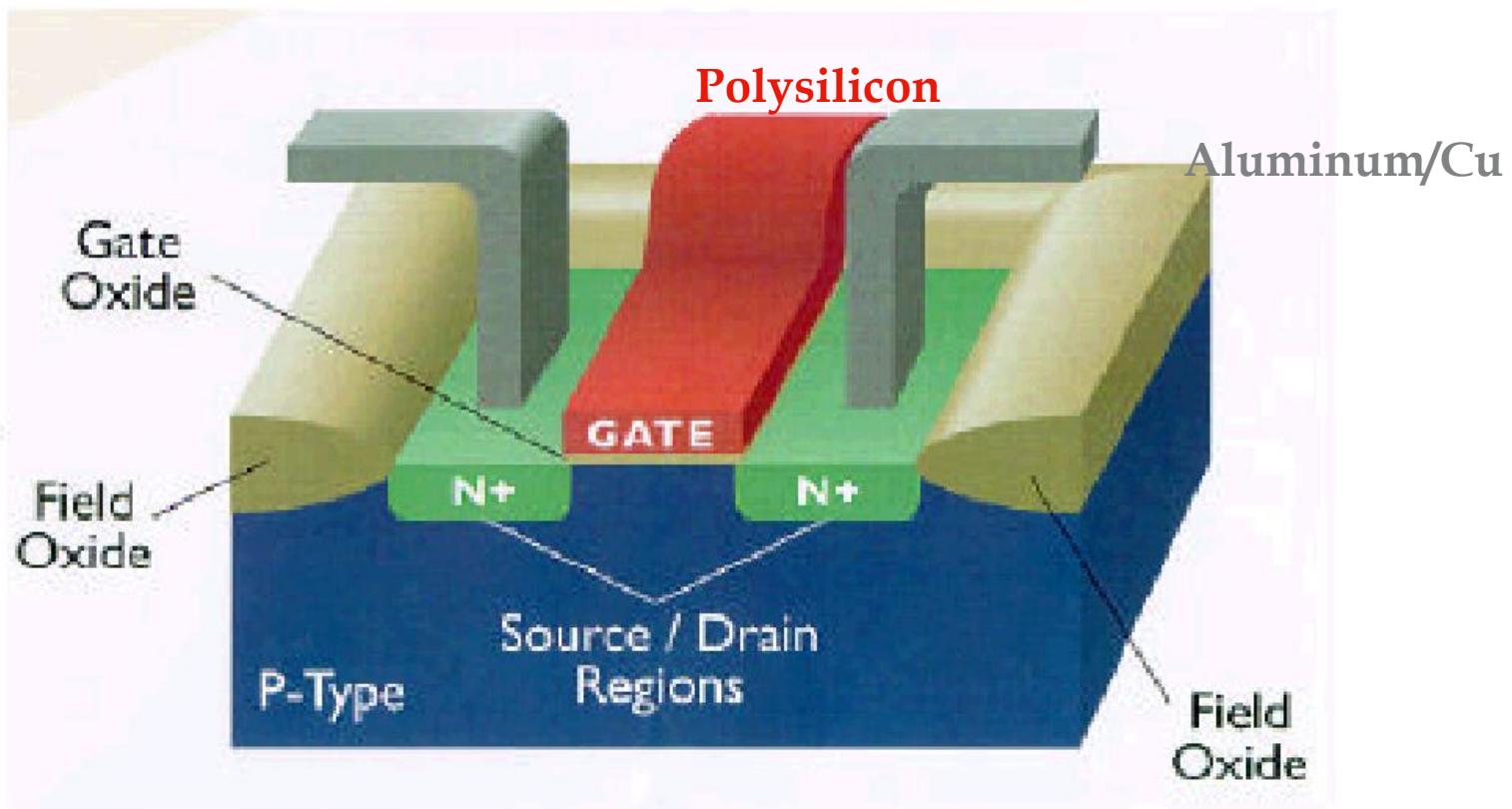


Discrete Transistors



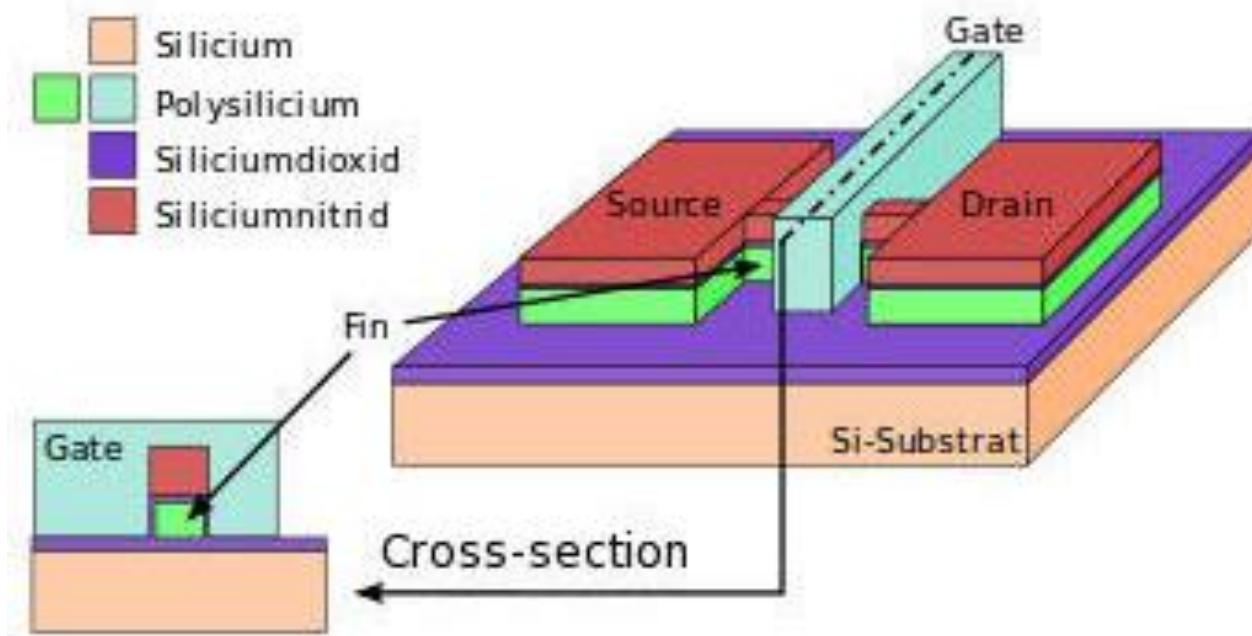


The MOS Transistor





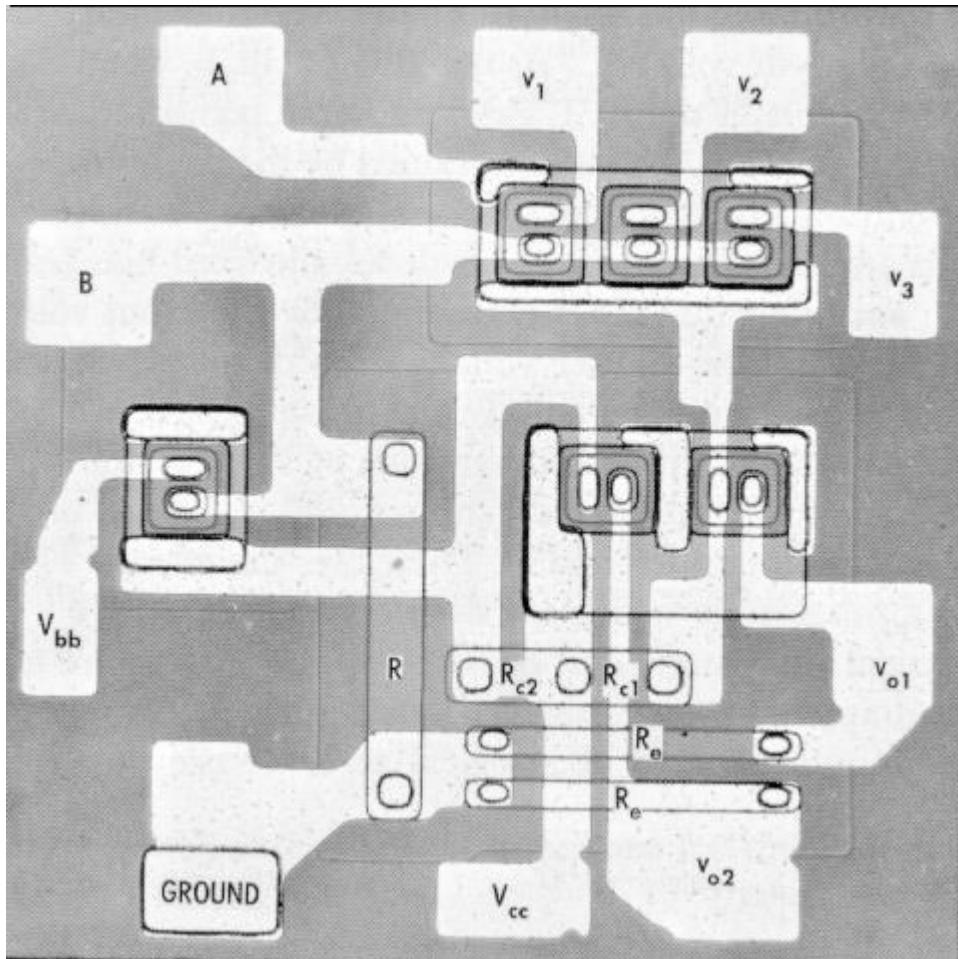
FinFET Device Schematic



ComputerHope.com



The First Integrated Circuits

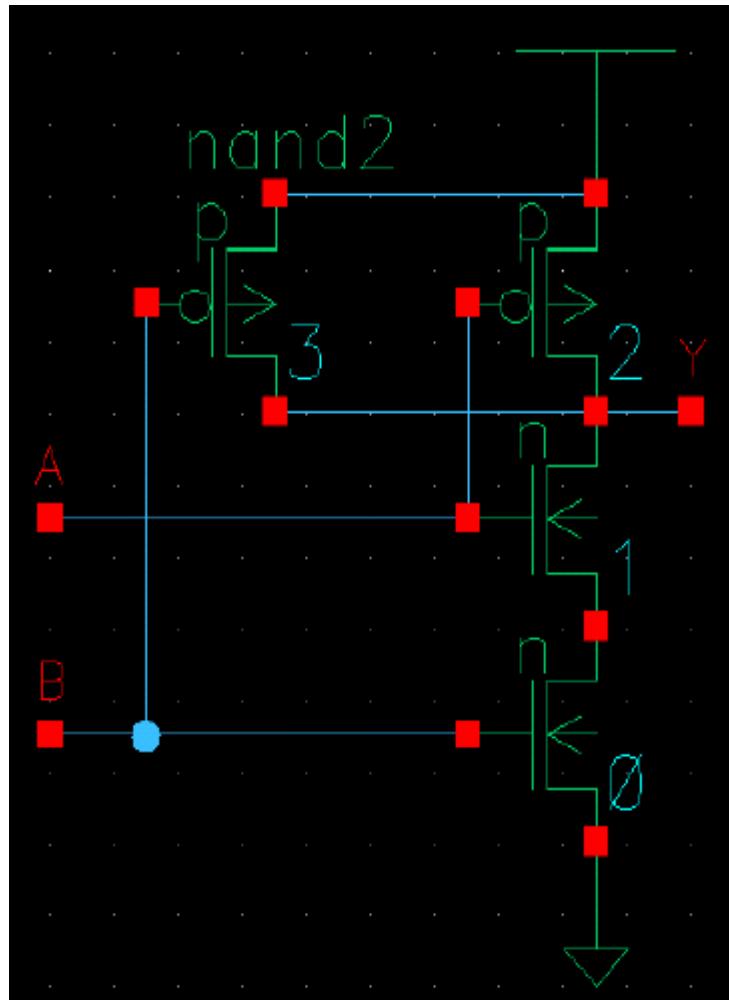
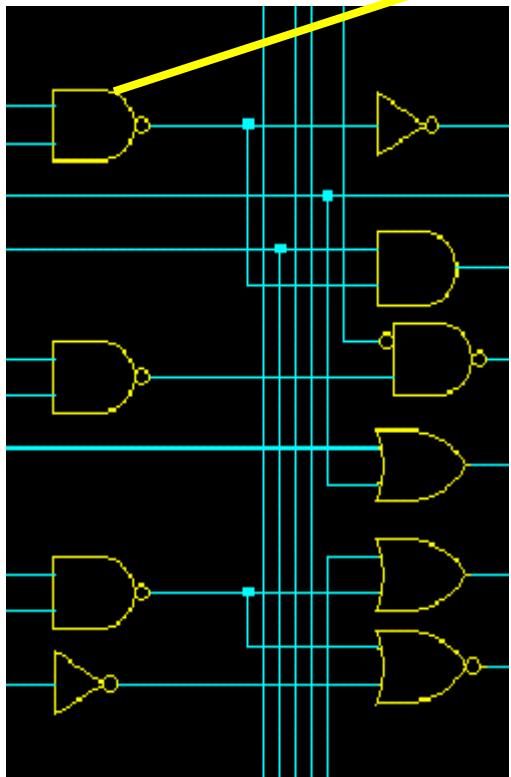


Bipolar logic
1960's

ECL 3-input Gate
Motorola 1966

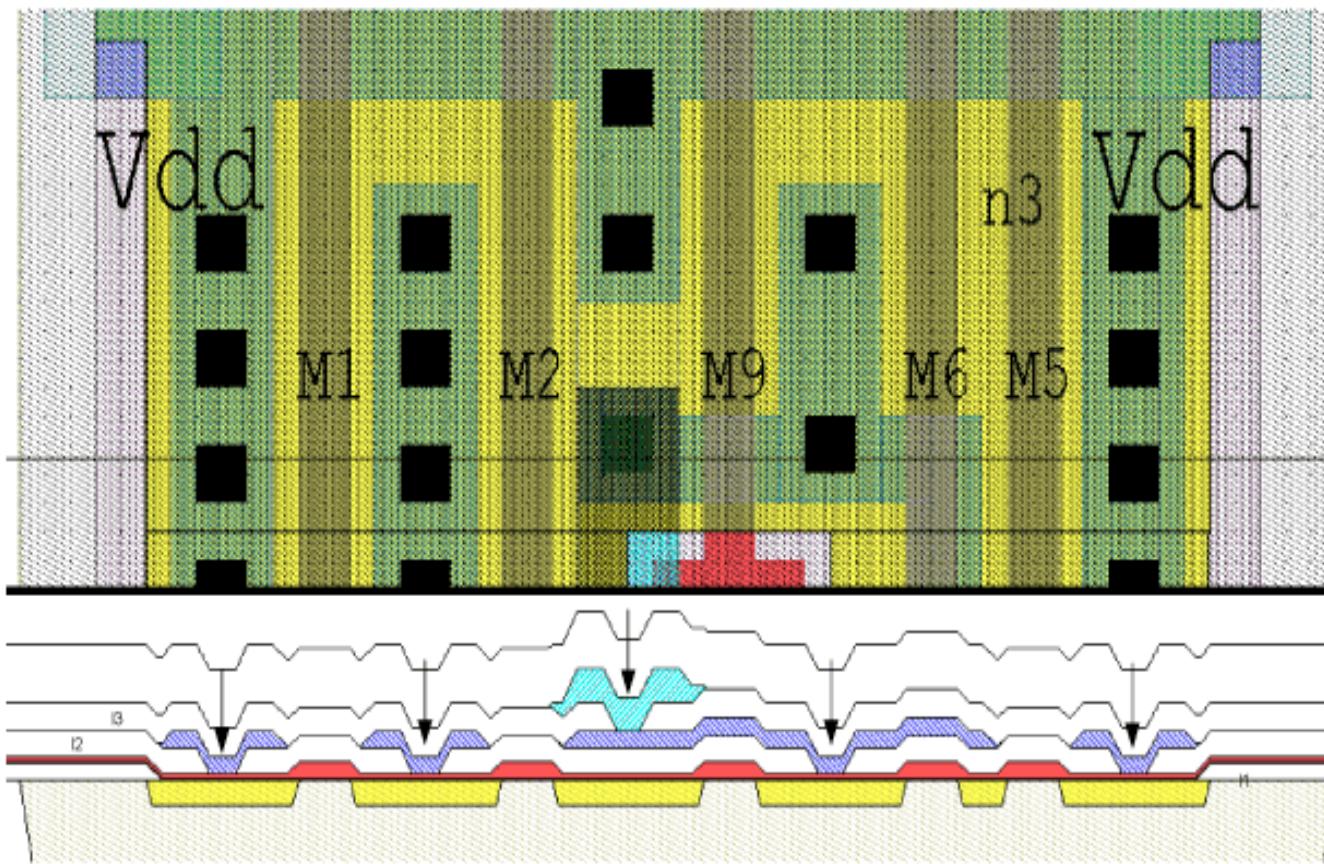


Gate and Circuit Level Design



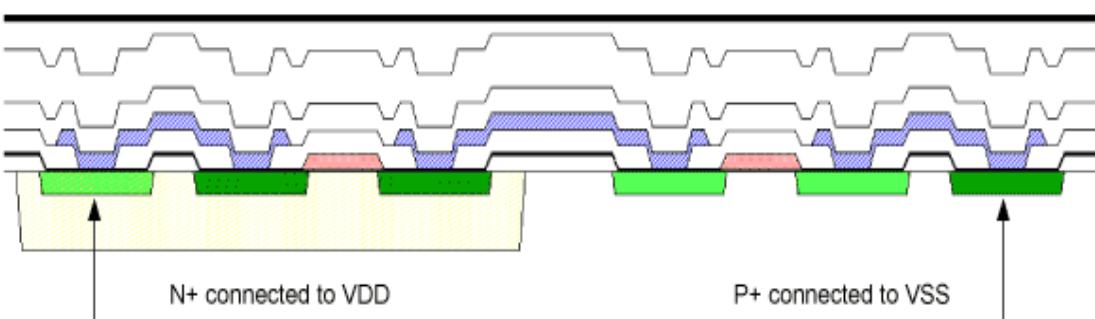
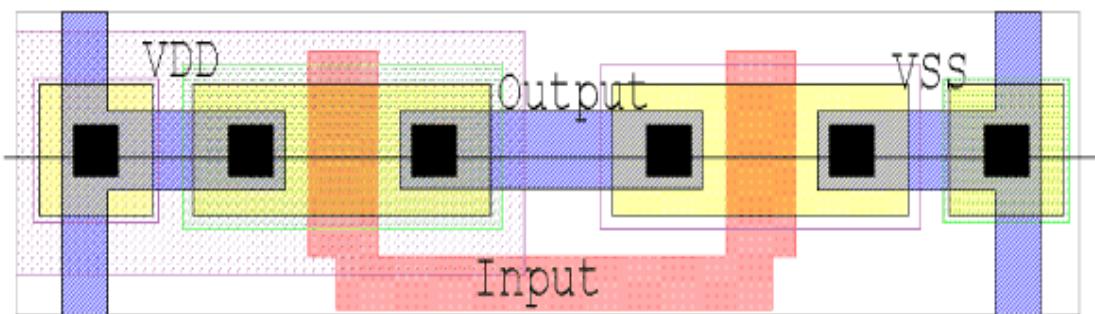
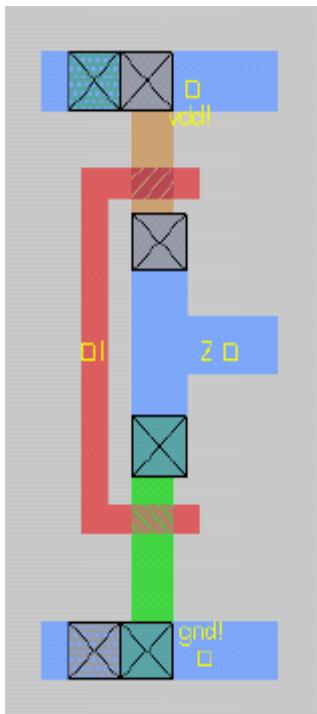


Mapping of Layout to IC Layers



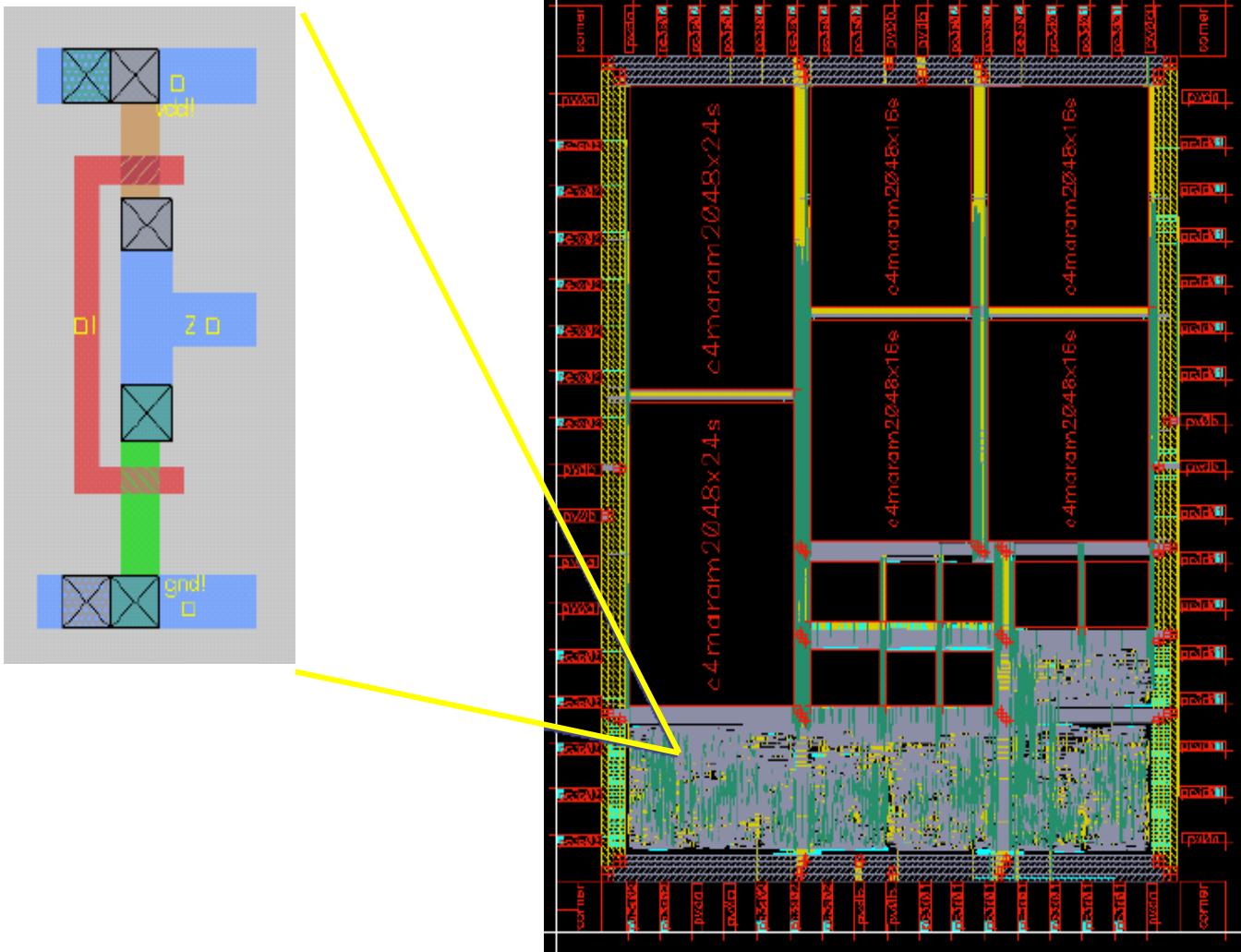


Layout of an CMOS Inverter



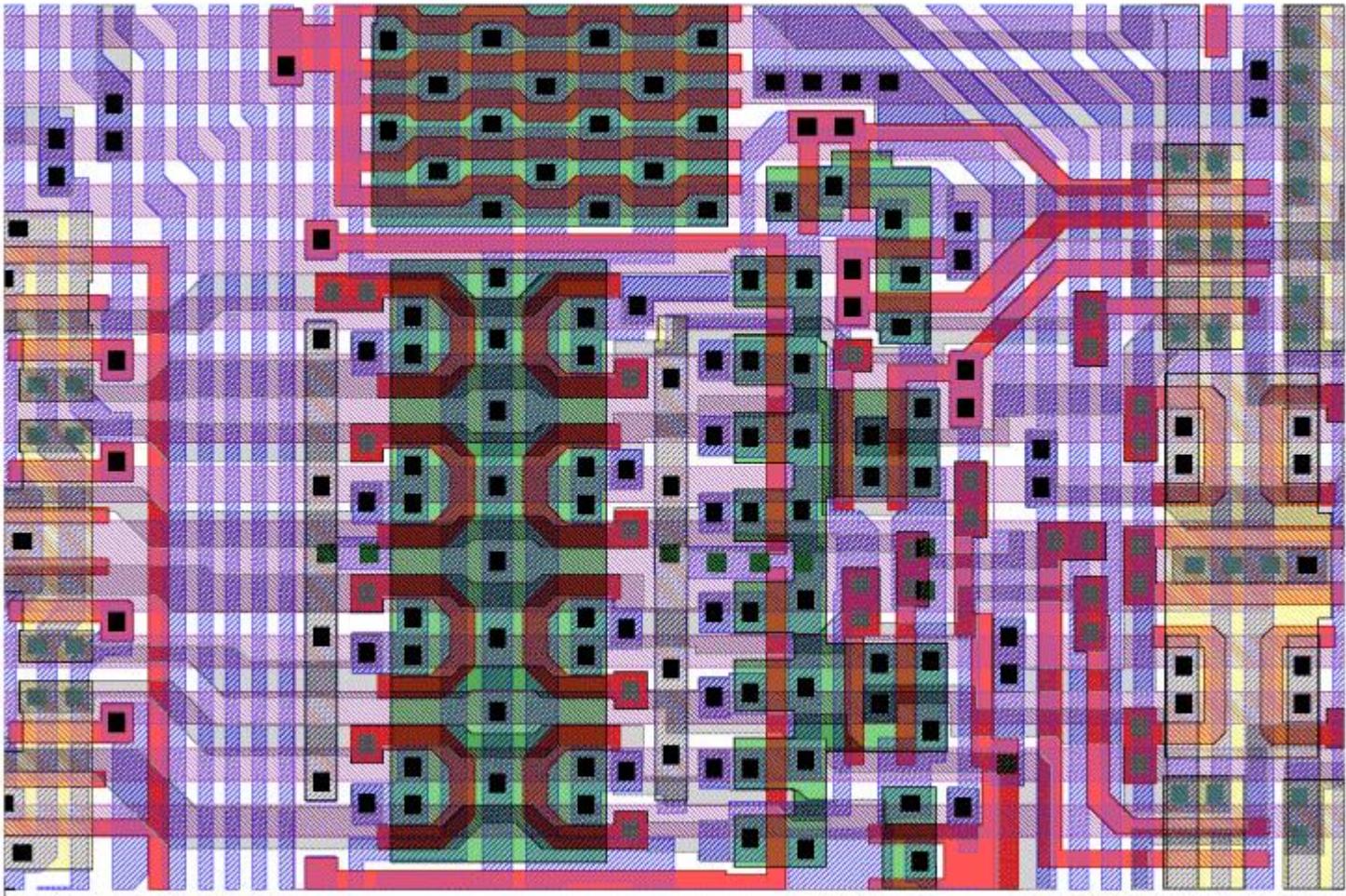


Physical Design



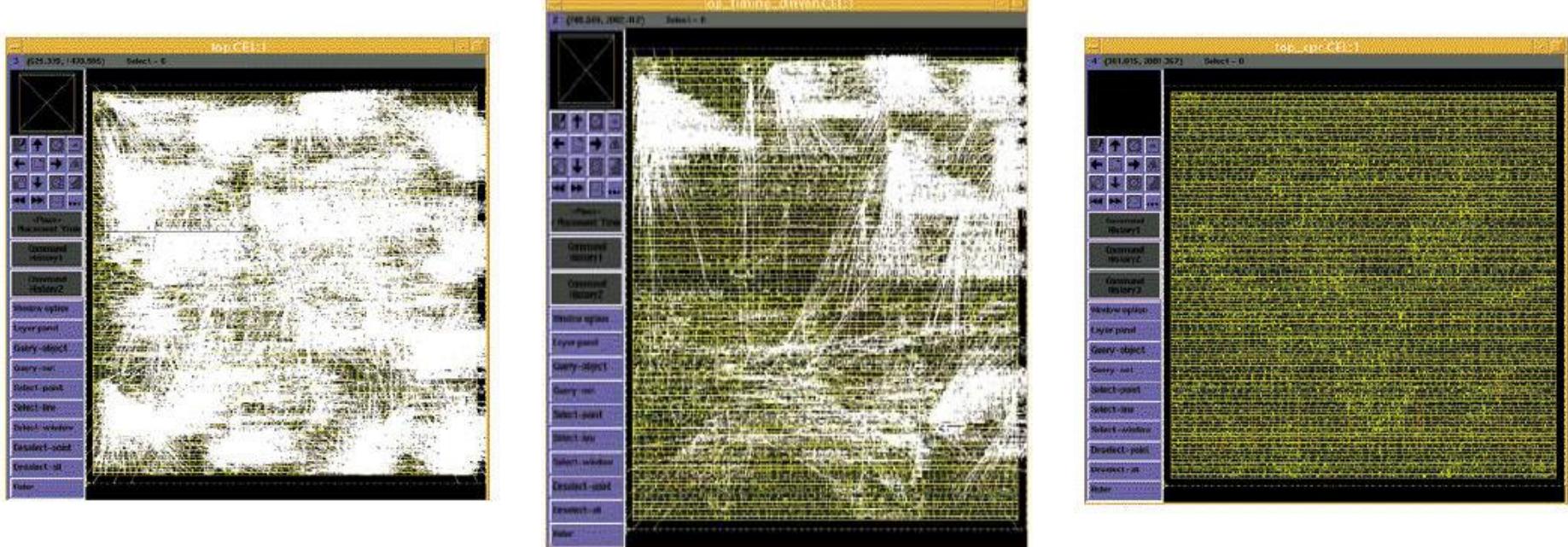


Physical Layout of your design





The “Timing Closure” Problem

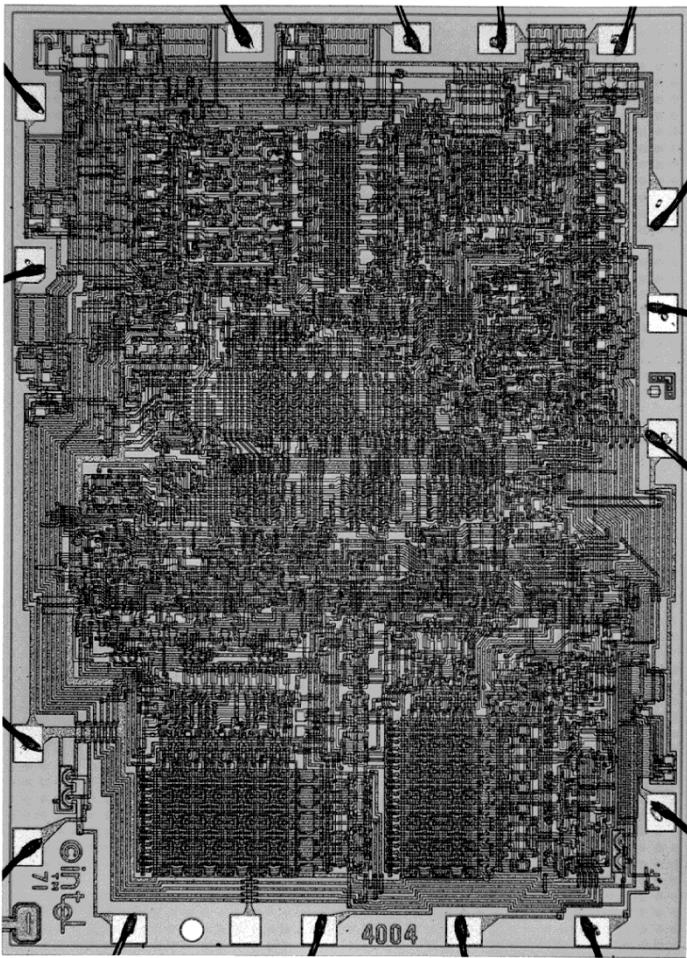


Iterative Removal of Timing Violations (white lines)

Courtesy Synopsys



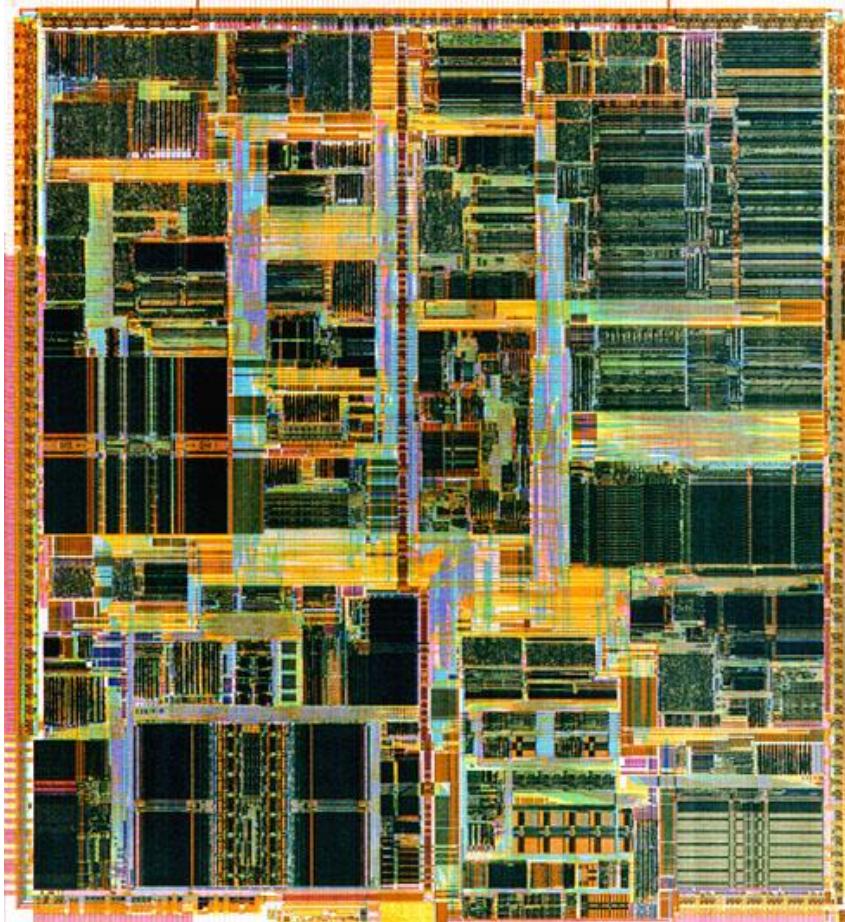
Example: Intel 4004 Micro-Processor



1971
1000 transistors
1 MHz operation

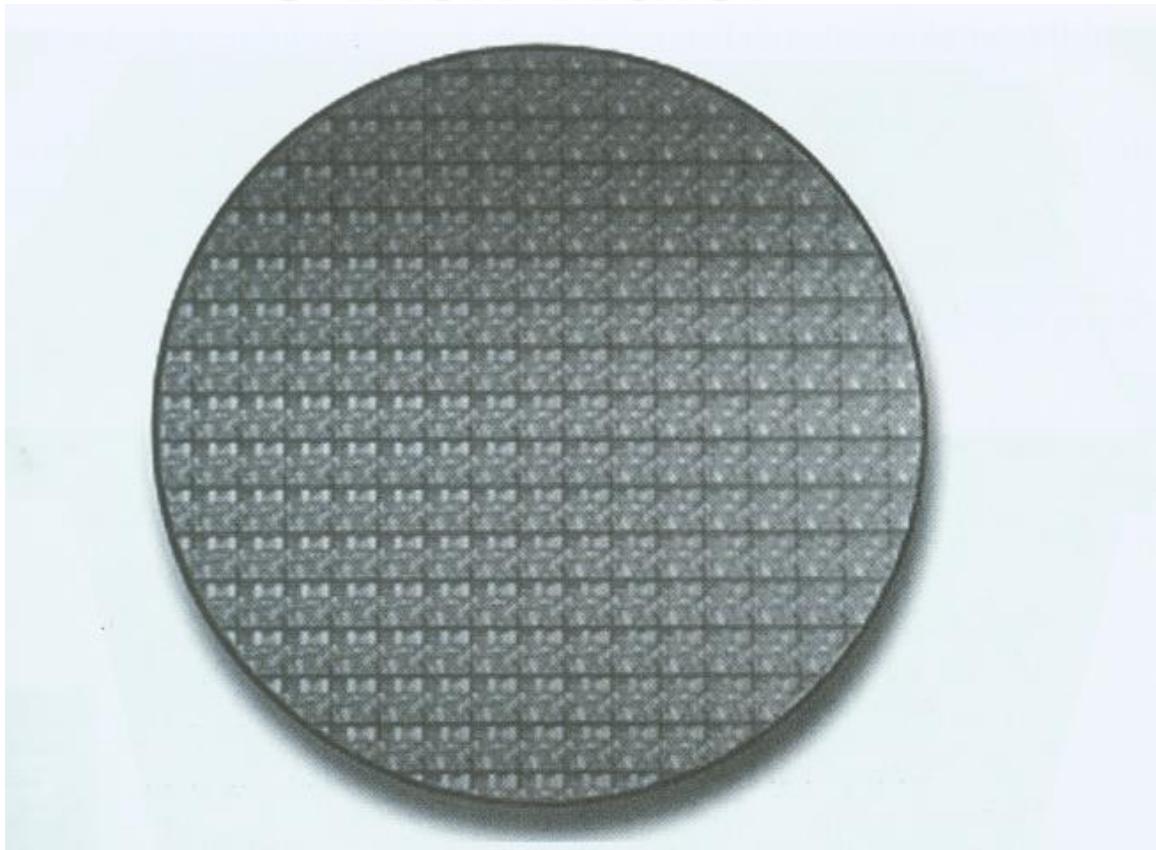


Intel Pentium (IV) microprocessor





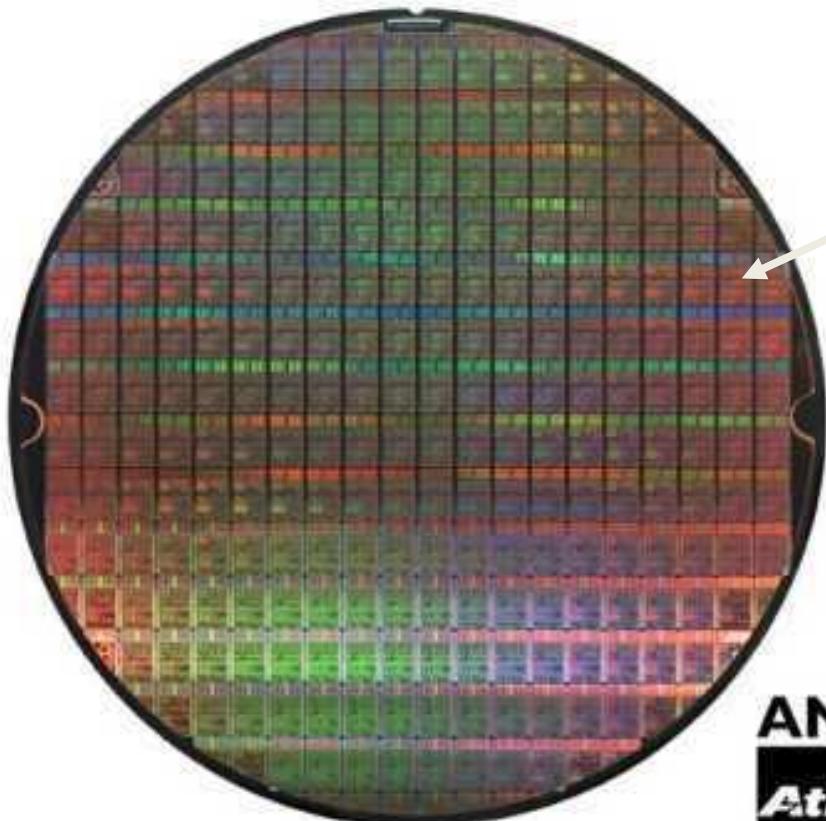
8-inch Wafer



An 8-inch (200-mm) diameter wafer containing Intel Pentium 4 processors



Die Cost



Single die

Wafer

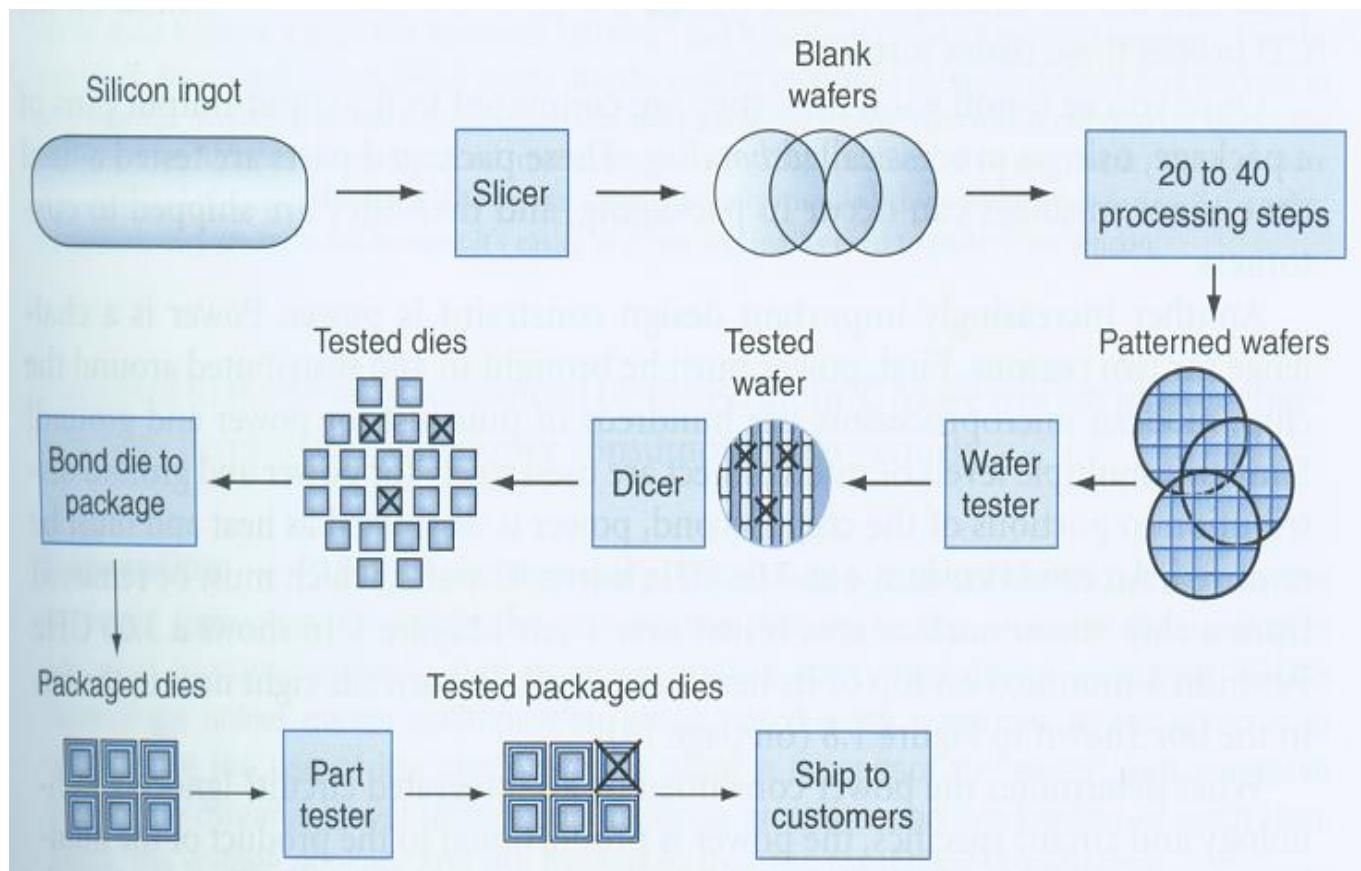


Going up to 18"

From <http://www.amd.com>

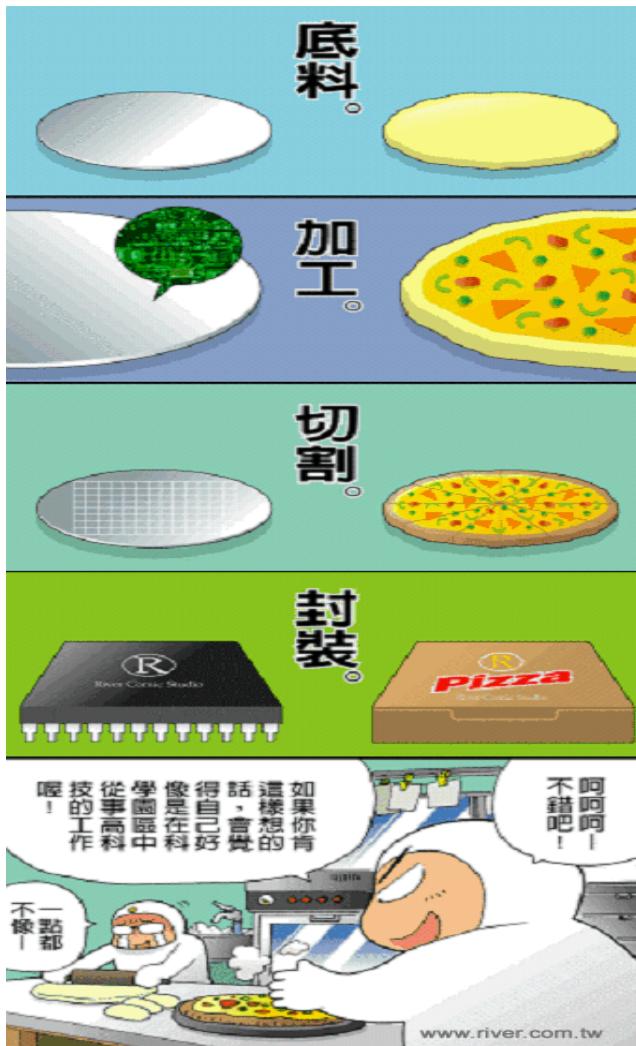


The Chip Manufacturing Process





Process vs. Pizza Making





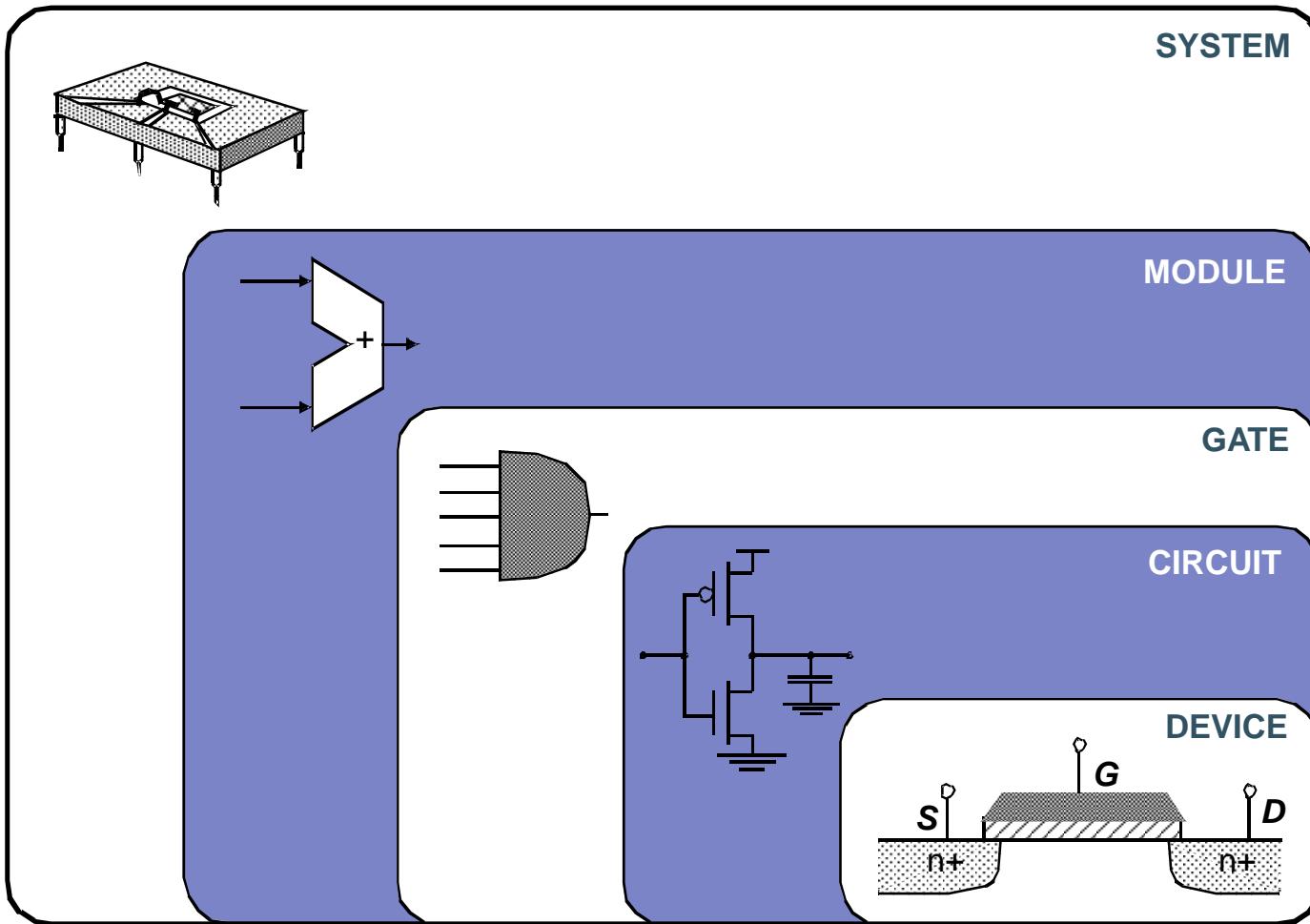
Technologies for Building Processors & Memories

Year	Technology used in computers	Relative performance/unit cost
1951	Vacuum tube	1
1965	Transistor	35
1975	Integrated circuit	900
1995	Very large scale integrated circuit	2,400,000
2005	Ultra large scale integrated circuit	6,200,000,000

Relative performance per unit cost of technologies used in computers over time

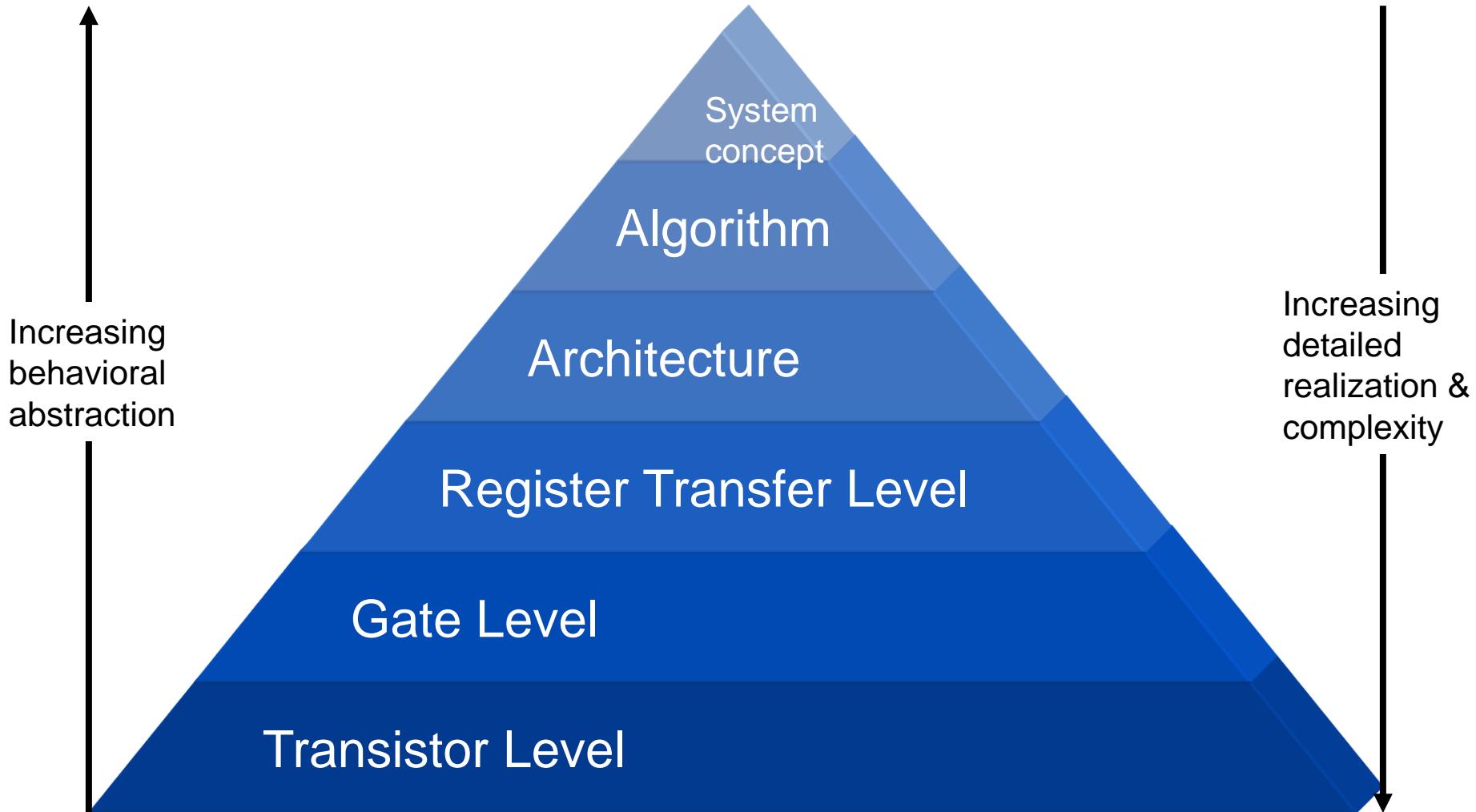


Design Abstraction Levels





Behavioral Model





Moore's Law vs. HDL

Issue : Design Productivity



Review of Full-custom Analog Design Flow



Schematic of 741 Op-amp Circuits

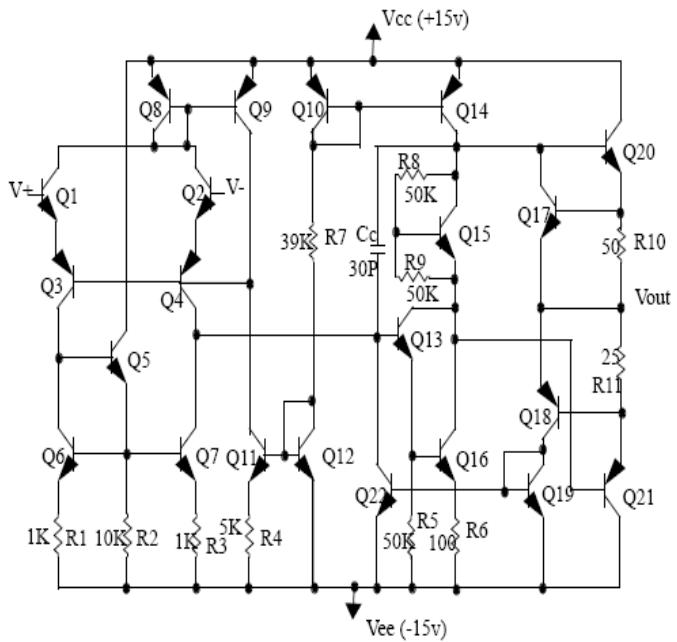
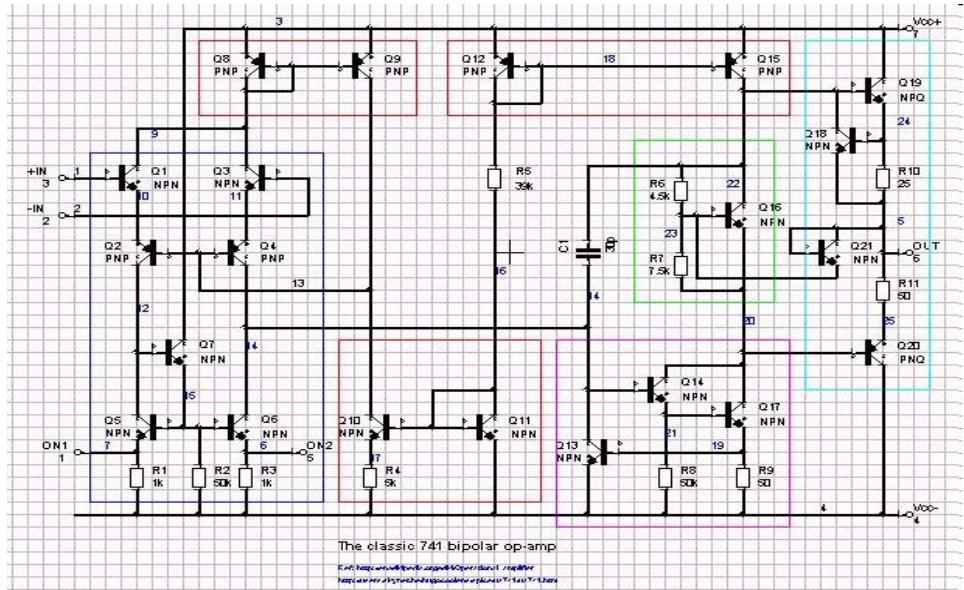


Fig. 1(a) Transistor level circuit diagram for op741



The classic 741 bipolar op-amp

Kap. 10: Несколько способов создания иерархии

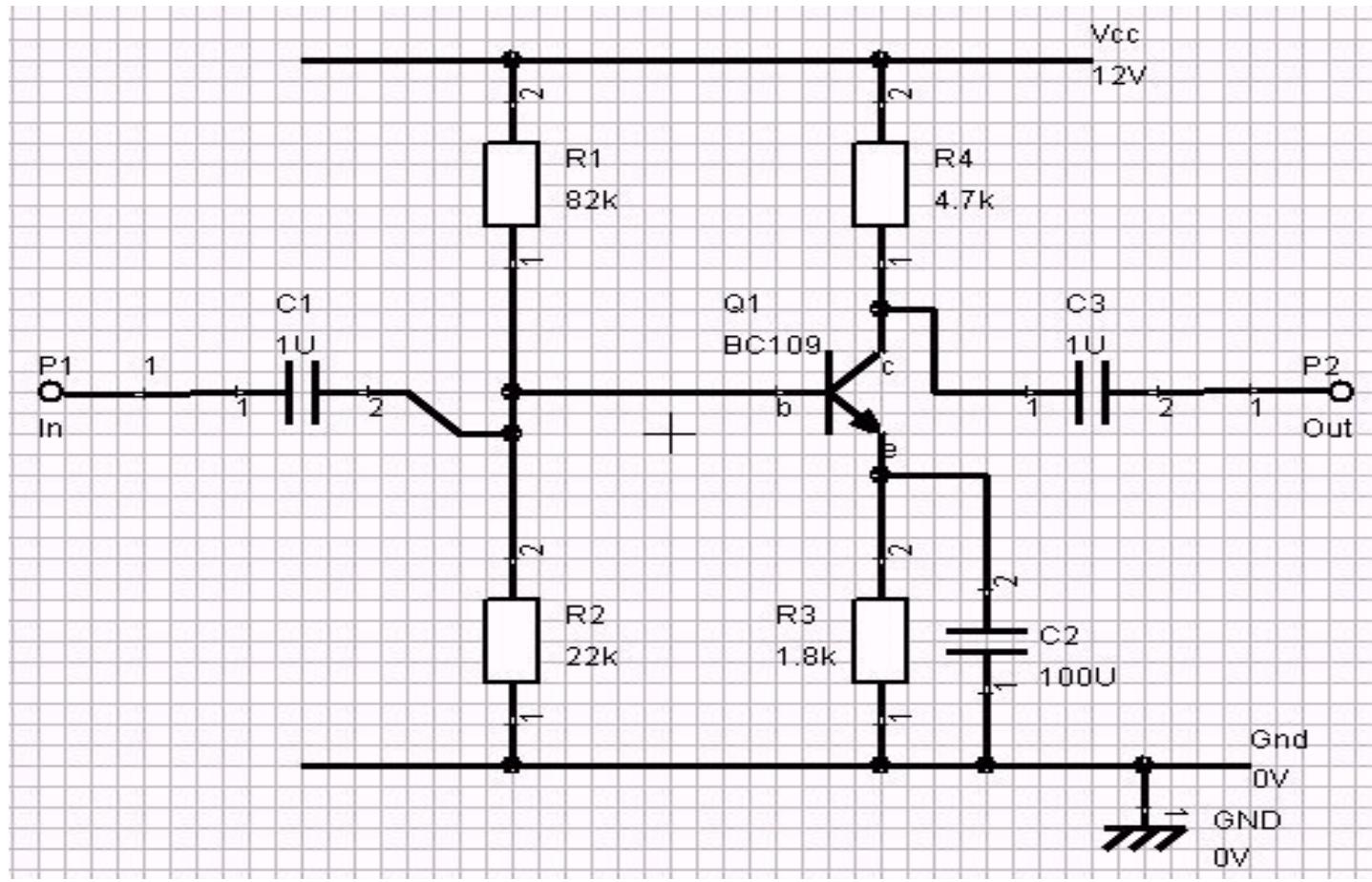
Keep writing until the space below is filled up to the top line.

Schematic
(Transistor level
circuit diagram)
for op741

Editing In EDA tools



SPICE (I)





SPICE (II) – Manual programming or Export from Schematic

- ❖ When you export the SPICE netlist, you get the following file:

*SPICE BJT Amplifier

C1 5 1 1U

C3 2 4 1U

C2 0 6 100U

Q1 2 1 6 ZTX109 1.0

R1 1 3 82k

R4 2 3 4.7k

R2 0 1 22k

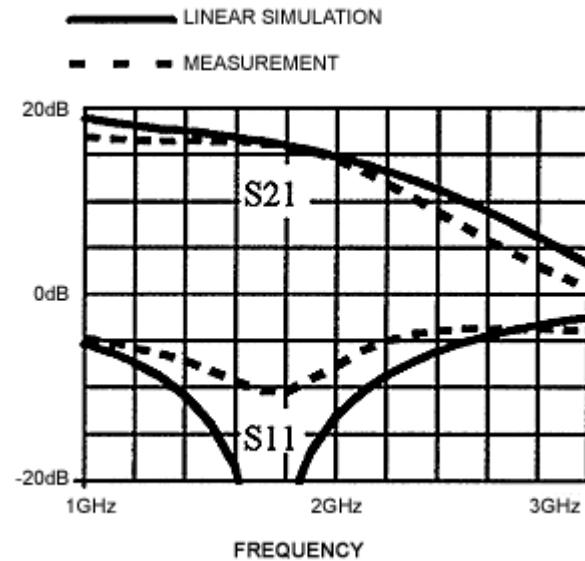
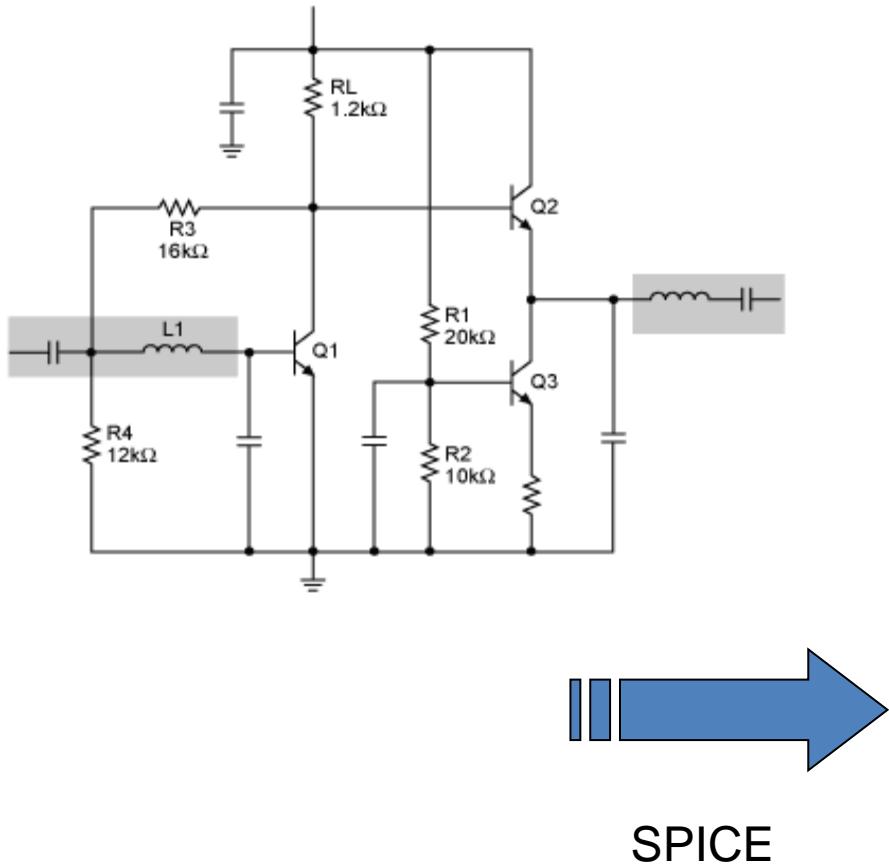
R3 0 6 1.8k

C4 0 3 100u

.MODEL ZTX109 NPN IS=1.8E-14 ISE=5.0E-14 NF=.9955 BF=400 BR=35.5
+IKF=.14 IKR=.03 ISC=1.72E-13 NC=1.27 NR=1.005 RB=.56 RE=.6 RC=.25
+VAF=80 VAR=12.5 CJE=13E-12 TF=.64E-9 CJC=4E-12 TR=50.72E-9
MJC=.33 .END



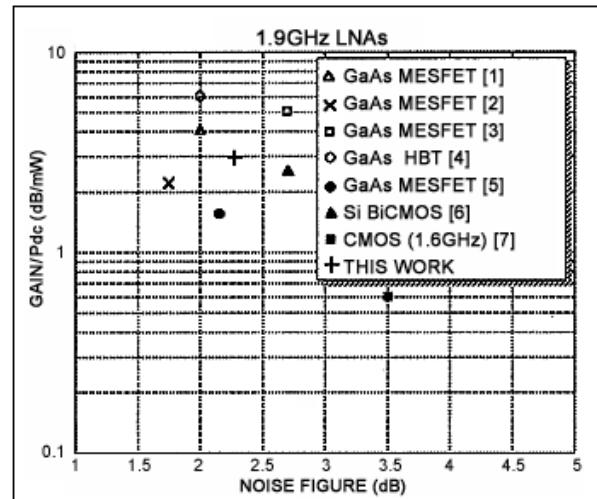
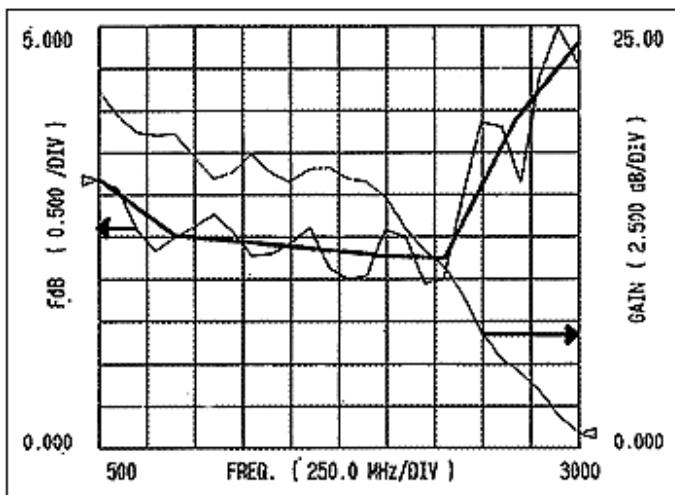
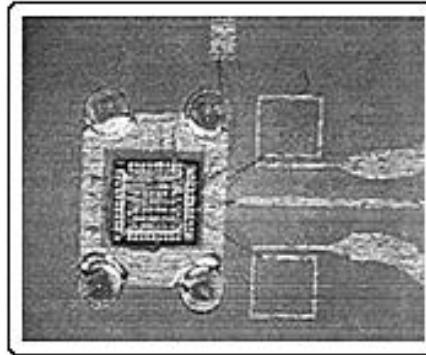
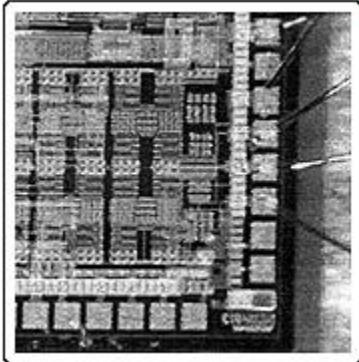
Schematic Inputs and Simulations of A two-stage 1.9GHz monolithic low-noise amplifier (LNA)



Source: <http://www.elecfans.com/article/84/148/2008/2008091712654.html>



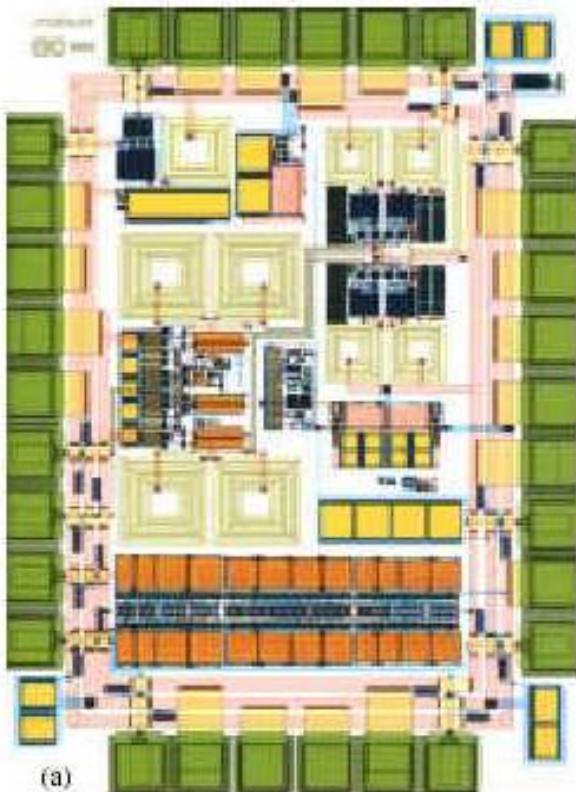
Fabrication of Chips and Measurement Results



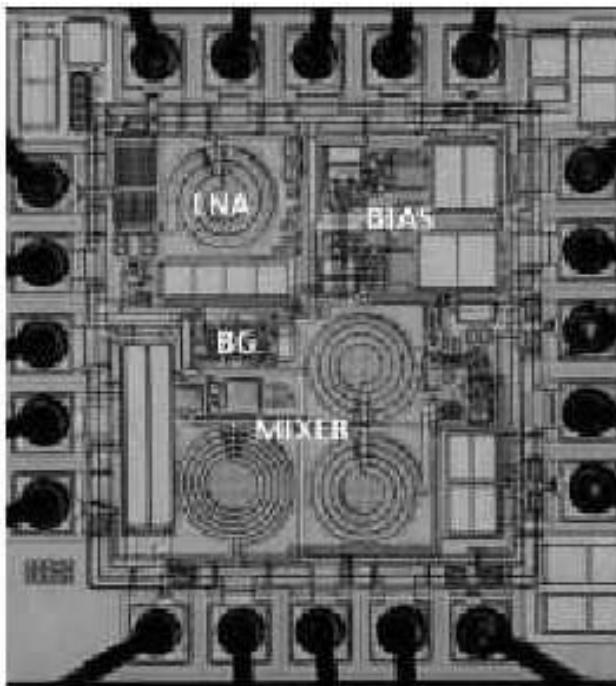
Source: <http://www.elecfans.com/article/84/148/2008/2008091712654.html>



7. 2-GHz Single-Chip Radio Developed at Stanford.



Layout (EDA tool result)



Die Photo (chip view)



Summary:

Full-custom Analog Design Flow



Lower Design
Productivity

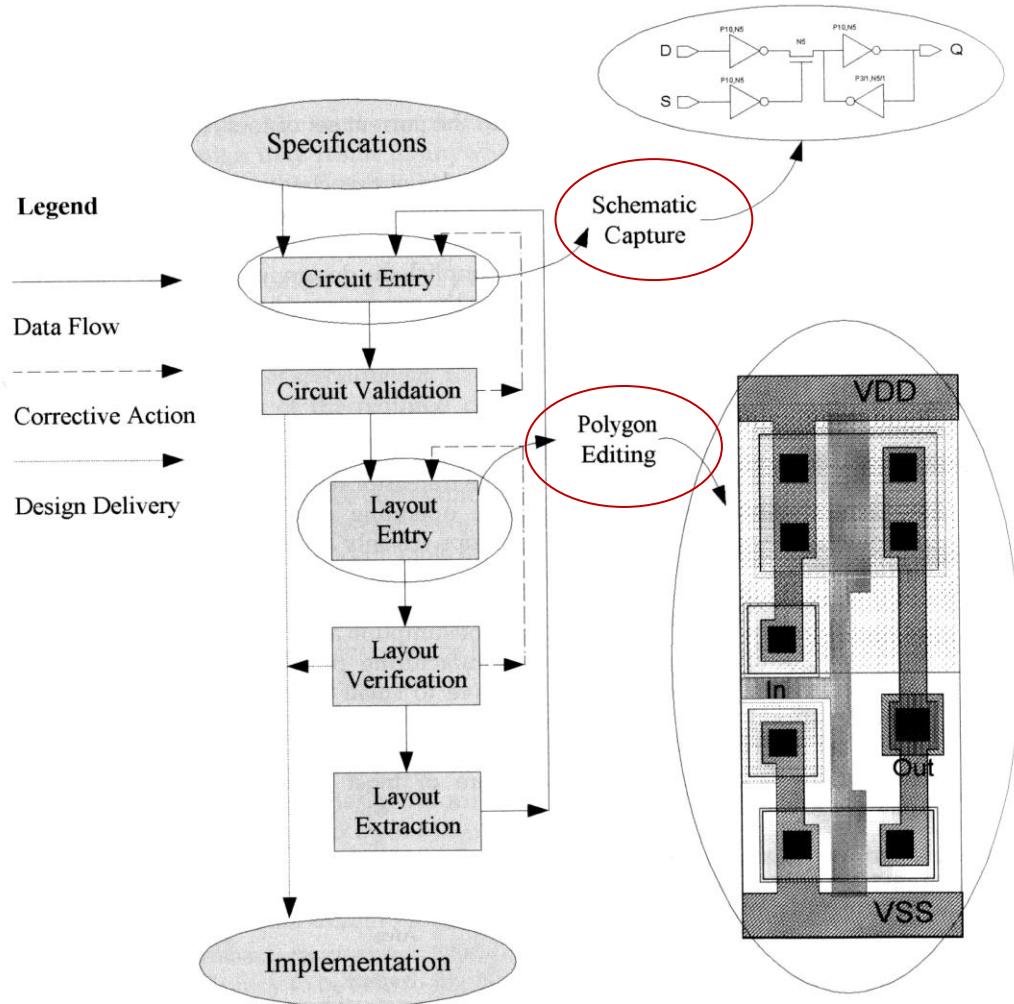


Figure 4.3 Full-custom (or analog) design flow.



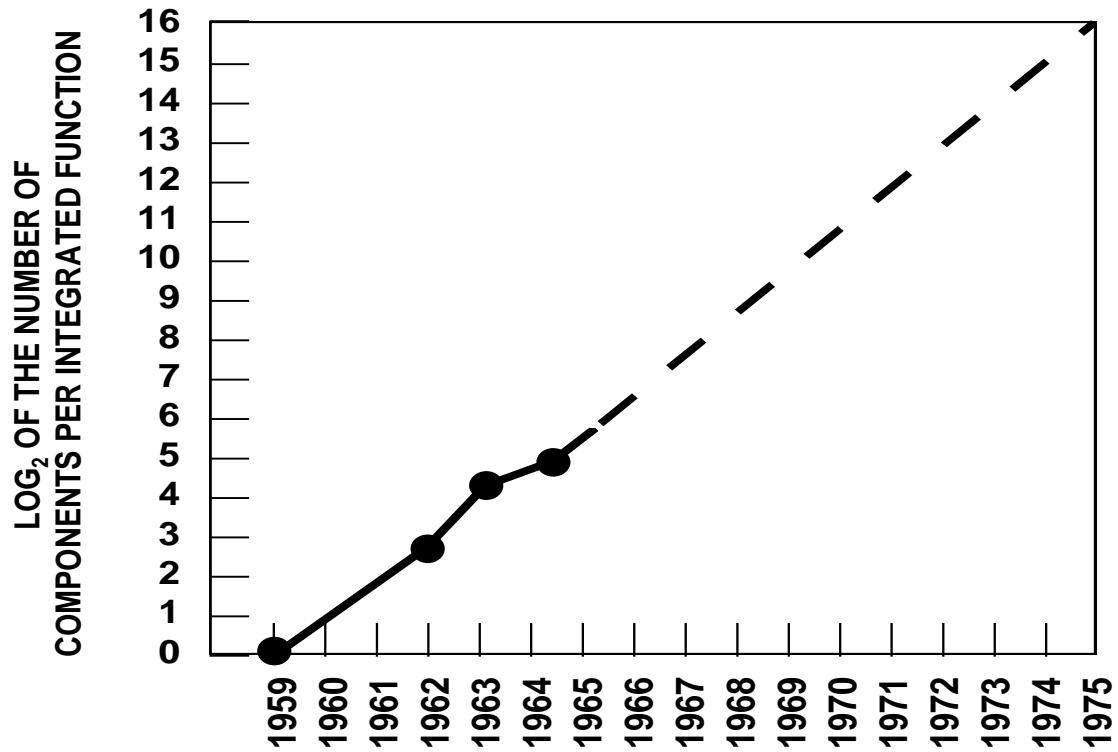
Moore's Law

In 1965, *Gordon Moore* noted that the number of transistors on a chip doubled every 18 to 24 months.

He made a prediction that semiconductor technology will **double** its effectiveness **every 18~24 months**



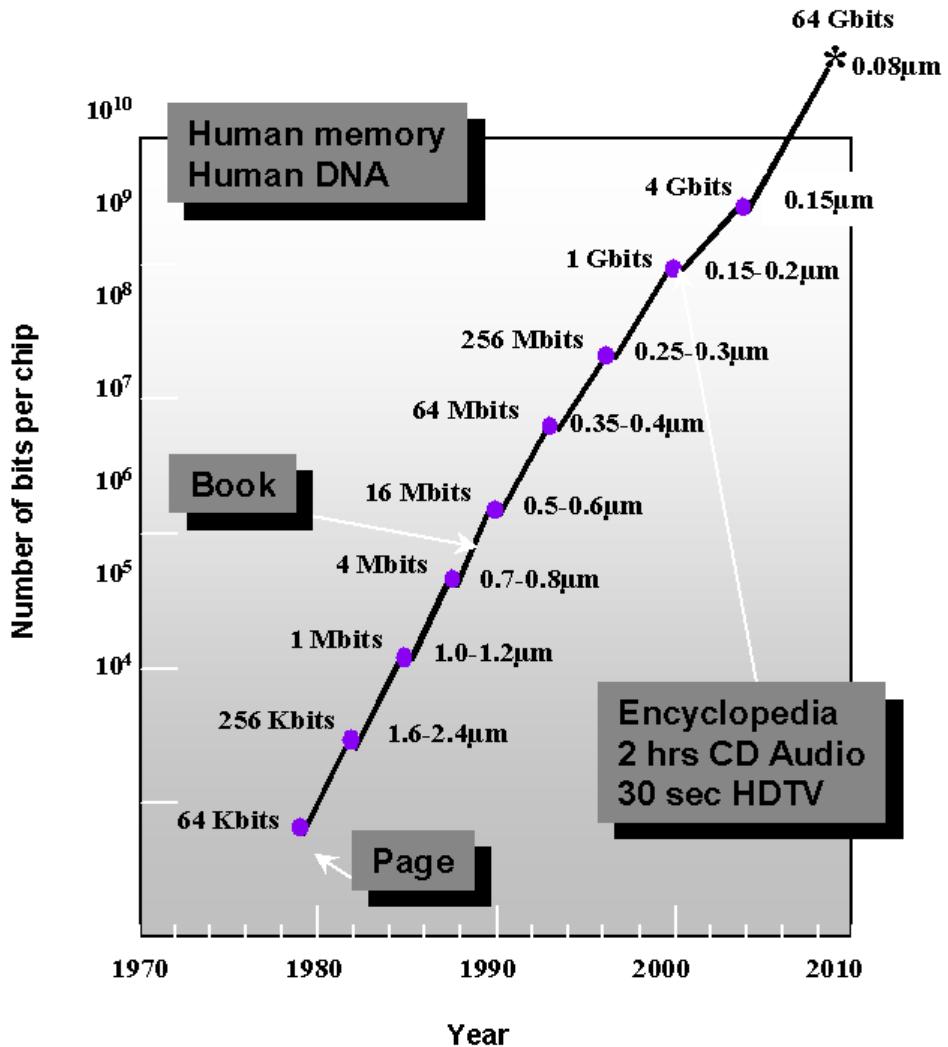
Moore's Law



Electronics, April 19, 1965.



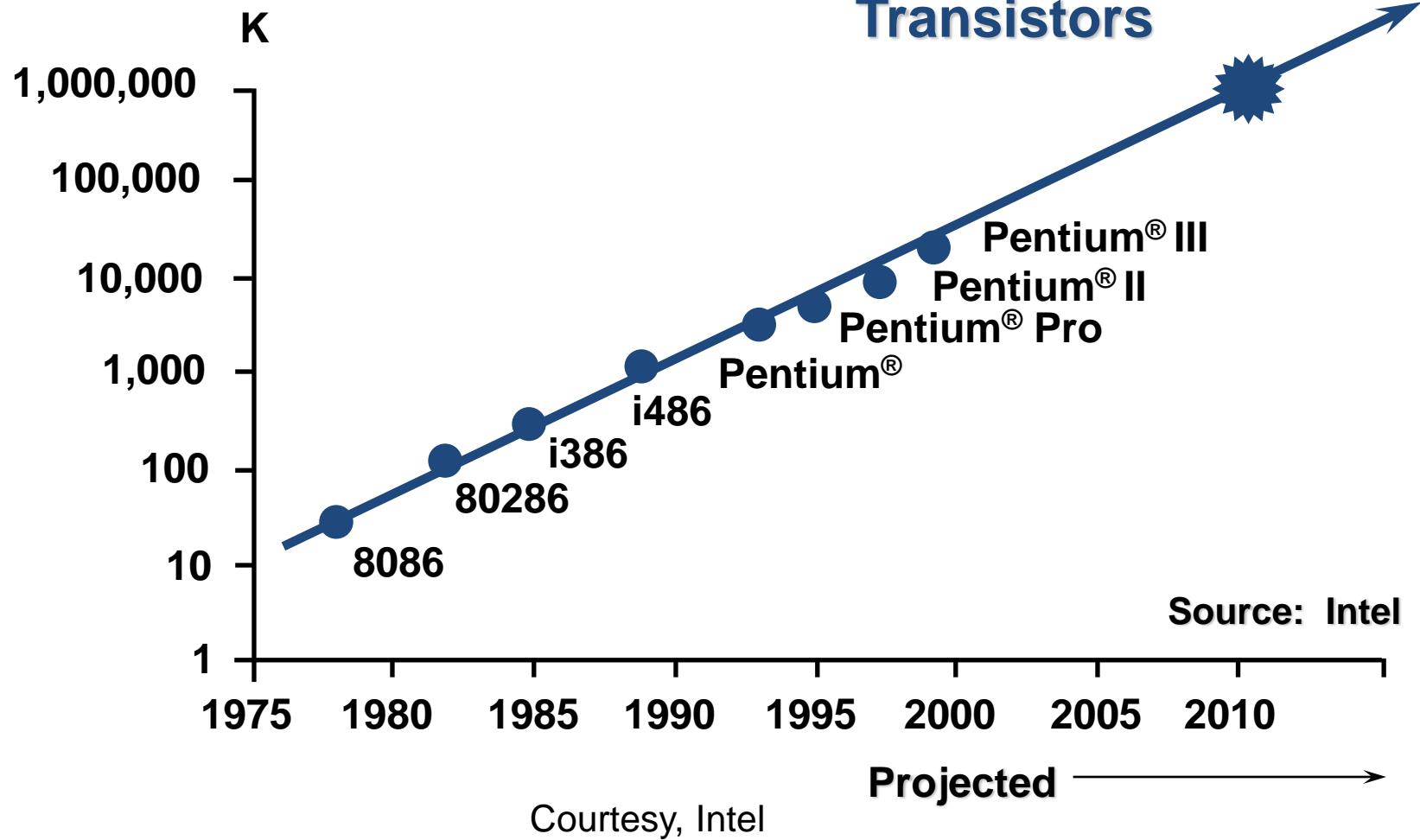
Evolution in Complexity





Transistor Counts

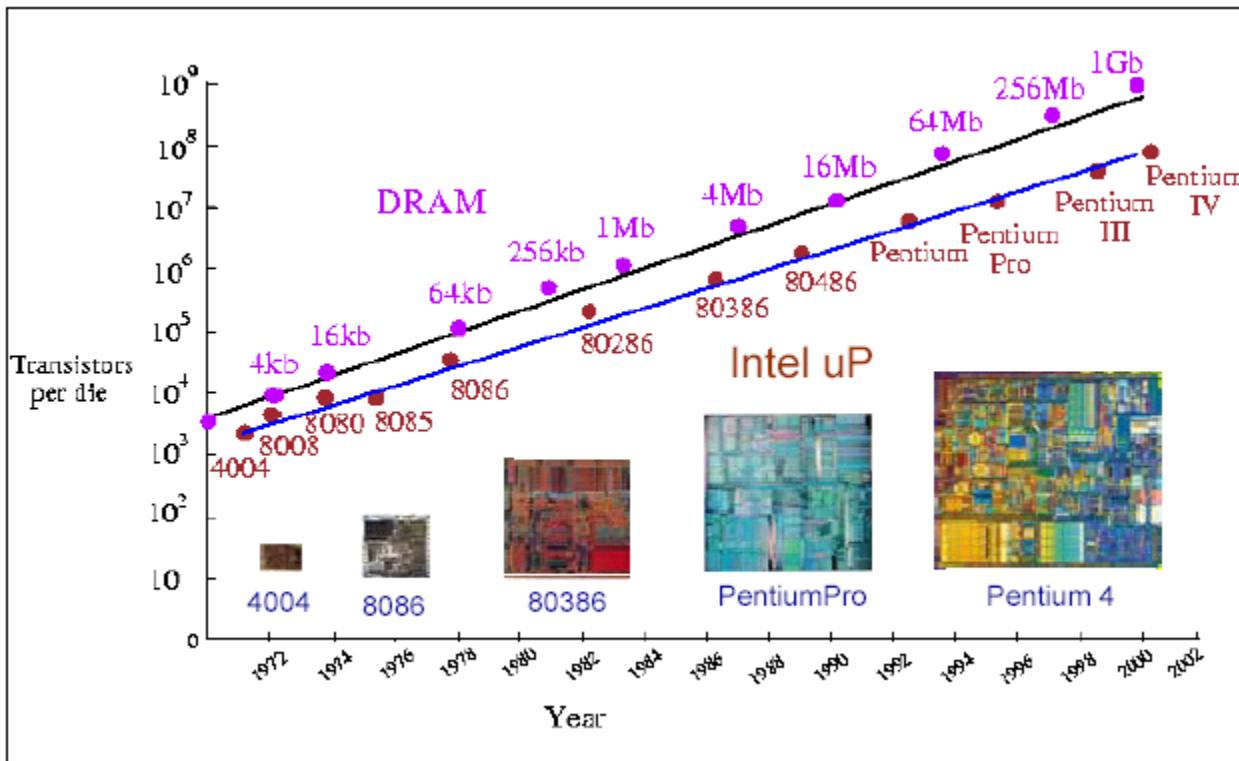
500M~ 1Billion
Transistors





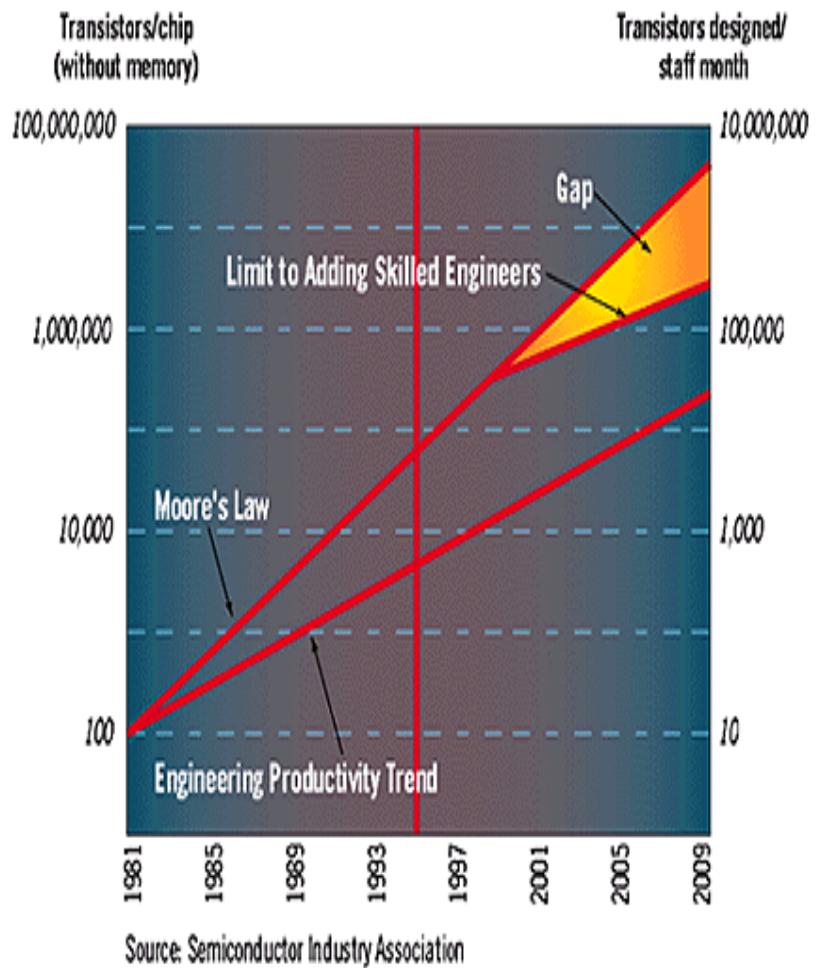
Moore's Law: Driving Technology Advances

- ❖ Logic capacity doubles per IC at regular intervals (1965).
- ❖ Logic capacity doubles per IC every 18 months (1975).





Engineering Productivity Gap

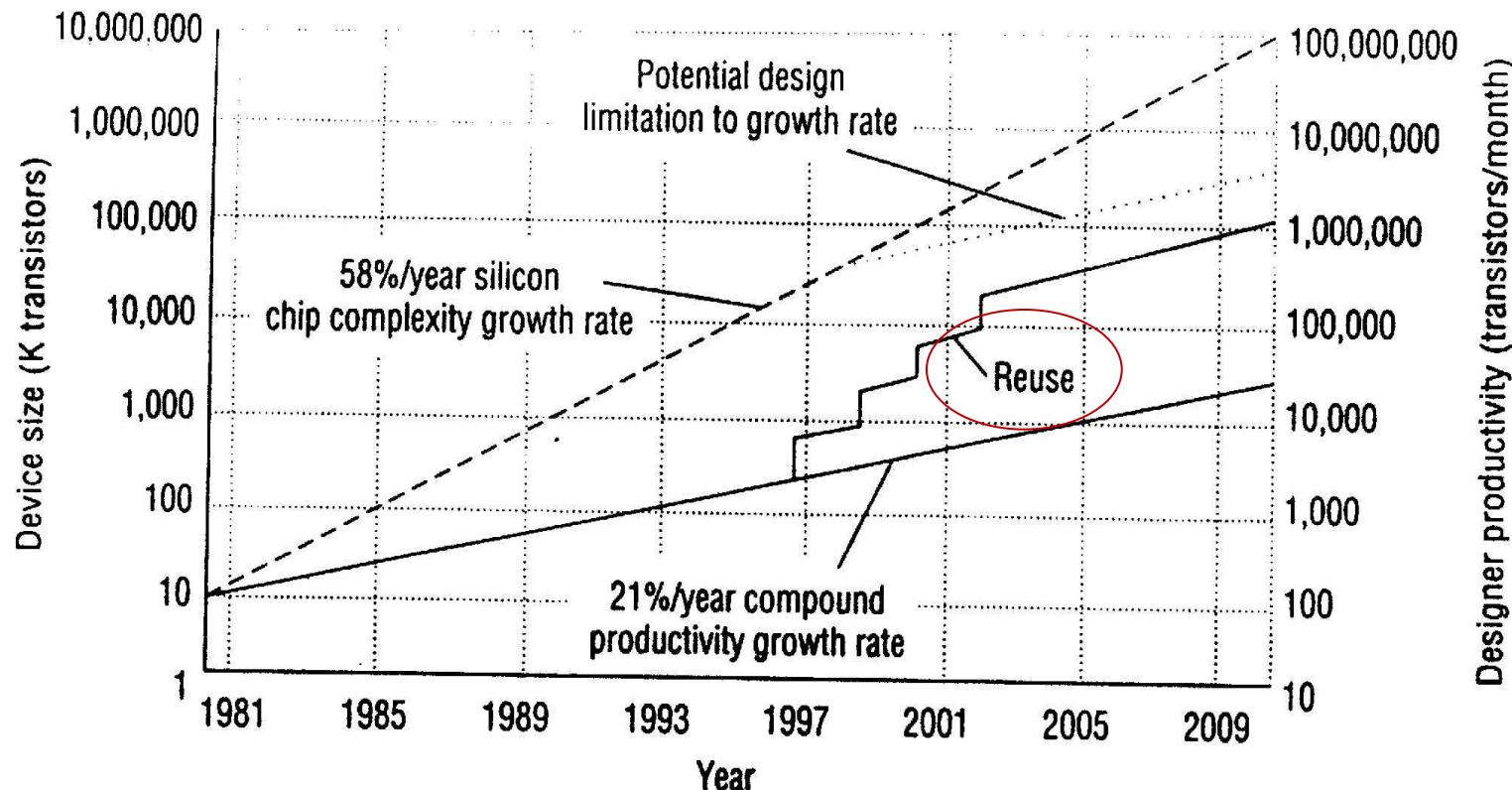


- Engineering productivity has not been keeping up with silicon gate capacity for several years.

- Companies have been using larger design teams, making engineers work longer hours, etc., but clearly the limit is being reached.



Why Must HDL Tools & IP Reuse?



Design productivity crisis:

Divergence of potential design complexity
and designer productivity



HDL and Moore's Law

- ❖ HDL – Hardware Description Language
- ❖ Why use an HDL ?
 - ❖ Unify design entries.
 - ❖ Easy for synthesis:
 - Hardware is becoming very difficult (and too big!) to design directly
 - HDL is easier and cheaper to explore different design options
 - Reduce time and cost to verify your digital designs in VLSI implementations



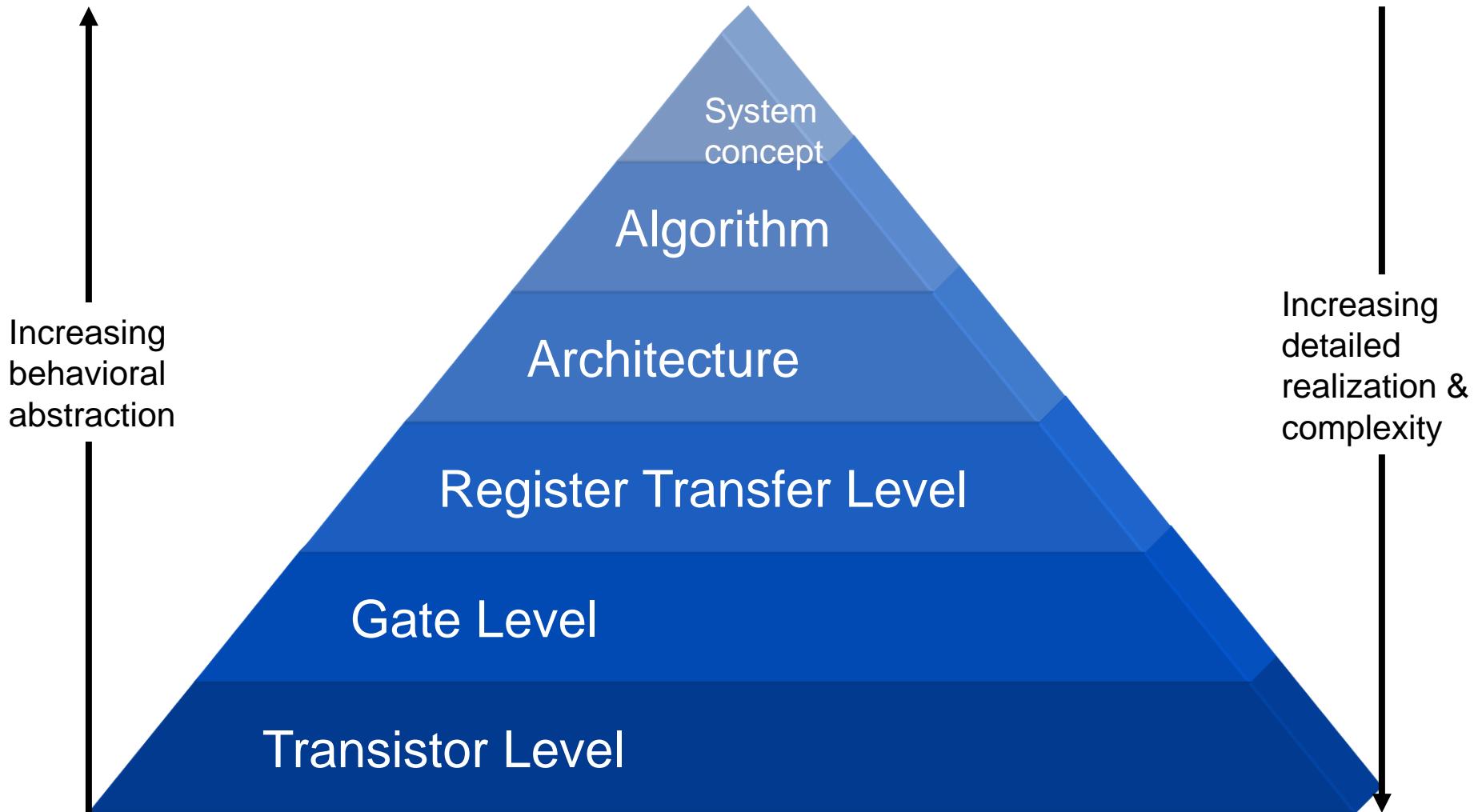
Verilog HDL

❖ Feature

- ❖ HDL has high-level programming language constructs and constructs to describe the connectivity of your circuit.
- ❖ Ability to mix different levels of abstraction freely
- ❖ One language for all aspects of design, test, and verification
- ❖ Functionality as well as timing
- ❖ Concurrency perform target functions
- ❖ Support timing simulation for your design

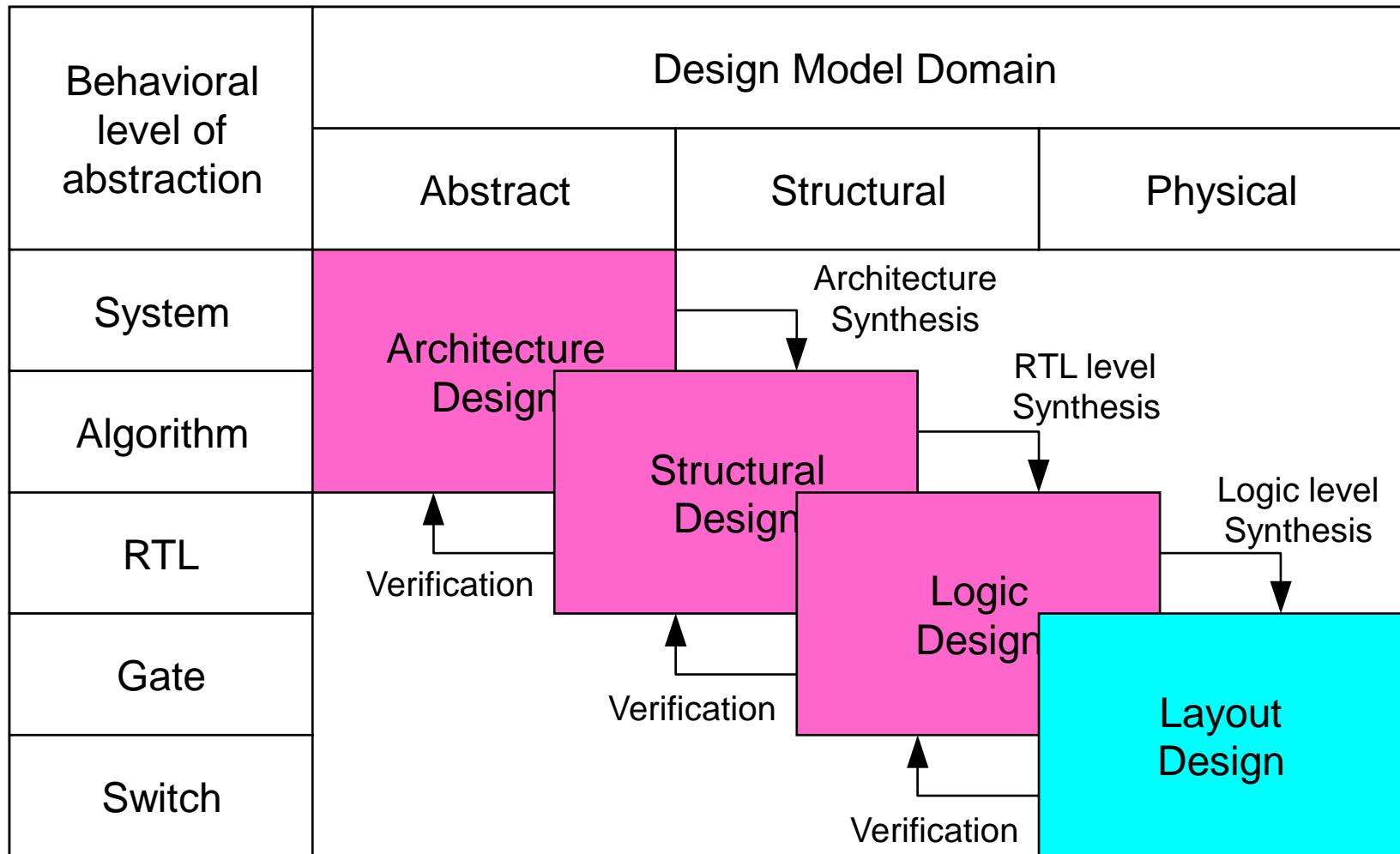


Behavioral Model



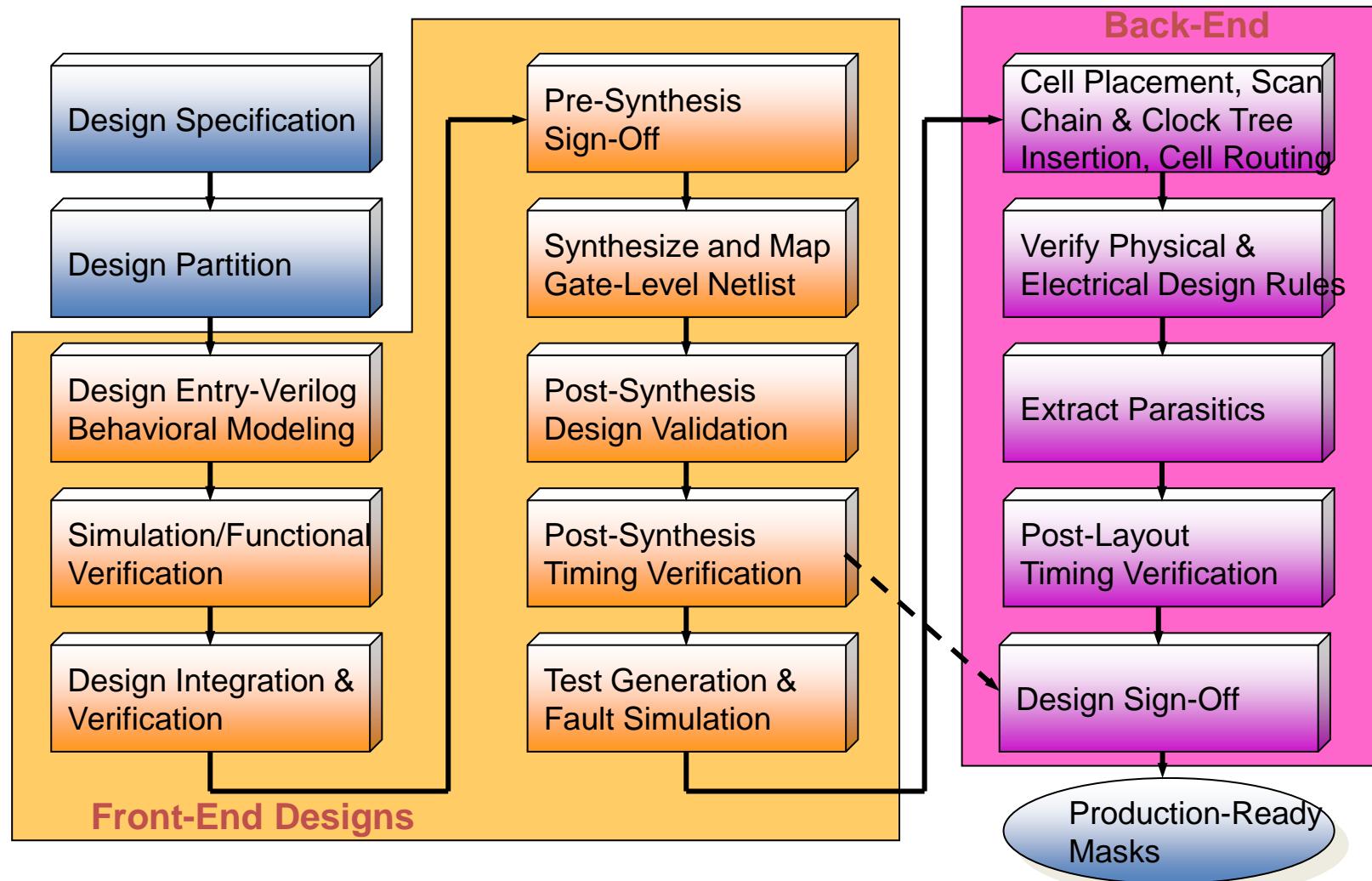


Verilog HDL in Different Design Domains





Digital IC Design Flow for Better Design Productivity



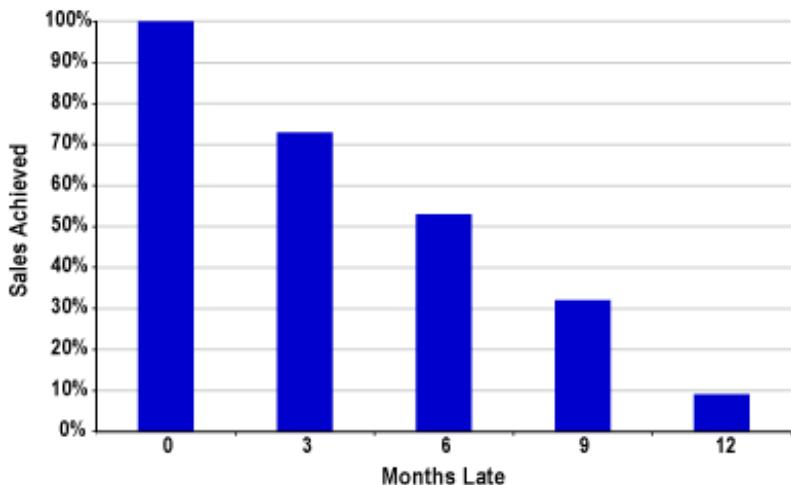


FPGA Prototyping as Design Verification



Cost & Time-to-Market

- ❖ Leading-edge digital system designs are becoming more expensive and time-consuming
 - ❖ Increasing cost of mask sets and the amount of engineering verification required.
 - ❖ Very difficult for a company to react nimbly to competitive pressures or evolving standards.

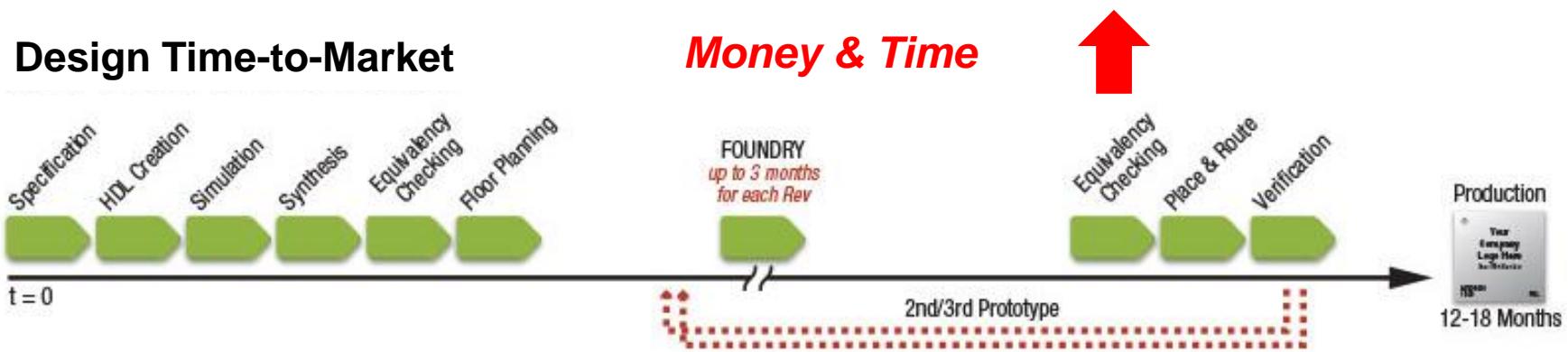


Declining Product Sales Due to Late-to-Market Designs The Cost of Chip Development



Cost & Time-to-Market

- ❖ Leading-edge digital system designs are becoming more expensive and time-consuming
 - ❖ Increasing cost of mask sets and the amount of engineering verification required.
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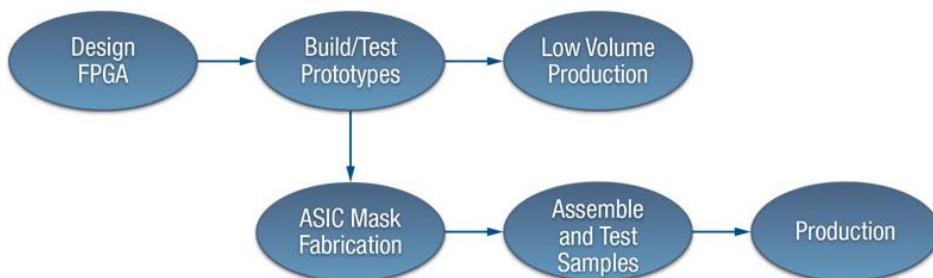
Getting your design “right the first time” is more and more imperative !!!



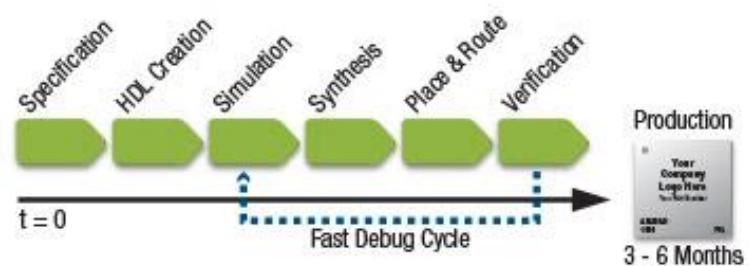
FPGA Prototyping

- ❖ Using an FPGA to prototype an digital system for verification has now become standard practice to:
 - ❖ Both decrease development time and reduce the risk of first silicon failure.
 - ❖ Faster “**emulation**” speed
 - ❖ Realistic system environment
 - ❖ System (HW/SW) development platform

Design process for developing a product with an FPGA
and converting the FPGA to an ASIC for production.

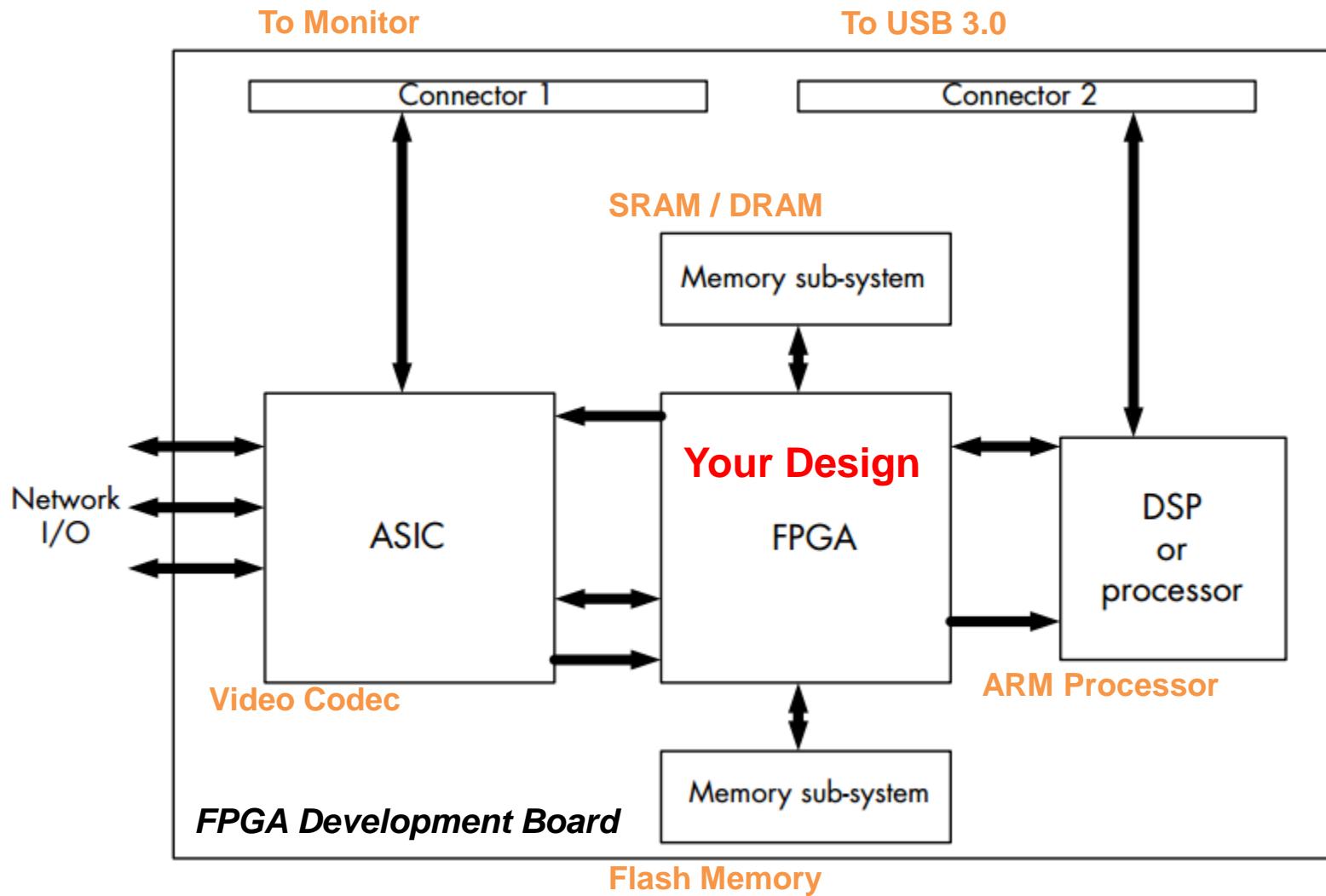


Design Time-to-Market





Verification Platform





FPGA Design Flow

